

**Radiation Hardened Octal Buffer/Line Driver, Three-State**

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCS244T is a Radiation Hardened Non-Inverting Octal Buffer/Line Driver, Three-State, with two active-low output enables.

**Specifications**

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the HCS244T are contained in SMD 5962-95731.** A "hot-link" is provided from our website for downloading.

[www.intersil.com/spacedefense/newsafclasst.asp](http://www.intersil.com/spacedefense/newsafclasst.asp)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/quality/manuals.asp](http://www.intersil.com/quality/manuals.asp)

**Ordering Information**

ORDERING INFORMATION	PART NUMBER	TEMP. RANGE (°C)
5962R9573101TRC	HCS244DTR	-55 to 125
5962R9573101TXC	HCS244KTR	-55 to 125

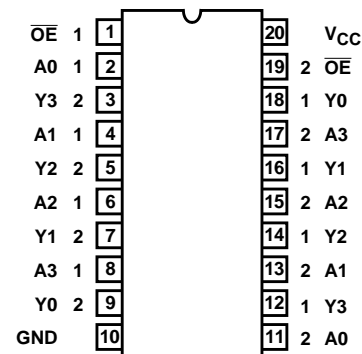
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

**Features**

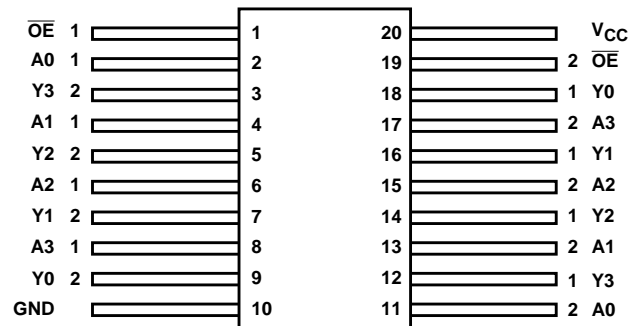
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets:  $>100$  MEV-cm<sup>2</sup>/mg
  - Single Event Upset (SEU) Immunity  $< 2 \times 10^{-9}$  Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened CMOS SOS
- Fanout (Over Temperature Range)
- Bus Driver Outputs - 15 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - $V_{IL} = 0.3 V_{CC}$  Max
  - $V_{IH} = 0.7 V_{CC}$  Min
- Input Current Levels  $I_i \leq 5\mu A$  at  $V_{OL}, V_{OH}$

**Pinouts**

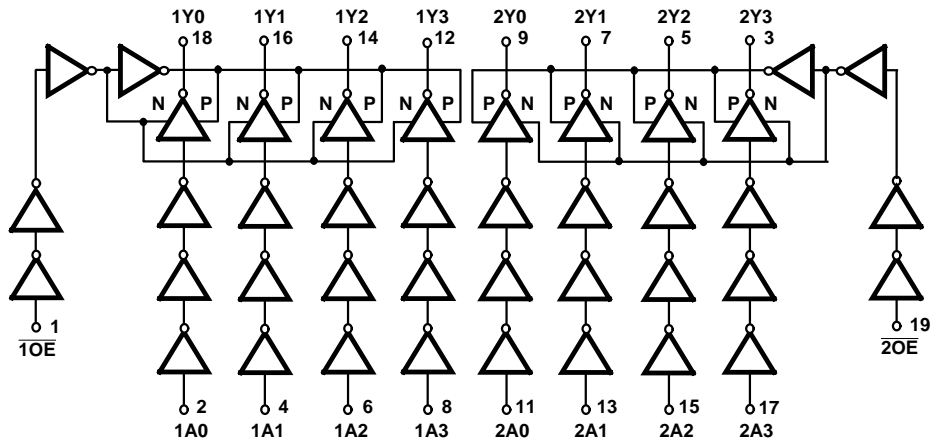
**HCS244DTR (SBDIP), CDIP2-T20**  
TOP VIEW



**HCS244KTR (FLATPACK), CDFP4-F20**  
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
1OE, 2OE	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage Level  
 L = Low Voltage Level  
 X = Immaterial  
 Z = High Impedance

# HCS244T

## Die Characteristics

### DIE DIMENSIONS:

(2747 $\mu$ m x 2693 $\mu$ m x 533 $\mu$ m  $\pm$ 51.0 $\mu$ m)  
108 x 106 x 21mils  $\pm$ 2mil

### METALLIZATION:

Type: Al Si  
Thickness: 11.0k $\text{\AA}$   $\pm$ 1k $\text{\AA}$

### SUBSTRATE POTENTIAL:

Unbiased Silicon on Sapphire

### BACKSIDE FINISH:

Sapphire

### PASSIVATION:

Type: Silox (SiO<sub>2</sub>)  
Thickness: 13.0k $\text{\AA}$   $\pm$ 2.6k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm<sup>2</sup>

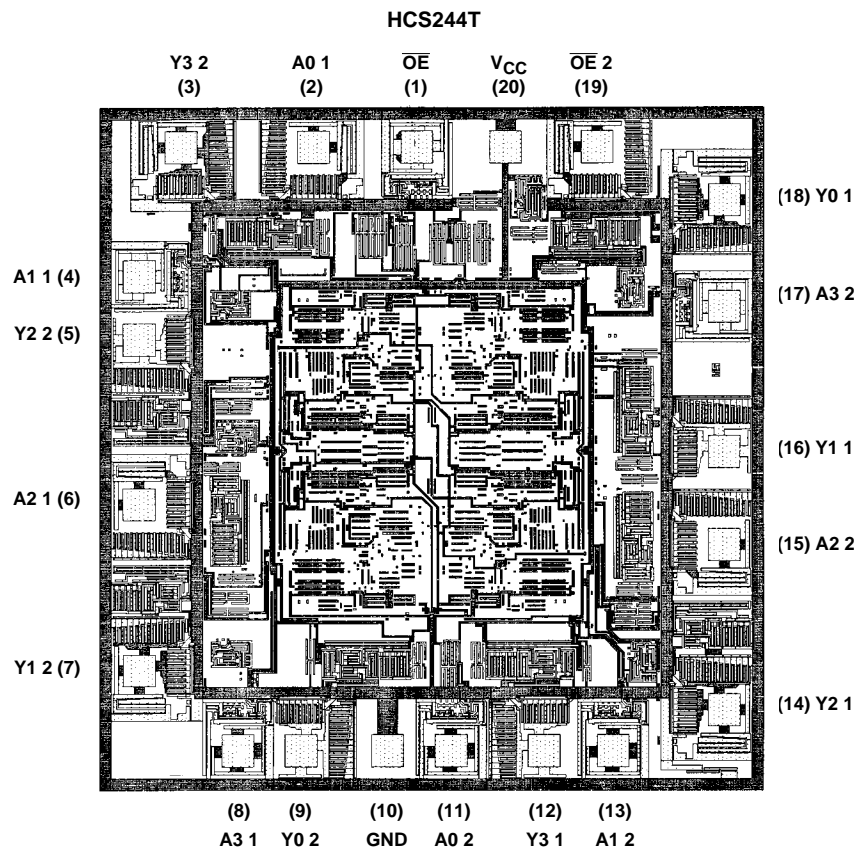
### TRANSISTOR COUNT:

224

### PROCESS:

CMOS SOS

## Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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