

January 1996

### Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96704 and Intersil's Intersil QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose ..... >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <math> <1 \times 10^{-10}</math> Errors/Bit/Day (Typ)
- SEU LET Threshold ..... >100 MEV-cm<sup>2</sup>/mg
- Dose Rate Upset ..... >10<sup>11</sup> RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability ..... >10<sup>12</sup> RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range ..... 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay ..... 21ns (Max), 14ns (Typ)

### Description

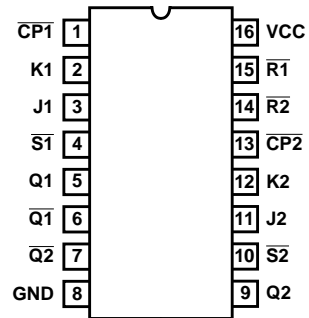
The Intersil ACS112MS is a Radiation Hardened Dual J-K Flip-Flop with Set and Reset. The output change states on the negative transition of the clock (CP1N or CP2N).

The ACS112MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

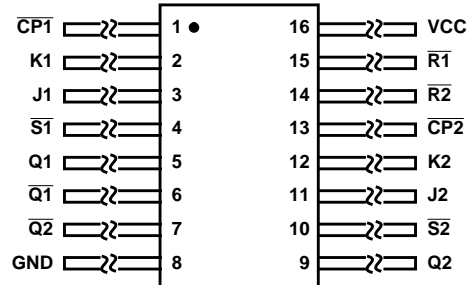
The ACS112MS is supplied in a 16 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

### Pinouts

16 PIN CERAMIC DUAL-IN-LINE  
MIL-STD-1835, DESIGNATOR CDIP2-T16,  
LEAD FINISH C  
TOP VIEW



16 PIN CERAMIC FLATPACK  
MIL-STD-1835, DESIGNATOR CDFP4-F16,  
LEAD FINISH C  
TOP VIEW



### Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9670401VEC	-55°C to +125°C	MIL-PRF-38535 Class V	16 Lead SBDIP
5962F9670401VXC	-55°C to +125°C	MIL-PRF-38535 Class V	16 Lead Ceramic Flatpack
ACS112D/Sample	25°C	Sample	16 Lead SBDIP
ACS112K/Sample	25°C	Sample	16 Lead Ceramic Flatpack
ACS112HMSR	25°C	Die	Die