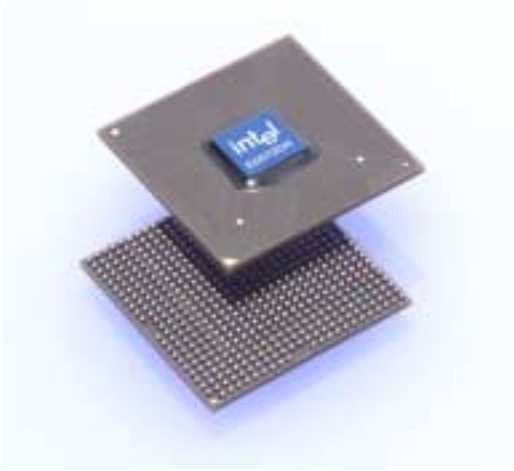
Intel® 82870DH DDR Memory Hub (DMH) Datasheet

Product Features

- Two independent DDR DIMM channels per DMH.
  - — 4 DIMMs per DDR Channel.
  - — Registered PC1600 DDR DIMMs.
- Write Buffers to minimize large turnaround times.
- Pass through architecture for Read and Write accesses.
- Supports 128 Mb, 256 Mb, 512 Mb and 1 Gb DDR SDRAM technologies.
- Each DMH supports a wide range of memory size.
  - — Up to 4 GB using 128 Mb device.
  - — Up to 8 GB using 256 Mb device.
  - — Up to 16 GB using 512 Mb device.
  - — Up to 32 GB using 1 Gb device.
- Support of RDRAM CMOS signals to facilitate initialization and read/write of registers.
- DMH internal registers accessed through CMOS signal interface.
- Tunnels DDR SDRAM protocol over RSL.
- Integrated System Management Bus (SMB) controller to read and write data from/to SPD EEPROM on the DIMMs.
- 1.6 GB/s data rates in either 16-byte or 32-byte DDR DIMM transfer mode.
- 567 pin OLGA package.



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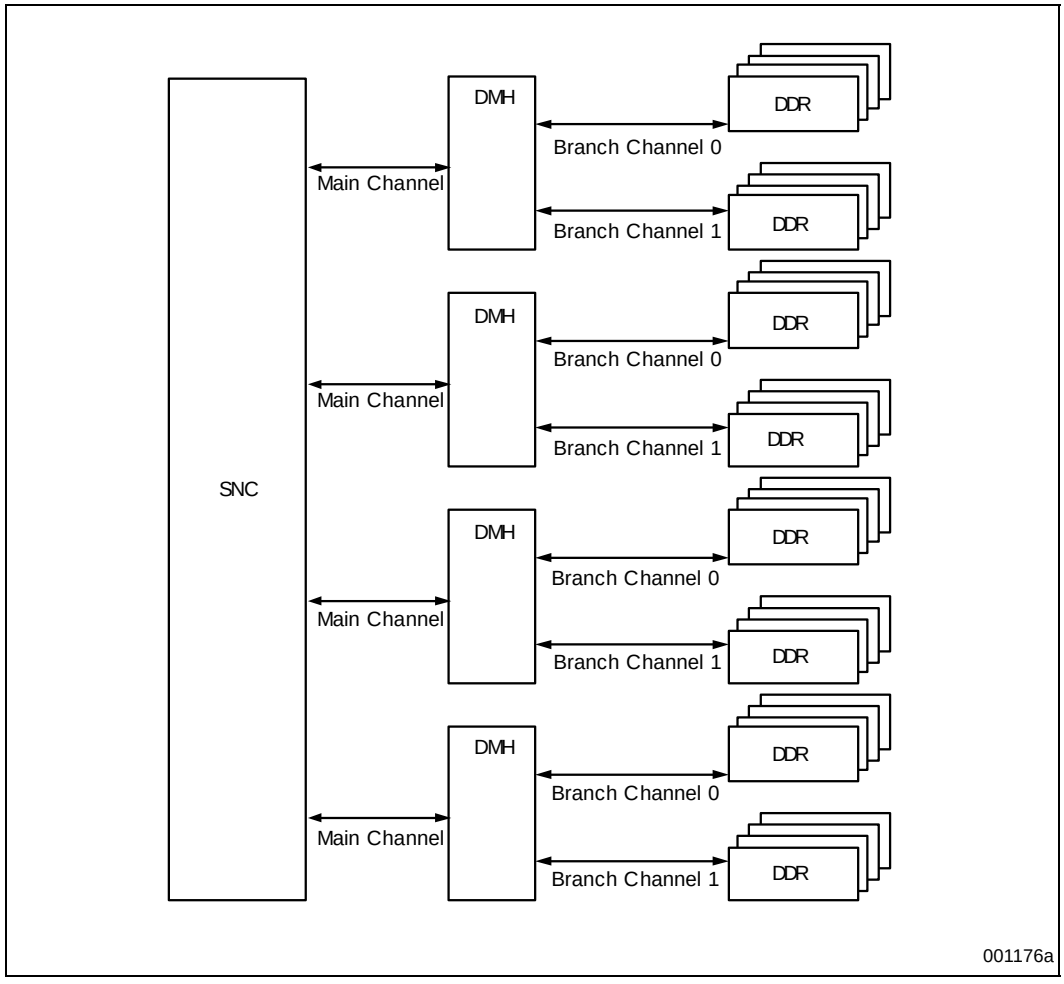
Overview 1

1.1 System Architecture

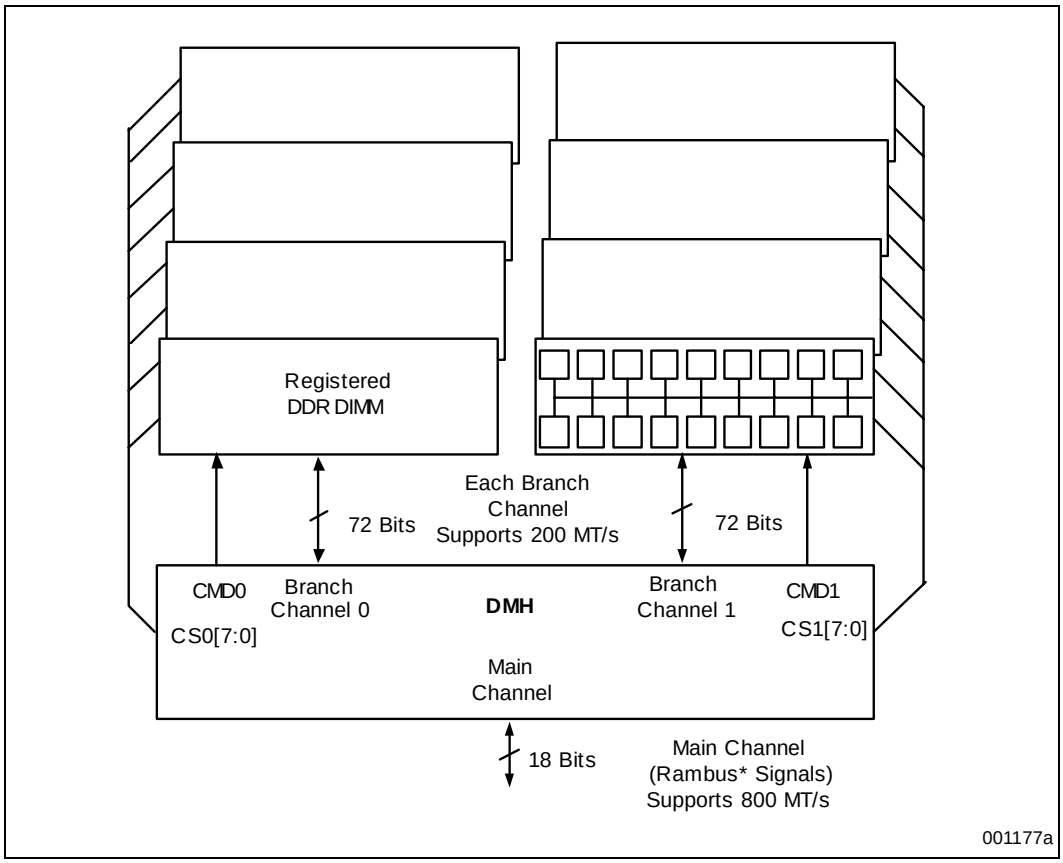
The DDR Memory Hub (DMH) is a memory translator hub that provides a mechanism for tunneling DDR SDRAM transactions between a Main Channel (RAMBUS* interface) and two Branch Channels (DDR SDRAM interfaces). While all RAMBUS signals maintain electrical compatibility with RDRAM pins, the RAMBUS signals are logically redefined to packetize DDR SDRAM I/O traffic. The DMH tunnels SDRAM packets between the Main Channel and a Branch Channel with deterministic timing.

Figure 1-1. Fully Loaded SNC Example



The DMH interfaces two 8-byte-wide DDR DIMM channels to a single, 2-byte-wide Main Channel as shown in Figure 1-2. Each DDR DIMM channel may contain from 0 to 4 DIMMs. The DMH supports a maximum of 8 DIMMs (4 each on each branch channel), and requires at least 1 DIMM.

Figure 1-2. DMH Driving Both DIMM Channels, Four DIMMs per Channel



The DMH facilitates memory devices isolation and correction for X4 memory geometries. The DMH facilitates this by ensuring that no data bit is mapped onto the same SDRAM device as any of its ECC bits. The mapping allows the Scalability Node Controller (SNC) to organize data and ECC symbols in an arrangement that allows ECC to reconstruct all four bits of data associated with a failed SDRAM device.

1.2 Supported Memory Configurations

The DMH supports 128 Mb, 256 Mb, 512 Mb, and 1 Gb[1] PC1600 DDR SDRAM memory technologies in 4-bank, X4 and X8 geometries, on 184-pin DIMMs.

1.2.1 Memory Capacity

Table 1-1 defines the minimum and maximum memory configurations supported by the DMH with various DDR SDRAM technologies.

1. 1 Gb devices are not validated at the time of writing.

Table 1-1. Memory Size

DDR SDRAM Technology	DIMM Size	DDR DIMM Device Organization[a]	Minimum Configuration[b]	Maximum Configuration[c]
128 Mb	16Mx72 (128MB)	4M x 8 bit x 4 Bank x 9 DRAMs/Side x 1 Side	128 MB	1 GB
	32Mx72 (256MB)	4M x 8 bit x 4 Bank x 9 DRAMs/Side x 2 Sides 8M x 4 bit x 4 Bank x 18 DRAMs/Side x 1 Side	256 MB	2 GB
	64Mx72 (512MB)	8M x 4 bit x 4 Bank x 18 DRAMs/Side x 2 Sides	512 MB	4 GB
256 Mb	32Mx72 (256MB)	8M x 8 bit x 4 Bank x 9 DRAMs/Side x 1 Side	256 MB	2 GB
	64Mx72 (512MB)	8M x 8 bit x 4 Bank x 9 DRAMs/Side x 2 Sides 16M x 4 bit x 4 Bank x 18 DRAMs/Side x 1 Side	512 MB	4 GB
	128Mx72 (1GB)	16M x 4 bit x 4 Bank x 18 DRAMs/Side x 2 Sides	1 GB	8 GB
512 Mb	64Mx72 (512MB)	16M x 8 bit x 4 Bank x 9 DRAMs/Side x 1 Side	512 MB	4 GB
	128Mx72 (1GB)	16M x 8 bit x 4 Bank x 9 DRAMs/Side x 2 Sides 32M x 4 bit x 4 Bank x 18 DRAMs/Side x 1 Side	1 GB	8 GB
	256Mx72 (2GB)	32M x 4 bit x 4 Bank x 18 DRAMs/Side x 2 Sides	2 GB	16 GB
1 Gb	128Mx72 (1GB)	32M x 8 bit x 4 Bank x 9 DRAMs/Side x 1 Side	1 GB	8 GB
	256Mx72 (2GB)	32M x 8 bit x 4 Bank x 9 DRAMs/Side x 2 Sides 64M x 4 bit x 4 Bank x 18 DRAMs/Side x 1 Side	2 GB	16 GB
	512Mx72 (4GB)	64M x 4 bit x 4 Bank x 18 DRAMs/Side x 2 Sides	4 GB	32 GB

a. A DIMM Side is defined as a group of DRAMs that share a common Chip Select.
b. DMH configured with 1 DDR DIMM on 1 Branch Channel.
c. DMH configured with 4 DDR DIMMs on each (of 2) Branch Channel, for a total of 8 DIMMs.

1.3 Terminology

SNC	Scalable Node Controller. Processor system bus interface and memory controller for the Intel® E8870 chipset.
RSL	RAMBUS Signaling Level. The name of the signaling technology used by RAMBUS.
SSTL_2	Stub Series Terminated Logic. Signal levels used in DDR DIMM data I/O.
RAC	RAMBUS ASIC Cell. It is the embedded cell designed by RAMBUS that interfaces with the RAMBUS devices using RSL signaling. The RAC communicates to the RMC.
RMC	RAMBUS Memory Controller. This is the logic that directly interfaces to the RAC.

DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory as defined by the Jedec DDR SDRAM specification.
DIMM	Dual Inline Memory Module.
MCP	Memory Control Packets.
DMH	DDR Memory Hub.
Main Channel	The RAC signals used to communicate with SNC.
Branch Channel	A DDR DIMM bus.
CFM	Clock From Master - Main Channel Receive clock.
CTM	Clock To Master - Main Channel Transmit clock.
RQ	Main Channel Request Control Signals (RSL signal level).
DQA/DQB	Main Channel Data Signals (RSL signal level).
MSIO Bus	The Main Channel Serial I/O bus. Uses the RAC serial I/O CMOS signals.
BSIO Bus	The Branch Channel Serial I/O bus. This is the DIMM Serial Presence Detect interface.
MT/s	Mega-Transfers per second.

1.4 Reference Documents

- Jedec Standard JESD-21C
- Jedec Standard 79 (JESD79)
- I^2C Bus Specifications, Version 2.0
- *Intel® E8870 Scalable Node Controller (SNC) Datasheet*

1.5 Revision History

Revision Number	Description	Date
-001	Initial release of this document.	August 2002

Signal Description 2

The following notations are used to describe the signal types and their drive state:

- I Input pin
- O Output pin
- I/O Bidirectional input/output pin
- Z Tri-stated
- L Driven low
- H Driven high
- ? Output state is indeterminate

2.1 Main Channel Interface

The Main Channel is the interface between the SNC and DMH.

Table 2-1. Main Channel Interface Signals

Signal	Type	State during PWRGOOD Deassertion	Description
DQA[8:0]	I/O RSL	?	**Data Bus, Data Byte A**: Bidirectional 9-bit data bus A. These correspond to the DQA[8:0] signals on the RAC.
DQB[8:0]	I/O RSL	?	**Data Bus, Data Byte B**: Bidirectional 9-bit data bus B. These correspond to the DQB[8:0] signals on the RAC.
RQ[7:0]	I RSL	I	**Request Control**: These signals carry the memory control packets (MCP) from the SNC to the DMH. These correspond to the RRq[2:0] and CRq[4:0] signals on the RAC.
SIO	I/O CMOS 1.8V	I	**Serial I/O Chain**: Serial input/output pins used for reading and writing control registers.
SCK	I CMOS 1.8V	I	**Serial Clock**: Clock source used for timing of the SIO and CMD signals. This corresponds to the SCK signal on the RAC.
CMD	I CMOS 1.8V	I	**Serial Command**: Serial command input used for control register read and write operations. This corresponds to the CMD signal on the RAC.
CTM	I RSL	I	**Clock to RAC Master**: One of the two differential transmit clock signals used for DMH to RAC Master operations.
CTMN	I RSL	I	**Clock to RAC Master Complement**: One of the two differential transmit clock signals used for DMH to RAC Master operations.

Table 2-1. Main Channel Interface Signals (Continued)

Signal	Type	State during PWRGOOD Deassertion	Description
CFM	I RSL	I	**Clock from RAC Master**: One of the differential receive clock signals used for RAC Master to DMH operation.
CFMN	I RSL	I	**Clock from RAC Master Complement**: One of the differential receive clock signals used for RAC Master to DMH operation.

2.2 Branch Channel Interface

The DMH drives two DDR Branch Channels. Channel 0 signals are prefixed with BC0 and channel 1 with BC1. Except for Table 2-2, the prefix is omitted in this document when discussing an aspect of the signal that applies to both ports. Unless specified in Table 2-2, signals on BC0 and BC1 are electrically identical, meaning they use the same voltage and current levels.

Table 2-2. Branch Channel Interface Signals

Signal	Type	State during PWRGOOD Deassertion	Description
BC0A[14:0] BC1A[14:0]	O SSTL_2 Class II	L	**SDRAM Address**: Used for providing multiplexed row and column address to SDRAM. Each set of address pins can drive up to eight rows of SDRAM.
BC0BA[1:0] BC1BA[1:0]	O SSTL_2 Class II	L	**SDRAM Bank Active**: Used to select the bank within a device.
BC0DQ[71:0] BC1DQ[71:0]	I/O SSTL_2 Class II	Z	**SDRAM Data**: BC0DQ and BC1DQ are independent to allow different data to be read or written on both ports simultaneously.
BC0RAS# BC1RAS#	O SSTL_2 Class II	L	**SDRAM Row Address Strobe**: Used with CS#, CAS# and WE# to specify the SDRAM command. Each signal can drive up to eight SDRAM rows. CS# selects the row.
BC0CAS# BC1CAS#	O SSTL_2 Class II	L	**SDRAM Column Address Strobe**: Used with CS#, RAS# and WE# to specify the SDRAM command. These signals are used to latch the column and bank addresses. Each signal can drive up to eight SDRAM rows.
BC0WE# BC1WE#	O SSTL_2 Class II	L	**SDRAM Write Enable**: Used with CS#, CAS# and RAS# to specify the SDRAM command. These signals are used for write and precharge operations of SDRAM. Each signal can drive up to eight SDRAM rows.
BC0CS#[7:0] BC1CS#[7:0]	O SSTL_2 Class II	L	**SDRAM Chip Select**: These signals are used for selecting one of eight SDRAM rows. CS#[0] is used to select the first row and CS#[1] is used to select a second row if present, etc. to CS#[7] which selects the last row.
BC0CKE BC1CKE	O SSTL_2 Class II	L	**SDRAM Clock Enable**: These signals are used for signaling commands to an SDRAM row.

Table 2-2. Branch Channel Interface Signals (Continued)

Signal	Type	State during PWRGOOD Deassertion	Description
BC0SCLK[3:0] BC0SCLK#[3:0] BC1SCLK[3:0] BC1SCLK#[3:0]	O SSTL_2 Class II	L H L H	**SDRAM Clocks**: One pair of differential clock signals for each DIMM.
BC0DQS[17:0] BC1DQS[17:0]	I/O SSTL_2 Class II	Z	**SDRAM Data Strobe**: DDR data strobes. Some of these pins are dual mode, and are DQM pins for X8 memory configuration as specified in Jedec Standard JESD79.
SREF	O SSTL_2 Class II	L	**SDRAM Feedback Output**: Used to calibrate the SDRAM clock.
SREFFB	I SSTL_2 Class II	I	**SDRAM Feedback Input**: Used to calibrate the SDRAM clock.
BC0SRCAL BC1SRCAL	I/O SSTL_2 Class II	Z	**Slew-rate Calibration**: BC0 tied to ground through 50 Ohm resistor BC1 tied to VCC25 through 50 Ohm resistor
SDA	I/O CMOS Open Drain 2.5V	Z	**Serial Data/Address**: Used to read and write the Serial Presence Detect EEPROMS associated with the DIMMs Controlled by this DMH.
SCL	I/O CMOS Open Drain 2.5V	Z	**Serial Clock**: Used to read and write the Serial Presence Detect EEPROMS associated with the DIMMs Controlled by this DMH.

2.3 Reset and Test Signals

Table 2-3. Reset and Miscellaneous Signals

Signal	Type	State during PWRGOOD Deassertion	Description
TSO	I CMOS Open Drain 2.5V	I	Disables all outputs except TSO and XOROUT.
PWRGOOD	I CMOS 1.8V	I	**Power Good**: This pin is used for asynchronous reset of the entire DMH.
RESET#	I CMOS 1.8V	I	**DMH Reset**: This signal is used for resetting the DMH internal logic during power up sequence.
XORIN	I CMOS 1.8V	I	Parametric XOR tree input.
XOROUT	O CMOS 1.8V	?	Parametric XOR tree output.

2.4 Voltage References

Table 2-4. Voltage Reference Signals

Signal	Description
VREF[A,B]RAC	RSL reference voltage for the RAC.
VCCRAC	1.8V digital power for RAC. 1.8V source for DMH core operation. 1.8V source for CMD, SCK, and SIO pins.
VCCRACA	Filtered Analog V_{CC}: Provide V_{CC} to RAC interface DLL.
VCCDLY	Filtered 1.8V for the DMH internal delay cells.
VCC25	2.5V source for DDR and 2.5V I/Os.
VSS	Ground
AD[0:1]VREF	DDR Address VREF
BC0VREF[A,B,C] BC1VREF[A,B,C]	DDR VREF
BC0VSSA[A,B,C] BC1VSSA[A,B,C]	DDR VREF Vss

Registers 3

The DMH has internal configuration and control registers. These registers are accessed via the MSIO bus (see Section 4.11, “Serial Interface”).

3.1 Gen – General Purpose Register

Address: **01h**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:0	General purpose R/W register.

3.2 DSTIM – DIMM Strobe Timing Register

Address: **02h**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Offsets each DIMM read-strobe-capture-window forward, relative to the base setting contained in the t_{DPL} field.

Bit	Description
15:14	Branch Channel 1, DIMM 7 Strobe Offset (t_{DSD7})**:** Bits [15:14] t_{DSD7} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3
13:12	Branch Channel 1, DIMM 6 Strobe Offset (t_{DSD6}): Bits [13:12] t_{DSD6} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3
11:10	Branch Channel 1, DIMM 5 Strobe Offset (t_{DSD5}): Bits [11:10] t_{DSD5} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3

Bit	Description
9:8 (cont'd)	Branch Channel 1, DIMM 4 Strobe Offset (t_{DSD4}): Bits [9:8] t_{DSD4} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3
7:6	Branch Channel 0, DIMM 3 Strobe Offset (t_{DSD3}): Bits [7:6] t_{DSD3} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3
5:4	Branch Channel 0, DIMM 2 Strobe Offset (t_{DSD2}): Bits [5:4] t_{DSD2} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3
3:2	Branch Channel 0, DIMM 1 Strobe Offset (t_{DSD1}): Bits [3:2] t_{DSD1} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3
1:0	Branch Channel 0, DIMM 0 Strobe Offset (t_{DSD0}): Bits [1:0] t_{DSD0} in CFMs 0 0 0 0 1 1 1 0 2 1 1 3

3.3 MCTIM – Main Channel Timing Register

Address: **03h**
Default: **0006h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:13	Reserved
12	Data Transfer Size (DTS): 1 = 16-byte Mode. The DMH transfers 16 bytes of data for each access. 0 = 32-byte Mode. The DMH transfers 32 bytes of data for each access.
11	Reserved
10:8	Main Channel Read Delay (t_{LVL}): Set by a SNC initialization procedure. Specifies the number of CTM pipe stages that data is delayed from the time that it appears at the DQS I/O pins of the DMH to the time it is driven at the DQA/DQB I/O pins of the DMH. Bit[7:4] — t_{LVL} in CFMs 0 0 0 — 2 0 0 1 — 3 0 1 0 — 4 0 1 1 — 5 1 0 0 — 6 1 0 1 — 7 1 1 0 — 8 1 1 1 — 9
7:5	Reserved
4:0	Main Channel Write Delay (t_{CWD}): Specifies additional pipestage delays from the completion of a MCP Write Command, to the beginning of the write data transfer. Bit[4:0] — t_{CWD} in CFMs — Bit[4:0] — t_{CWD} in CFMs 0 0 0 0 0 — Reserved — 1 0 0 0 0 — 15 0 0 0 0 1 — Reserved — 1 0 0 0 1 — 16 0 0 0 1 0 — Reserved — 1 0 0 1 0 — 17 0 0 0 1 1 — Reserved — 1 0 0 1 1 — 18 0 0 1 0 0 — Reserved — 1 0 1 0 0 — 19 0 0 1 0 1 — Reserved — 1 0 1 0 1 — 20 0 0 1 1 0 — 5 — 1 0 1 1 0 — 21 0 0 1 1 1 — 6 — 1 0 1 1 1 — 22 0 1 0 0 0 — 7 — 1 1 0 0 0 — 23 0 1 0 0 1 — 8 — 1 1 0 0 1 — 24 0 1 0 1 0 — 9 — 1 1 0 1 0 — 25 0 1 0 1 1 — 10 — 1 1 0 1 1 — 26 0 1 1 0 0 — 11 — 1 1 1 0 0 — 27 0 1 1 0 1 — 12 — 1 1 1 0 1 — 28 0 1 1 1 0 — 13 — 1 1 1 1 0 — 29 0 1 1 1 1 — 14 — 1 1 1 1 1 — 30

3.4 BCTIM – Branch Channel Timing Register

Address: **04h**
Default: **0002h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:9	Reserved
8	Manual DIMM Path Latency Calibration Enable (DPLE): Setting this bit to 1 causes the DMH to perform a DIMM Path Latency calibration on both branch channels. Upon completion of the calibration, the DMH resets the bit to 0. The Main channel should remain quiescent throughout the calibration procedure. The results of this command are stored in the t_{DPL} field of this register.
7	Reserved
6:4	Branch Channel DIMM Path Latency (t_{DPL}): Specifies the number of CFM round-trip delays from the time a DIMM drives data to the time it appears at the I/O pins of the DMH. This field is typically set by the DIMM path calibration procedure (see DPLE field above), but can be set manually as well. Bit[6:4] t_{DPL} in CFMs 0 0 0 0 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7
3	Reserved
2:0	DIMM CAS Latency (t_{CL}): This bit specifies the number of SCLKs from when a read command is sampled by the SDRAMs to when the DMH samples read data from the SDRAMs. Bit[2:0] t_{CL} in SCLKs 0 0 0 Reserved 0 0 1 Reserved 0 1 0 2 0 1 1 Reserved 1 0 0 Reserved 1 0 1 1.5 1 1 0 2.5 1 1 1 Reserved

3.5 DGR – DIMM Geometry Register

Address: **05h**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:8	Reserved
7:0	Branch Channel Geometry: Each bit specifies the X4 or X8 geometry of a single or double-density DIMM. This configures the DMH to respond to the appropriate DIMM data strobes and drive dual-use DQM pins appropriately. Setting a bit to 0 indicates X4 geometry, while setting a bit to one specifies X8 geometry. Bit Description 0 Controls geometry for Branch Channel 0, DIMM0 1 Controls geometry for Branch Channel 0, DIMM1 2 Controls geometry for Branch Channel 0, DIMM2 3 Controls geometry for Branch Channel 0, DIMM3 4 Controls geometry for Branch Channel 1, DIMM0 5 Controls geometry for Branch Channel 1, DIMM1 6 Controls geometry for Branch Channel 1, DIMM2 7 Controls geometry for Branch Channel 1, DIMM3

3.6 MRF – Mode Register Set Function Register

Address: **06h**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15	Reserved
14:0	Mode Register Function (MRF): A[14:0] bit values to be used with MRS command of **SDI** register below. See MRF bits of the **SDI** register below.

3.7 SDI – SDRAM Initialization Register

Address: **07h**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:11	Reserved
10	Broadcast SIC (BRD): When this bit is set to 1, the command specified by the SIC field (bits [2:0]) is issued to all SDRAM rows on both branch channels. When this bit is 0, the SIC command is issued only to the branch channel and row specified by the BC and CS fields.
9:8	Mode Register Function (MRF): These bits define the value of BA[1:0] driven on the SDRAM pins during an MRS command. The bits driven onto A[14:0] are defined in the preceding MRF register.
7	Initiate SIC Operation (ISO): When set to 1, the execution of the command specified in the SIC field starts. After the execution is complete, the DMH clears this bit to 0. The software must check to see if this bit is 0 before writing to this register.
6	Branch Channel (BC): Specifies the branch channel to be used with the SIC operation when the BRD field is set to 0. 1 = Branch Channel 1 1 = Branch Channel 0
5:3	DIMM Side Select (CS): Specifies the DIMM Side (by Chip Select) to be used with the SIC operation when the BRD field is set to 0. Bits[5:3] DIMM Side Select 0 0 0 CS#[0] 0 0 1 CS#[1] 0 1 0 CS#[2] 0 1 1 CS#[3] 1 0 0 CS#[4] 1 0 1 CS#[5] 1 1 0 CS#[6] 1 1 1 CS#[7]
2.0	SDRAM Initialization Command (SIC): This field allows the DMH to issue various commands to the SDRAM row specified by the CS field, on the branch channel specified by the BC field. This field is provided for BIOS to initialize the SDRAMs. The BIOS programs this field with an appropriate command and then sets the ISO field to logic one. When the DMH observes the ISO field set to 1 it performs the operation specified by the SIC field. Upon completion of the operation, DMH sets the ISO field to logic 0. Bits[2:0] SIC 0 0 0 NOP Command: When DMH receives this command it issues a NOP command to the DIMM side specified by the BC and CS bits of this register. 0 0 1 DDR delay line calibration: When DMH receives this command it issues a DDR delay line calibration sequence to both branch channels. This command sets the DQS strobe delay to 2.2ns. This command ignores CS, BC, and BRD. Do not perform this command while in self-refresh mode. 0 1 0 Precharge: When DMH receives this command it issues a Precharge command to the DIMM side specified by the BC and CS bits of this register. Precharge mode (all banks or single bank) is determined by Bank Address (BA) and precharge all (PA) bits, which are set through the MRF field of this register and the preceding MRF register. Refer to Jedec Standard JESD79 for Precharge command details. 0 1 1 Mode Register Set: When DMH receives this command it issues a Mode Register Set (MRS) command. The MRF bits of this register, combine with the preceding MRF register to define the DDR SDRAM Mode register bits. Refer to Jedec Standard JESD79 for Mode Register Set command details.

Bit	Description	
2:0 (cont'd)	1 0 0	Reserved
	1 0 1	Auto Refresh: When the DMH receives this command it issues an Auto Refresh command to the DIMM side specified by the BC and CS bits of this register. This command ignores BRD.
	1 1 0	Reserved
	1 1 1	Reserved

3.8 RCC – RAMBUS Current Control Register

Address: **0Bh**
Default: **0040h**
Access: **R/W**
Size: **16 bits**

This register returns the value of the RAC's internal Current Calibration register, which is set by performing a manual current calibration or by auto calibration (see Section 4.4.1, "Current Calibration").

Note: The contents written to this register cannot be directly read back. After writing to this register, preform a Manual Current Calibration to load the register contents into the RAC's internal Current Calibration register.

Bit	Description
15:7	Reserved
6:0	Current Control: This seven bit field controls the current for RSL pins DQA[8:0] and DQB[8:0].

3.9 RIR – RAC Initialization Register

Address: **0Ch**
Default: **0000h**
Access: **R/W: RIC, IRO**
R-O: RC, RSP
Size: **16 bits**

Bit	Description
15:6	Reserved
5	Ready for Synchronization Packet (RSP): The DMH sets this bit to 1 when it is ready to accept a Clock-Synchronization MCP. The BIOS must check this bit before sending the Synchronization packet to DMH.
4	RAC Initialization Complete (RC): The DMH sets this bit to 1 after it has completed RAC initialization and clock synchronization. The BIOS must check this bit to make sure the RAC is properly initialized before initiating memory accesses.
3	Initiate RIC Operation (IRO): When set to 1, the execution of the RIC command specified by bits[2:0] starts. After the execution is completed the DMH clears this bit to 0. The software must check to see if this bit is zero before writing to this bit.

Bit	Description
2:0 (cont'd)	RAC Initialization Command (RIC): This field allows the BIOS to initialize DMH RAC. The BIOS programs this field with an appropriate command and sets the IRO field to logic one. The DMH then performs the operation specified by the RIC field. Upon successful completion of the operation, the DMH sets the IRO field to logic zero. For procedures, see Section 4.14.1, "RAC Initialization." Bits[2:0] Description 0 0 0 RAC Power Up Sequence: DMH performs the internal RAC and 200 MHz logic power up sequence. Required to power up and reset the RAC. 0 0 1 RAC Initialization: When the DMH receives this command, it internally performs an Auto-Current and Temperature Calibration of the DMH RAC. Upon completion of the calibration procedures, the DMH sets the RSP bit, indicating that a Clock-Sync packet must now be sent to the DMH. After clock synchronization, the DMH sets the RC bit to logic one and resets the IRO bit to logic zero to indicate successful completion of the procedure. This operation must be performed exactly one time after the RAC Power Up Sequence is performed. 0 1 0 RAC Manual-Current Calibration: When DMH receives this command it issues a Manual-Current Calibration sequence to the RAC, and loads the value contained in the RCC. 0 1 1 RAC Temperature Calibration: When DMH receives this command it issues a Temperature Calibration sequence to the RAC. 1 0 0 Reserved 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved

3.10 SPD – Serial Presence Detect Status Register

Address: **0Fh**
Default: **00FFh**
Access: **R/W: DIV**
R-O: RDO, WOD, BBE, BUSY, DATA
Size: **16 bits**

This register provides an interface between the MSIO bus (SCK, SIO, CMD) and BSIO bus (SCL,SDA) that is used to access the Serial Presence Detect EEPROM. See Section 4.11.4, "BSIO Bus Interface."

Bit	Description
15	Read Data Valid (RDO): This bit is set by the DMH when the Data field of this register receives read data from the SPD EEPROM. It is cleared by the DMH when an MSIO SPDR command is received.
14	Write Operation Done (WOD): This bit is set by the DMH when the SPDW command has been completed on the BSIO bus. It is cleared by the DMH when an MSIO SPDW command is received.
13	BSIO Bus Error (BBE): This bit is set by the DMH if it initiates a BSIO bus transaction that does not complete successfully. It is cleared by the DMH when an MSIO SPDR or SPDW command is received.
12	Busy state (BUSY): This bit is set by the DMH while an SPD command is executing.
11:8	Clock Divider (DIV): Sets the BSIO clock frequency from 100 KHz to 4 KHz. Refer to Section 4.11.4.2, "Clock Divider."
7:0	Data: Holds data read from SPDR commands. Refer to Section 4.11.4.3, "BSIO Request Packet for SPD Random Read."

3.11 PWR – Power Up Control Register

Address: **10h**
Default: **0100h**
Access: **R/W: RVXSEL, RFSV, RSM, RLSM, RBM, RPWRGD, CPWRGD, CKE, RRESET**
R-O: RCSV, RBF, RCL
Size: **16 bits**

This register provides manual access to internal functions that are automatically controlled.

Bit	Description
15:14	Reserved
13	RAC Reset (RRESET): 0 = RAC is alive. 1 = RAC held in reset.
12	RAC Power Good (RPWRGD): 0 = RAC held in reset. 1 = RAC is alive.
11	Core Power Good (CPWRGD): 0 = 200 MHz core held in reset. 1 = 200 MHz core is alive.
10	DIMM Clock Enable (CKE): 0 = Deasserted. 1 = Asserted.
9	RAC Clock Lock (RCL): 0 = Not Locked. 1 = Locked.
8	RAC BIST Failure (RBF): 0 = Passed. 1 = Failed.
7	RAC BIST Mode (RBM): 1 = Enabled. 0 = Disabled.
6	Reserved
5	RAC Current Skip Value (RCSV): 0 = Falling edge of internal RAC clock. 1 = Rising edge of internal RAC clock.
4	RAC Latch Skip Mode (RLSM): 0 = Skip Mode Enabled. 1 = Skip Mode Disabled.
3	RAC Skip Mode (RSM): 0 = Normal mode. 1 = Use RFSV.
2	RAC Forced Skip Value (RFSV): 0 = Falling edge of internal RAC clock. 1 = Rising edge of internal RAC clock.

Bit	Description
1:0 (cont'd)	Operation Mode: Bits[1:0] Mode 0 0 Both Channels in normal functional mode. 0 1 Reserved 1 0 Reserved 1 1 Reserved

3.12 VID – Vendor Identification Register

Address: **11h**
Default: **8086h**
Access: **R-O**
Size: **16 bits**

Identifies the manufacturer of the DMH to be Intel Corporation.

Bit	Description
15:0	This is a Vendor Identification Number (VIN) and is assigned by Intel as a 16-bit number (8086h).

3.13 RID – Revision Identification Register

Address: **12h**
Default: **0000h**
Access: **R-O**
Size: **16 bits**

Bit	Description
15:4	Reserved
3:0	Stepping: This field specifies the revision number of this component. Table only shows possible values. Not all stepping versions have actual corresponding silicon. At the time of publication, A1 appears to be the final stepping. 0000 = A0 step 0001 = A1 step

3.14 MUARS – DMH Unified Access Register Select

Address: **1Ah**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:8	Reserved
7:0	Select. Refer to Table 3-1 "Unified Access Register Definitions."

3.15 MUARD – DMH Unified Access Register Data

Address: **1Bh**
Default: **0000h**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:0	Data. Refer to Table 3-1 “Unified Access Register Definitions.”

3.15.1 DMH Unified Access Registers

The DMH provides the **MUARS** and **MUARD** registers, which allow access to information in the high-speed core. These registers are read and written through the MSIO serial interface (see Section 4.11, “Serial Interface”).

To read or write information to the high-speed core through this interface, first write the **MUARS** register SELECT field with the entry to be accessed. Then, to write data to the entry selected, write the data to the **MUARD** register. Or to read data from the entry selected, read the **MUARD** register. Some entries are read-only as indicated in Table 3-1.

Table 3-1. Unified Access Register Definitions

MUARS Select	Mode	MUARD	Description
The following selectors control attributes for Branch Channel 0 (BC0) and Branch Channel 1 (BC1) data path.			
BC0: 0H BC1: 20H	R/W	Bit[5] - Reserved. Bit[4] - Latch Delay Value Bits[3:0] - Iterations per short calibration	Strobe delay calibration control.
BC0: 1H BC1: 21H	R/W	Bits[5:0] - Encoded Delay	Bottom chunk strobe delay.
BC0: 2H BC1: 22H	R/W	Bits[5:0] - Encoded Delay	Middle chunk strobe delay.
BC0: 3H BC1: 23H	R/W	Bits[5:0] - Encoded Delay	Top chunk strobe delay.
p-type: 4H n-type: 24H	R/W	Bit[15] - Manual Calibration Start Bit[14] - Range Error Bit[13] - Reserved Bit[12] - Auto Calibration Enable Bit[11] - Reserved Bit[10] - Disable Zero Calibration Bit[9:8] - Hysteresis Control Bit[7:4] - Reserved Bit[3:0] - Scale Factor	Slew-rate calibration control register.
p-type: 5H n-type: 25H	R/W	Bits[7:0]	Process counter for slew-rate calibration.
BC0: 6H BC1: 26H	R/W	Entire Register	Clock driver calibration LUT entry 0.
BC0: 7H BC1: 27H	R/W	Entire Register	Clock driver calibration LUT entry 1.
BC0: 8H BC1: 28H	R/W	Entire Register	Clock driver calibration LUT entry 2.

Table 3-1. Unified Access Register Definitions (Continued)

MUARS Select	Mode	MUARD	Description
BC0: 9H BC1: 29H	R/W	Entire Register	Clock driver calibration LUT entry 3.
BC0: AH BC1: 2AH	R/W	Entire Register	Clock driver calibration LUT entry 4.
BC0: BH BC1: 2BH	R/W	Entire Register	DQ/DQS driver calibration LUT entry 0.
BC0: CH BC1: 2CH	R/W	Entire Register	DQ/DQS driver calibration LUT entry 1.
BC0: DH BC1: 2DH	R/W	Entire Register	DQ/DQS driver calibration LUT entry 2.
BC0: EH BC1: 2EH	R/W	Entire Register	DQ/DQS driver calibration LUT entry 3.
BC0: FH BC1: 2FH	R/W	Entire Register	DQ/DQS driver calibration LUT entry 4.
BC0: 10H BC1: 30H	R/W	Entire Register	Addr/Ctl driver calibration LUT entry 0.
BC0: 11H BC1: 31H	R/W	Entire Register	Addr/Ctl driver calibration LUT entry 1.
BC0: 12H BC1: 32H	R/W	Entire Register	Addr/Ctl driver calibration LUT entry 2.
BC0: 13H BC1: 33H	R/W	Entire Register	Addr/Ctl driver calibration LUT entry 3.
BC0: 14H BC1: 34H	R/W	Entire Register	Addr/Ctl driver calibration LUT entry 4.
BC0: 15H BC1: 35H	R/W	Entire Register	CS driver calibration LUT entry 0.
BC0: 16H BC1: 36H	R/W	Entire Register	CS driver calibration LUT entry 1.
BC0: 17H BC1: 37H	R/W	Entire Register	CS driver calibration LUT entry 2.
BC0: 18H BC1: 38H	R/W	Entire Register	CS driver calibration LUT entry 3.
BC0: 19H BC1: 39H	R/W	Entire Register	CS driver calibration LUT entry 4.
p-type: 1AH n-type: 3AH	R/W	Bits[7:0]	LUT offset.
p-type: 1BH n-type: 3BH	R/W	Bits[7:0]	Intrinsic fastest delay.
BC0: 1CH BC1: 3CH	R/W	Bit[15] - Manual Calibration Start	DIMM strobe time zone calibration control.
		Bit[14] - First-Flag	
		Bit[13] - Last-Flag	
		Bit[12:8] - Start/End Position	
		Bit[7:4] - Second Pattern	
		Bit[3:0] - First Pattern	

3.16 SPDID – SPD Device ID Register

Address: **1Ch**
Default: **000Ah**
Access: **R/W**
Size: **16 bits**

Bit	Description
15:4	Reserved
3:0	Serial Presence Detect Device ID (SPD). Refer to Section 4.11.4.5, "Changing the Default SPD Device ID."

3.17 DID – Device Identification Register

Address: **23h and 37h**
Default: **8765h**
Access: **R-O**
Size: **16 bits**

This field distinguishes the device as the DMH.

Bit	Description
15:0	The type of Memory Interface - DMH.

Functional Description 4

4.1 Operation Overview

The DMH receives commands from the SNC through the Main Channel or Main Channel Serial I/O (MSIO) bus interface. These commands are encoded as Memory Control Packets (MCPs; refer to Section 4.2, "Main Channel to Branch Channel Translation") and sent across the Main Channel. When the DMH receives an MCP, it decodes it and performs an operation. If the MCP contains a DIMM command, the DMH performs a serial-to-parallel conversion of the command contained in the MCP packet, and drives the command to the specified DIMM. For a read command, the DMH captures the data from the DIMM, performs a parallel-to-serial conversion, and then returns the data to the SNC, and pushing the data onto the top of a write FIFO. Simultaneously, the DMH then pops a write from the bottom of the write FIFO and commits it to the appropriate DIMM. The DMH controls data timing for registered DIMMs and CAS latency.

The DMH requires periodic calibration of its RAC and DDR I/Os. DIMMs also require periodic refresh cycles. The DMH provides no autonomous periodic functions. It is the responsibility of the SNC to maintain all periodic timers, and send the appropriate calibration MCPs to the DMH.

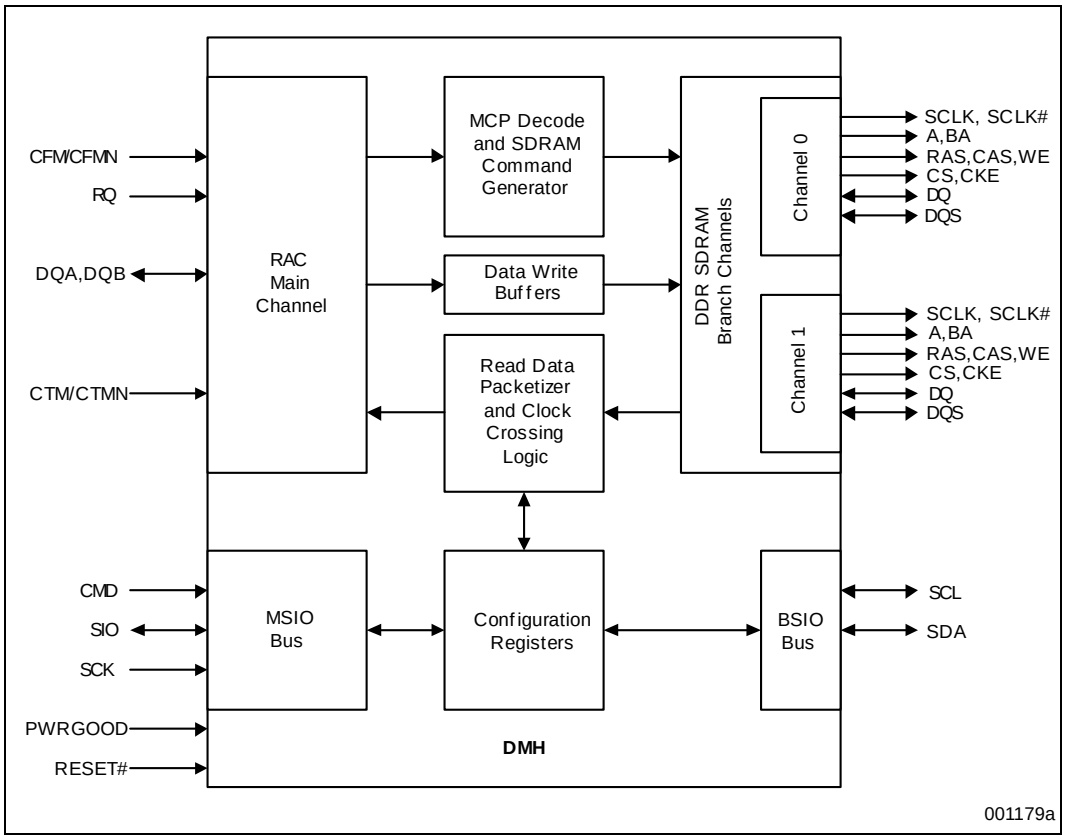
The DMH does not generate or detect data parity or ECC. However, the DMH does provide a generic 72-bit wide DDR DIMM data path. The SNC can be designed to generate and detect parity or ECC with the additional 8 bits, beyond the 64 data bits.

The DMH contains registers for configuration and control. These registers are accessed through the MSIO bus, a three-signal CMOS interface.

The DMH contains an I^2C interface that is intended for sizing DIMMs. This interface is controlled via the MSIO bus, and is functional immediately after reset deassertion. This interface conforms to the I^2C specification for a single-master with multiple-slave devices.

Figure 4-1 is a block diagram of internal logic blocks in the DMH. Refer to Chapter 2, "Signal Description" for pin descriptions.

Figure 4-1. DMH Block Diagram



4.2 Main Channel to Branch Channel Translation

The Main Channel consists of unidirectional high speed RSL control signals, and bi-directional high speed RSL data signals. The control signals are referred to as the Request Control (RQ) bus, and the data signals are referred to as the DQA/DQB bus. The RQ bus carries the MCP from the SNC to the DMH.

The SNC tunnels DDR DIMM commands and data over the Main Channel, and the DMH deterministically moves them onto the Branch Channels. The command path is one-way, with no command feedback from the DDR side. The datapath is bi-directional.

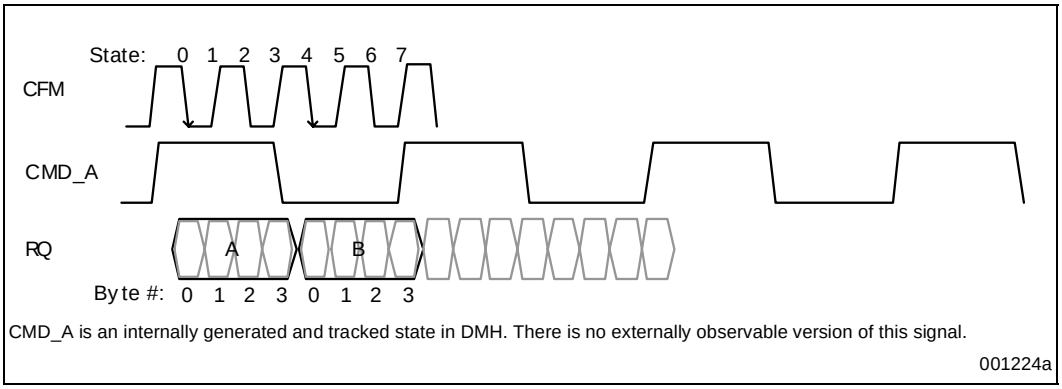
The SNC must track and emit periodic DIMM refresh cycles, short RAC current calibration cycles and RAC temperature calibration cycles. The DMH does not provide autonomous periodic calibration event handling, but instead deterministically forwards each periodic MCP command received from the SNC. The DMH embeds a Branch Channel short slew-rate calibration within its temperature calibration command. The DMH also embeds a DQS delay line calibration within its Main Channel short current calibration command. Therefore, there are no separate commands for Branch Channel short slew-rate calibration or DQS delay line calibration.

Page Open policy is somewhat constrained by the DMH write FIFO logic (refer to Section 4.8, “Memory Translation Rules”). Managing of the open pages is done by the SNC and the DMH does not track pages.

4.2.1 MCP Format and Timing

A Memory Control Packet (MCP) is generated by the SNC, and is sent over the Request Control bus (RQ[7:0]) to the DMH. An MCP is a 32-bit packet sent over two CFMs (Main Channel clocks), at double data rate as depicted in Figure 4-2. The MCP may begin in state 0 or in state 4. An MCP that begins in state 0 (MCP CMD-A) will appear on the DDR DIMM address and control lines 2.5 CFMs later. An MCP that begins in state 4 (MCP CMD-B) will appear on the DDR DIMM address and control lines 4.5 CFMs later. An MCP that begins in state 1, 2, 3, 5, 6 or 7 is illegal and will have undetermined effects.

Figure 4-2. Driving MCP to DIMM Address and Control Lines



No external MCP tracking signal is provided by the SNC. The DMH internally maintains an MCP state tracker that must be synchronized with the SNC. Upon reset deassertion, the DMH MCP state tracker is arbitrarily set. Before the SNC can send any MCP packets, it must first synchronize the DMH state tracker. Refer to Section 4.3, "DMH Time Synchronization Packet" for the details.

4.2.2 MCP Command Type Field

There are two bits (ST and SF) in the MCP which indicate the packet type. The encoding of ST and SF is shown in Table 4-1.

Table 4-1. Encoding of ST and SF

ST	SF	Operation
0	0	No Packet
0	1	Activate Command
1	0	Read/Write Command (CMD-B only)
1	1	Extended Command

4.2.3 MCP for DIMM Activate Command

A DIMM Activate Command MCP is translated into a DDR DIMM Activate packet, as defined in Jedec Standard JESD79.

4.2.4 MCP for DIMM Read/Write Command

A DIMM read/write command MCP is translated into a DDR DIMM read packet or DDR DIMM write packet, as defined in Jedec Standard JESD79. Read/write MCPs are only valid as an MCP-B packet.

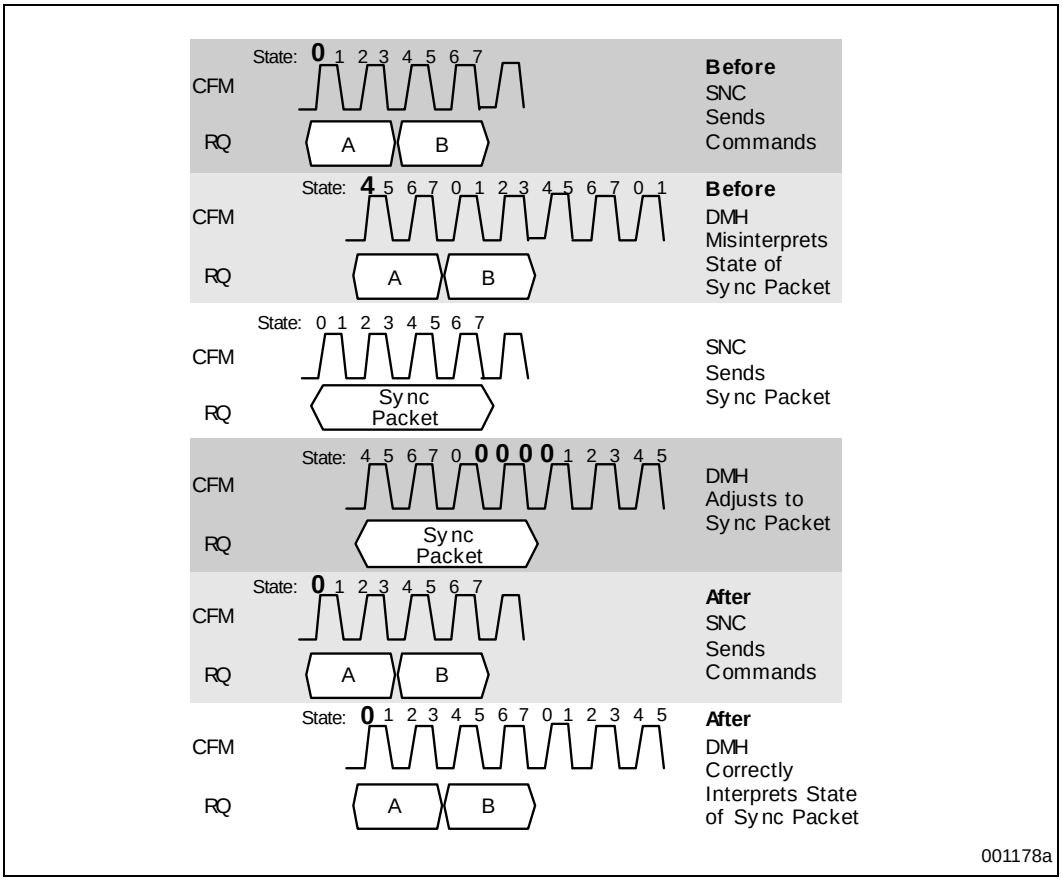
4.2.5 MCP for Extended Commands

Two categories of extended commands exist. A DIMM extended command is translated into a DDR DIMM packet, as defined in Jedec Standard JESD79. A DMH extended command is used to perform RAC calibration, and will not generate any externally observable cycles on a branch channel.

4.3 DMH Time Synchronization Packet

The DMH maintains an internal MCP state tracker that must be synchronized to the SNC after reset. The DMH state tracker could be phase shifted by 0 to 3 clocks relative to the SNC as shown in Figure 4-3 (depicted in this example shifted 2 clocks, or 4 clock edges). During the RAC initialization (see Section 4.14.1, "RAC Initialization"), the SNC sends a Time Synchronization Packet to the DMH. This causes the DMH to stall its internal clock and MCP state tracker, bringing them in sync.

Figure 4-3. Phase Shifted MCP Command State Tracker and Correction



Note: One DDR clock cycle may be stretched during this procedure if the DMH stalls its internal clock to bring its MCP state tracker into sync.

Note: Unlike MCP packets, there is no Command Type Field (ST, SF) for this packet. The DMH specifically expects to receive a time sync packet only during a certain point in RAC Initialization mode.

4.4 Main Channel Periodic Calibration

The Main Channel RAC must be calibrated on a periodic basis to prevent timing violations that could occur as a result of variations in voltage and temperature over time. Periodic current and temperature calibration will sufficiently compensate for these variations. Periodic Branch Channel calibration is embedded within the Main Channel calibration events as described in Section 4.5, "Branch Channel Periodic Calibration."

4.4.1 Current Calibration

The DMH provides a long current calibration and a periodic current calibration procedure. The long current calibration procedure is for reset initialization.

BIOS performs a long current calibration once after reset through an initialization calibration sequence that takes approximately 6 µs to complete (see Section 4.14.1, "RAC Initialization"). BIOS accesses the long current calibration controls through the RIR register (see Section 3.9, "RIR – RAC Initialization Register"). The Main Channel and Branch Channels must remain quiescent during the 6 µs calibration interval.

4.4.2 Temperature Calibration

Main Channel temperature calibration provides a mechanism to dynamically compensate the output driver slew-rate for changes in temperature. The DMH provides two methods of access to the temperature calibration procedure. One method is used for reset initialization by BIOS, the other is used for autonomous periodic calibration by the SNC.

BIOS performs a temperature calibration once after reset as part of its RAC initialization sequence (see Section 4.14.1, "RAC Initialization"). The RIR register (see Section 3.9, "RIR – RAC Initialization Register") used in this procedure provides two different methods for invoking the temperature calibration event. The RAC initialization operation (used in the procedure) performs a RAC temperature calibration within its sequence of events. Optionally, the RIR register provides a RAC temperature calibration operation as well. The Main Channel and Branch Channels should remain quiescent until the serial command completes.

Temperature calibration is also performed periodically by an autonomous timer function within the SNC. The SNC sends temperature calibration MCPs at intervals of 100 ms or less. Upon receiving the Temperature Calibrate MCP (see Section 4.2.5, "MCP for Extended Commands") from the Main Channel, the DMH initiates the RAC temperature calibration process as well as the Branch Channel slew rate calibration (see Section 4.5.1, "Slew Rate Calibration").

4.5 Branch Channel Periodic Calibration

Like the Main Channel, the Branch Channels must also be periodically calibrated to prevent timing violations that could occur as a result of variations in voltage and temperature over time. Since the minimum required frequency of periodic Branch Channel calibration events falls below the frequency for periodic calibration of the Main Channel, all periodic Branch Channel calibration events are embedded within the periodic Main Channel calibration events discussed in the previous section.

4.5.1 Slew Rate Calibration

Slew rate calibration compensates for variations in process, voltage, and temperature. The DMH provides two slew-rate calibration procedures. An extensive initialization procedure for long slew rate calibration is done once after reset. The periodic slew rate calibration is embedded within the RAC short temperature calibration event. When the DMH receives a Short Temperature Calibrate MCP (see Section 4.2.5, “MCP for Extended Commands”) from the Main Channel, the DMH performs a single short slew rate calibration procedure.

4.5.2 Read Strobe 2.2 ns Delay Calibration

As defined in Jedec Standard JESD79, the memory controller is responsible for internally delaying the data strobes (DQS) during the data phase of a DDR read transaction to center them on the data. The DMH provides two strobe delay calibration procedures.

The long strobe delay calibration procedure is done once after reset (see Section 4.14.4, “DDR Read Strobe Delay Calibration”). This procedure performs a complete initialization of the strobe delay circuits, which takes approximately 1 µs.

The periodic delay line calibration is embedded within the periodic RAC short current calibration event. When the DMH receives a Short Current Calibrate MCP (see Section 4.2.5, “MCP for Extended Commands”) from the Main Channel, the DMH initiates the current calibrate process of its RAC, and the Branch Channel Read Data 2.2 ns DQS Delay Calibration

4.6 Transfer Mode

Two parameters must be programmed to set the DMH transfer mode. The DDR DIMM burst length in each DIMM’s MRS register is programmed via the DMH DDR SDRAM initialization register (Section 3.7, “SDI – SDRAM Initialization Register”). The Main Channel burst length is set by programming the DMH data transfer size (DTS) in the Main Channel Timing register (Section 3.3, “MCTIM – Main Channel Timing Register”). DIMM burst length and Main Channel burst length must match.

4.6.1 32-Byte Mode

In this mode, each DDR SDRAM is programmed to use a burst length of 32 bytes (four transfers) across the Branch Channel. The Mode Register of each SDRAM must be programmed for a burst length of 4, and for sequential mode (as defined in the Jedec Standard JESD79). In addition, the DMH **MCTIM** register DTS field must be set to a 32-byte mode. The DMH sends and receives data across the Main Channel in bursts of 16 transfers at 2 bytes/transfer.

4.6.2 16-Byte Mode

In this mode, each DDR SDRAM is programmed to use a burst length of 16 bytes (two transfers) across the Branch Channel. Each DIMM's Mode Register must be programmed for a burst length of 2 and for sequential mode.(as defined in the Jedec Standard JESD79) In addition, the DMH **MCTIM** register DTS field must be set to a 16-byte mode. The DMH sends and receives data across the Main Channel in bursts of 8 transfers at 2 bytes/transfer.

4.7 Write Buffers

The DMH uses write buffers to decouple the Main Channel's Write Data timing from the Branch Channel Write Data timing. Without the write buffer mechanism, write-command to write-data timing would require a longer time period than read-command to read-data timing, resulting in a large turnaround time.

The DMH implements write buffering with FIFOs. The DMH maintains three independent write FIFOs for Activate for Write MCPs, Write Command MCPs, and Write Data. Read-hit logic ensures that the most recently written data is always returned on a read.

The timing between the Write Command MCP and its data phase on the Main Channel should be set (see Section 3.3, "MCTIM – Main Channel Timing Register") such that it has the same relationship as the Read Command MCP and its data phase on the Main Channel.

During PWRGOOD deassertion, or RESET# assertion, the state of all FIFO entries are asynchronously set to invalid. The DMH does not generate a Branch Channel transaction from an invalid entry popped off of a FIFO. The FIFO is 4-deep for 32-byte mode and 8-deep for 16-byte mode.

Write transactions to both Branch Channels are staged through a single set of FIFOs (Activate command, Write command, and Write data).

4.8 Memory Translation Rules

4.8.1 Read Rules

The following read rules apply:

1. Open-Page Activate for Read command must be issued to open a page before reads to the page are allowed.
2. Multiple pages may be open for reading at the same time.
3. An Activate for Read cannot be issued to a page that is currently opened due to an Activate for Write.

4.8.2 Write Rules

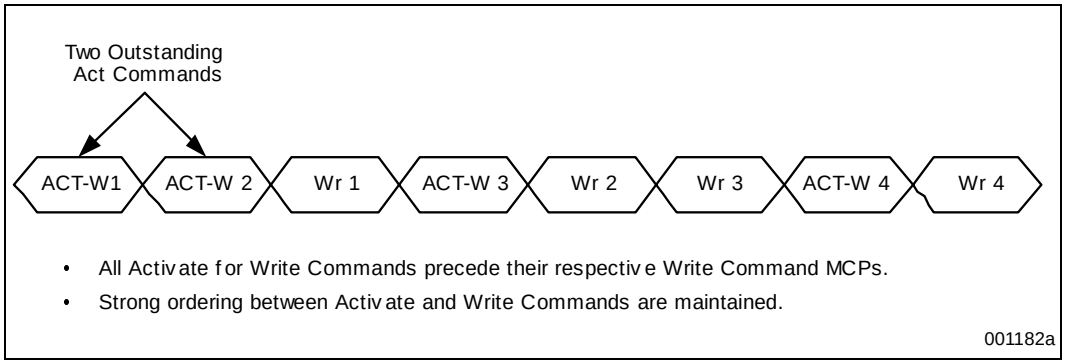
The following write rules apply:

1. Open-Page write policy is not supported.
2. An Activate for Write command must be issued to open a page before a write to the page is allowed.
3. Neither an Activate for Write nor a Write can be issued to a page that is currently open due to an Activate for Read.
4. Strict ordering of Write Command MCPs must be maintained relative to their respective Activate for Write commands.

4.8.3 Miscellaneous Rules

Write to Read turnaround time of the same memory address must be spaced a minimum of 16 CFMs apart to allow the data/address to be valid in the Write FIFO.

Figure 4-4. Example of Valid Write Command Ordering



4.8.4 Read-Hit Handling

A read-hit occurs when a Read Command MCP matches a valid write buffer. The DMH will provide the data for the read-hit from the write buffer, and will also generate the associated Branch Channel Read Command. The stale data from the Read Command is thrown away. Allowing the Branch Channel Read Command to occur prevents the DMH from masking the auto-precharge function that may be set in the Read Command.

4.8.5 Burst Operation

The DMH supports a subset of available DDR DIMM burst operations.

SNC uses DMH read-hit logic and follow the rules:

1. Writes must always be of natural alignment.
2. Read alignments shown in Table 4-2 are the only alignments supported.
3. The DMH Write buffer provides the burst operation support on a read-hit as defined in Table 4-2.

Table 4-2. Write Buffer Burst Operation for Read-Hit Operations

Burst Length	Starting Address (C2, C1, C0)	Sequential Mode
16-Byte	xx0	0,1
	xx1	Not Supported
32-Byte	x00	0,1,2,3
	x01	Not Supported
	x10	2,3,0,1
	x11	Not Supported

4.8.6 Invalid and Unsupported DIMM Transactions

The DMH does not support or prevent cycle combinations where data interruption or early termination (as defined in the Jedec Standard JESD79) would result. Further, the DMH does not prevent or support any combinations of transactions that would create bus contention (i.e. where two DIMMs would be required to drive data simultaneously onto a branch channel). Also, since the DMH does not provide the Burst Stop DDR command, it does not provide a mechanism to interrupt writes for reads. The DMH provides a precharge command, but does not support early read or write termination due to precharge. Even though it is possible to create the conditions for these events, they are invalid to the DMH.

4.9 Error Mechanisms

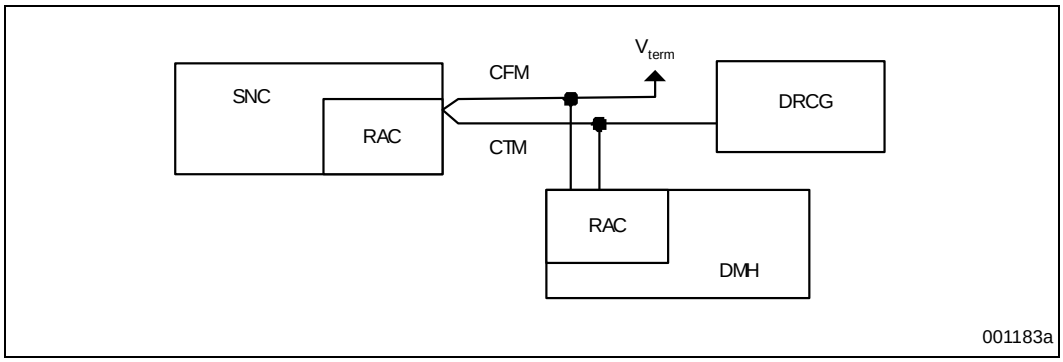
4.9.1 Support for Memory Device Failure

The error isolation and correction feature is achieved by mapping the DIMM data bits with respect to the Main Channel as used by the SNC. An SNC that can correct a single bit in each transfer can then correct any single device failure.

4.10 System Clocking

The DMH receives the 400 MHz differential RAC clock from the system's Direct RAC Clock Generator (DRCG) (refer to Figure 4-5). The core frequency of the DMH is 200 MHz, derived from the 400 MHz RAC clock. From the 200 MHz core clock, the DMH generates eight pairs of SCLK (SDRAM clocks) for the DDR DIMMs. There is a 1 MHz serial I/O clock input for the MSIO bus, which is used to generate a 100 kHz serial I/O clock on the DDR DIMM side. The 1 MHz MSIO clock must be provided at all times.

Figure 4-5. DRCG Connection Diagram



4.11 Serial Interface

4.11.1 Overview

The CMOS interface signals on the MSIO Bus are used to perform DMH initialization, DIMM Serial Presence Detect (SPD), DIMM initialization, and DMH register access.

The MSIO bus is a point-to-point interface. Using the MSIO bus, Control Transactions are communicated between the SNC and the DMH.

4.11.2 MSIO Transaction Packet Formats

A Control Transaction consists of four serial control packets as described below.

1. Main Channel Serial request, SRQ.
2. Main Channel Serial address, SA.
3. Main Channel Serial interval, SINT.
4. Main Channel Serial data, SD.

There are two kinds of control transactions. Figure 4-6 and Figure 4-7 show the layout of Register Read and Register Write control transactions. Register Read and Register Write transactions are used to access the DMH internal registers, and for DIMM SPD.

Figure 4-6. Register Read MSIO Transaction

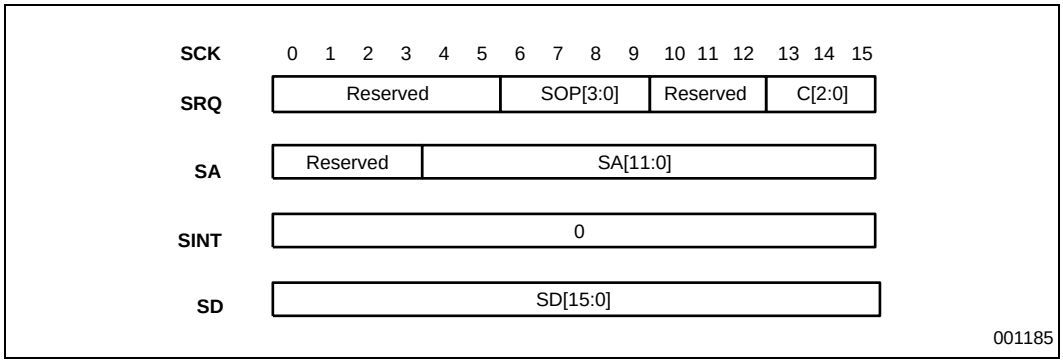


Figure 4-7. Register Write MSIO Transaction

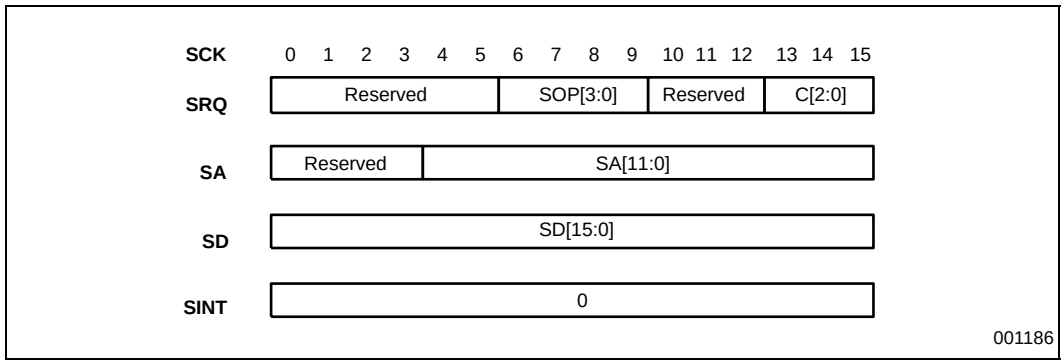


Table 4-3. MSIO Packet Field Definitions

Field	Description
SOP[3:0]	**Serial Op-code (SOP).** Specifies the MSIO operation to perform. **0000 - SRD**: Serial read of the DMH register specified in SA[11:0]. **0001 - SWR:** Serial write of the DMH register specified in SA[11:0]. **1101 - SPDW:** SPD Write Byte to SPD EEPROM. The EEPROM device is specified by C[2:0], SA[7:0], and SD[7:0] of the Write MSIO transaction. Bits C[2:0] specifies the DIMM SPD EEPROM address, SA[7:0] contains the byte address, and SD[7:0] contains data to be written to the SPD EEPROM. When the write has completed, the **WOD** bit of the **SPD** register is set to 1 by the DMH (see Section 3.10, "SPD – Serial Presence Detect Status Register"). **1110 - SPDR:** SPD Random Read the SPD EEPROM. The EEPROM device is specified by C[2:0], SA[7:0] of the Read MSIO transaction. Bits C[2:0] specifies the DIMM SPD EEPROM address, SA[7:0] contains the byte address. The data read from the EEPROM is placed in the **data** field of the **SPD** register. The **RDO** bit of the **SPD** register (see Section 3.10, "SPD – Serial Presence Detect Status Register") indicates when the data is available. All other combinations are reserved.
C[2:0]	Specifies the DIMM serial address for **SPDW** and **SPDR** commands. See Figure 4-11 and Figure 4-12 for placement in I^2C packets.
SA[11:0]	**Serial Register Address.** For **SRD** and **SWR** commands, SA[11:0] selects which control register is read or written. For **SPDW** and **SPDR** commands, SA[7:0] selects which DIMM register is read or written.
SD[15:0]	**Serial Data.** For **SRD** and **SWR** commands, the 16-bits of data read from or written to the selected control register in the DMH. For **SPDW** command, **SD[7:0]** is the data written to the DIMM register.

The following sections detail the available packet formats and the operations that can be performed on the serial control bus.

4.11.3 MSIO Bus Interface

The MSIO bus is a three-pin low-speed CMOS serial interface. SCK and CMD are input-only, and SIO is bi-directional.

SCK is driven by the SNC at up to 1 MHz.

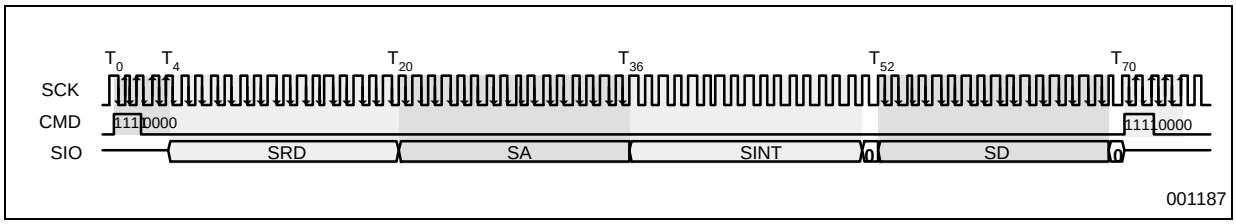
CMD is driven by the SNC, and is used to indicate the beginning of a new command, or a reset sequence. CMD is sampled on both edges of SCK by the DMH.

SIO is driven by the DMH for the SD packet of an MSIO Register Read transaction (see Figure 4-8). SIO is driven by the SNC to provide the SRD and SA packets. Additionally, for an MSIO Register Write transaction (see Figure 4-9), the SD packet is also driven by the SNC. The DMH ignores the contents of the SINT packets, and does not drive the bus during this interval.

When an MSIO Register Read transaction is performed, a turnaround clock is placed in front of (T52), and after (T69), the SD packet (see Figure 4-10). The SNC must not drive the bus during these two clocks.

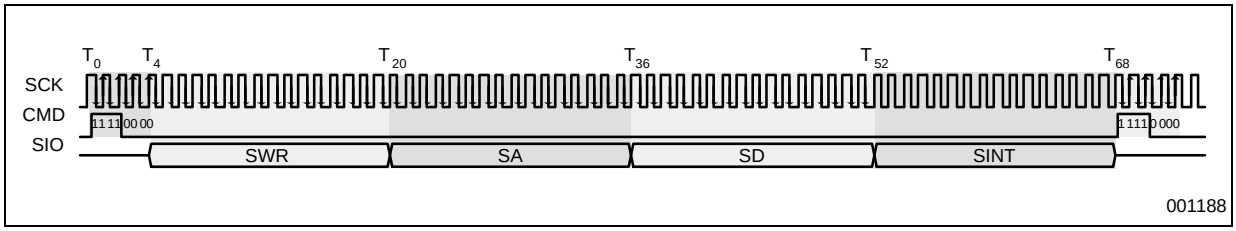
The DMH also detects a certain sequence on CMD as a serial I/O reset. Refer to Section 4.13.4, "MSIO Local Reset" for details.

Figure 4-8. MSIO Register Read Transaction



Note: The DMH samples data on clock edges indicated by arrows.

Figure 4-9. MSIO Register Write Transaction

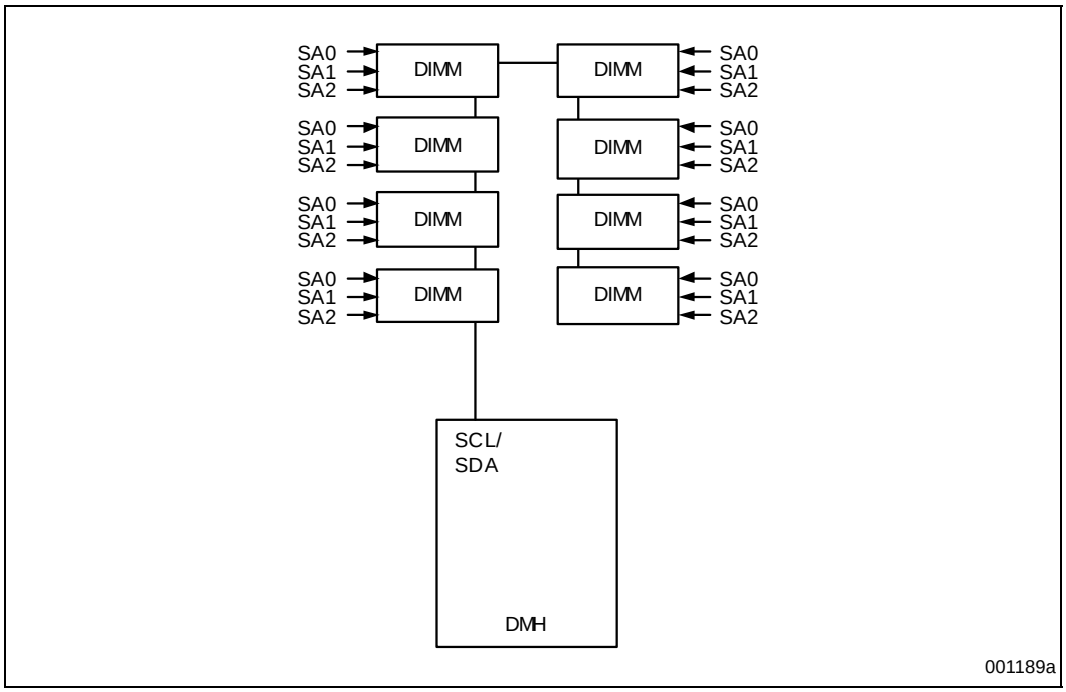


Note: The DMH samples data on clock edges indicated by arrows.

4.11.4 BSIO Bus Interface

The DMH integrates an I^2C controller to access the DIMM SPD EEPROMs. There can be a maximum of eight SPD EEPROMs associated with each I^2C bus; thus, the I^2C interfaces are wired as indicated in Figure 4-10.

Figure 4-10. Connection of DIMM Serial I/O Signals



4.11.4.1 BSIO Asynchronous Handshake

The I^2C interface is a non-deterministic, asynchronous interface. Once software issues an SPD command (MSIO SPDW or SPDR**)**, software is responsible for verifying command completion before another SPD command can be issued. Software can determine the status of an SPD command by observing the **SPD** register.

An SPD command has completed when any one command completion field (RDO, WOD, BBE) of the **SPD** register (see Section 3.10, “SPD – Serial Presence Detect Status Register”) is observed set to 1. An SPDR command has successfully completed when the RDO field is observed set to 1. An SPDW command has successfully completed when the WOD field is observed set to 1. An unsuccessful command termination causes the BBE field to be set to 1. The DMH will clear the **SPD** register command completion fields automatically whenever an SPDR or SPDW command is initiated. An application may begin polling the register immediately after initiating an SPD command.

Software can determine when an SPD command is being performed by observing the BUSY field of the **SPD** register. When this bit is observed set to 1, the interface is busy performing a command.

The Register Read MSIO transaction initiates the SPDR operation and will not directly receive the SPD data in its SD packet field. The SPDR operation must be tunneled across the much slower BSIO interface, and will not return data on time for transfer to the SD packet field of the initiating Register Read MSIO transaction. Instead, valid SPD data is stored in the DATA field of the **SPD** register upon successful completion of the SPDR operation (indicated by 1 in the RDO field of the **SPD** register).

Unsuccessful command termination can be caused by one of two conditions. The first condition occurs when an EEPROM does not acknowledge a packet at any of the required ACK points. The second condition occurs when an EEPROM throttles the serial clock for more than 25 ms. These conditions generate the same end result (BBE field set to 1).

4.11.4.2 Clock Divider

The SPD register contains a clock divider field (DIV). Table 4-4 provides the available SCL frequency settings, assuming SCK = 1 MHz.

Table 4-4. SCK Clock Divider Frequency Table

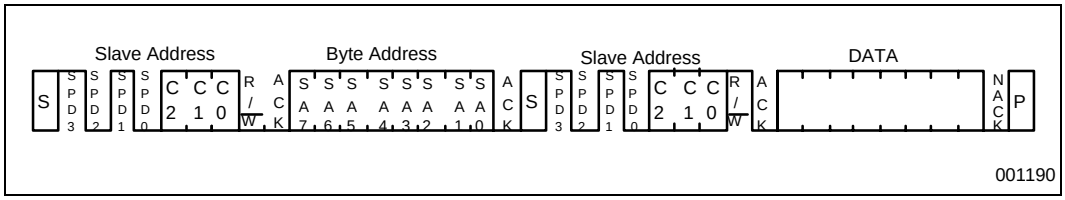
DIV	SCL Frequency	Frequency Scaler
0	100 KHz	10
1	38.5 KHz	26
2	23.9 KHz	42
3	17.2 KHz	58
4	13.5 KHz	74
5	11.1 KHz	90
6	9.4 KHz	106
7	8.2 KHz	122
8	7.3 KHz	138
9	6.5 KHz	154
10	5.9 KHz	170
11	5.4 KHz	186
12	5 KHz	202
13	4.6 KHz	218
14	4.3 KHz	234
15	4 KHz	250

4.11.4.3 BSIO Request Packet for SPD Random Read

The MSIO transaction packet format for the SPD EEPROM Random Read command is shown in Figure 4-11. C[2:0] of the MSIO SRQ packet provides the I^{2}C Slave Address, while SA[7:0] field of the MSIO SA packet selects the I^{2}C Byte Address. Note that the MSIO SD packet is unused for this purpose.

Upon receiving the MSIO SPDR command, the DMH generates the Random Read Register I^{2}C command sequence on the BSIO interface. The returned data is then stored in the DMH SPD register in bits [7:0], and the RDO field is set to 1 by the DMH to indicate that the data is present and that the command has completed without error (see Section 3.10, “SPD – Serial Presence Detect Status Register”).

Figure 4-11. Random Byte Read Timing

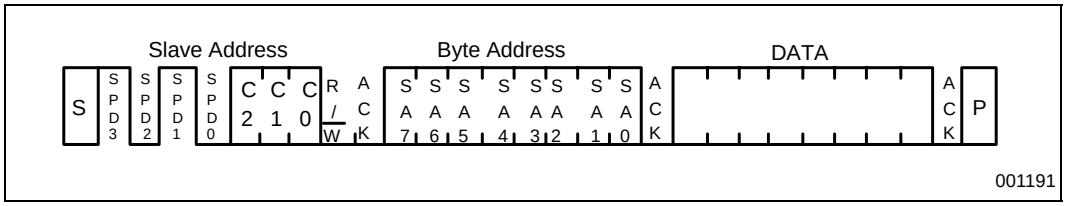


4.11.4.4 BSIO Request Packet for SPD Byte Write

The MSIO transaction packet format for the SPD EEPROM Byte Write command is shown in Figure 4-12. C[2:0] of the MSIO SRQ packet provides the I^{2}C Slave Address, while the SA[7:0] field of the MSIO SA packet selects the I^{2}C Byte Address. The Write Data is passed in the SD[7:0] field of the MSIO SD packet.

Upon receiving the MSIO SPDW command, the DMH generates the Byte Write Register I2C command sequence on the BSIO interface as shown in Figure 4-12. The DMH indicates that the BSIO command has completed by setting the WOD bit of the DMH **SPD** register to 1 (see Section 3.10, "SPD – Serial Presence Detect Status Register").

Figure 4-12. Byte Write Register Timing



4.11.4.5 Changing the Default SPD Device ID

In Figure 4-11 and Figure 4-12, the SPD device ID is represented by the SPD[3:0] bit fields. After reset, the default SPD device ID is 0AH (DIMM device type). The DMH provides a mechanism to change the device ID.

To change the device ID, software programs the **SPDID** register with a new SPD device ID while the BSIO interface is quiescent. Then, software performs one BSIO Read command to any SPD address (it is not necessary for a device to respond to the address) to load the new device ID. This first transaction will have an invalid Device ID, and its returned data and completion status must be ignored. Afterwards, software may perform any supported BSIO commands, and the newly loaded device ID will be used.

4.11.4.6 I2C Protocols

Refer to the I2C Bus Specification for standard timing protocols. The DMH supports the following I2C protocols:

- Random Byte Read
- Byte Write

4.11.4.7 I2C Bus Timeout

If there is an error in the transaction such that the SPD EEPROM does not signal an acknowledge, or holds SCK longer than the allowed time-out period of 25 ms, the transaction will time out. The DMH will discard the cycle and set the BBE bit of the DMH **SPD** register to 1 to indicate this error (see Section 3.10, "SPD – Serial Presence Detect Status Register"). The timeout counter within the DMH begins counting after the last bit of data is transferred to the DIMM and the DMH is waiting for a response.

4.12 DDR SDRAM Transactions

4.12.1 DIMM Initialization

DIMM initialization is done by BIOS through the serial interface. The **SDI** register (see Section 3.7, "SDI – SDRAM Initialization Register"), accessible through the MSIO interface, is used by BIOS to cause specific initialization sequences to be sent to the DIMMs over the DIMM command lines. Table 4-5 shows the SDRAM command encoding for the respective SDRAM commands available through the SDI register.

Table 4-5. DDR SDRAM Command Encoding for SDI Register

Function	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	Address
NOP[a]	H	H	H	X	X	X	X
NOP[b]	H	H	L	H	H	H	X
(Extended) Mode Register Set	H	H	L	L	L	L	Opcode
Precharge all Banks	H	H	L	L	H	L	PA = H
Precharge Single Bank	H	H	L	L	H	L	PA = L, BA = Bank Address
NOP for Self-refresh	L	L	X	X	X	X	X
Auto Refresh	H	H	L	L	L	H	X

a. This NOP is used when the selected DIMM Chip Select CS[2:0] is not asserted at the time of this command.
b. This NOP is used when the selected DIMM Chip Select CS[2:0] is asserted at the time of this command.

NOTES:
1. X = Don't care, H = Logic high, L = Logic low.
2. PA = Precharge All (CA_{10}).
3. Opcode = Extended Mode Register Operation on A_0-A_{14},BA_0-BA_1.
4. BA = Bank Address (BA_0-BA_1).

4.13 Reset

4.13.1 Power Good Sequence

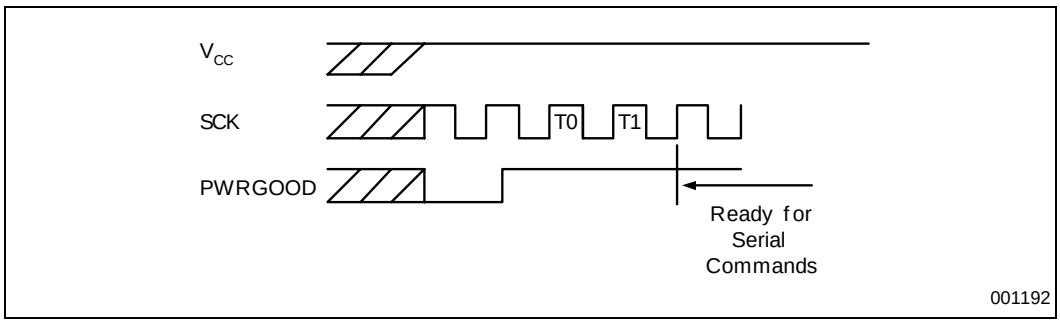
The assertion of PWRGOOD indicates that all voltage supplies are stable and within their operating specifications. During deassertion of the PWRGOOD signal, the DMH will asynchronously set all I/O pins to the state indicated in Table 2-1, Table 2-2, and Table 2-3, and reset all internal logic and all registers.

Upon the assertion of PWRGOOD, the DMH requires two serial clocks (SCK) to complete its reset sequence. After this period of time has elapsed, and after the DMH is receiving a clean and stable Main Channel clock (CFM/CTM), software may proceed to bring the high-speed core out of reset and initialize it by following the procedures outlined in Section 4.14, "Initialization."

When bringing the DMH out of PWRGOOD reset, the CMD and SIO signals must be quiescent, and SCK must be provided by one of two appropriate methods.

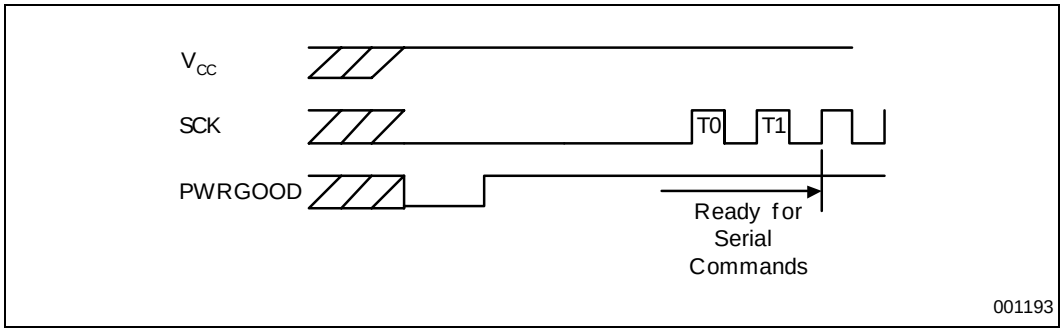
The first method (Figure 4-13) is used when SCK begins before PWRGOOD assertion. In this scenario, the quality of SCK while PWRGOOD is deasserted is not important. Once PWRGOOD is asserted, SCK must be stable.

Figure 4-13. PWRGOOD Sequence Method 1



The second method (Figure 4-14) is used when SCK begins after PWRGOOD assertion. In this scenario, SCK must begin with a clean and complete cycle.

Figure 4-14. PWRGOOD Sequence Method 2



4.13.2 Hard Reset

Upon the deassertion of the RESET# signal, the DMH will asynchronously reset all internal logic except for programmable registers, calibration registers, and the serial interface. Write buffers are invalidated by hard reset. SNC guarantees that all memory pages have been closed and data flushed prior to hard reset. The DMH requires a sufficient number of quiescent clock cycles on the Main Channel to allow any pending memory commands to complete prior to hard reset.

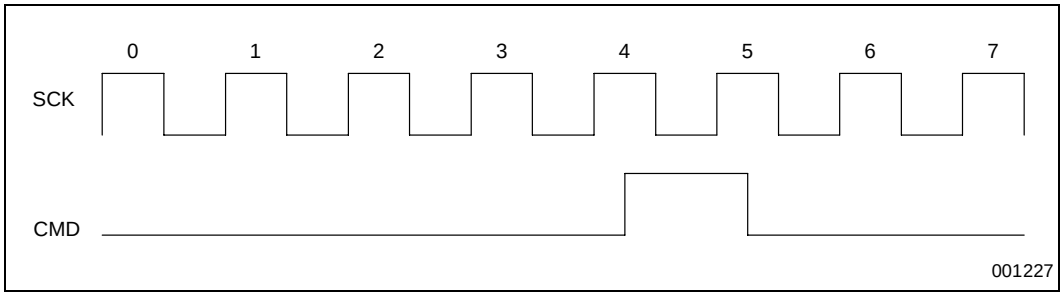
4.13.3 Local Reset

The MSIO interface can be locally reset. MSIO reset will reset the MSIO and BSIO interfaces to an initial state.

4.13.4 MSIO Local Reset

BIOS can reset the DMH through the MSIO serial interface by issuing an SIO reset sequence as shown in Figure 4-15. CMD is sampled on both the rising and falling edges of SCK. A 1-1-0-0 sequence on CMD resets the state machines controlling the MSIO pins. Programmable registers in the DMH are not affected by this reset.

Figure 4-15. SIO Reset Sequence



4.14 Initialization

After the Power Good sequence (Section 4.13.1, “Power Good Sequence”) has occurred, the DMH is in the powered-down idle state, i.e. the serial interface is active, while the rest of the DMH is held in reset. Branch Channel clocks are stopped and Branch Channel Clock Enables are deasserted. All Main Channel I/Os are indeterminate and may be driving the bus until the RAC reset sequence is completed.

The DMH core is programmatically sequenced out of reset and initialized by BIOS. Before BIOS begins the process of initializing the DMH, all DMH inputs must be stable and the Main Channel and MSIO clocks must be running.

DMH behaves deterministically at the end of the reset and initialization sequence.

4.14.1 RAC Initialization

RAC initialization is performed by BIOS after power up of the DMH. This involves using the MSIO serial interface to send a sequence of RAC initialization steps to the DMH to power up the DMH’s core. BIOS completes RAC initialization by synchronizing the SNC and DMH main channels.

Upon completion of the RAC initialization procedure, the DMH is in the powered up idle state, i.e. the DMH provides stable DIMM clocks and drives a NOP command state on each branch channel, DIMM Clock Enable (CKE) on each branch channel is asserted, and the DMH main channel will be synchronized and ready to accept commands.

4.14.2 DDR DIMM Sizing

DIMM Sizing is performed by using the BSIO interface to interrogate the DIMM SPD logic to determine DIMM population and characteristics.

1. Size the DMH for DIMMs by using the MSIO SPDR command (see Section 4.11.2, “MSIO Transaction Packet Formats”) to generate BSIO transactions, reading all SPD EEPROM read-only registers, and processing the information (See Section 4.11.4, “BSIO Bus Interface”).

4.14.3 DDR DIMM Initialization

Branch channel initialization must be performed after power-up and RAC initialization of the DMH. BIOS will use the MSIO bus (see Section 4.11, “Serial Interface”) to send a sequence of Branch Channel initialization steps to the DMH.

1. For each DIMM, issue **SDI** register commands (see Section 3.7, “SDI – SDRAM Initialization Register”) for precharge, mode register set, and auto refresh, as necessary to perform the manufacturer’s DIMM power-up sequence (see Jedec Standard JESD79 and also manufacturers requirements for specific DIMMs).
2. Program the DIMM MRS registers for correct CAS latency and burst size using the SDI Mode Register Set command (see Section 3.7, “SDI – SDRAM Initialization Register”). Program the corresponding DIMM CAS latency field of the **BCTIM** register (see Section 3.4, “BCTIM – Branch Channel Timing Register”) to match the DIMM CAS latency. Program the DTS field of the **MCTIM** register (Section 3.3, “MCTIM – Main Channel Timing Register”) burst side to match the SNC burst size. Also program the **DGR** register (Section 3.5, “DGR – DIMM Geometry Register”) with the geometry of the DIMMs as determined by sizing the DIMMs through SPD.

4.14.4 DDR Read Strobe Delay Calibration

This procedure adjusts the DIMM read strobe delay to 2.2 ns as specified in Jedec Standard JESD79.

Program the **SDI** register to perform a DDR Delay Line Calibration command by writing 81H to the **SDI** register. Poll the **SDI** register until the ISO field is reset to 0 by the DMH. This calibrates the strobes to be centered on data on DIMM read commands.

4.14.5 DDR DIMM Path Delay Calibration

Data (DQ) from memory is captured by the DMH using a source-synchronous clock (DQS) supplied by the DIMMs. The JEDEC DDR DIMM standard requires DQS to be tristated while the Branch Channel is in a quiescent state. This causes the DQ/DQS signals to float to the termination voltage, and causes glitches on the DQ/DQS capture registers. Without special capture logic, these glitches would leave the DMH in a non-functional state.

The DMH implements capture-window logic that turns on the DQ/DQS receivers only during the data-phase of a Branch Channel Read transaction. While the capture-window is disabled, the DMH ignores any events occurring on the DQ/DQS signals. In this way, the DMH isolates itself from induced noise on the DQ/DQS lines during the quiescent intervals.

The capture-window occurs relative to the Read command, and during a time-interval that is a function of DIMM Path Latency, DIMM CAS latency, and the DIMM registered delay. DIMM CAS latency is obtained from the DIMM SPD ROM. A DIMM registered delay must always be 1 DIMM clock for the DMH.

For each DIMM side, BIOS must determine and program the t_{DPL} (Section 3.4, “BCTIM – Branch Channel Timing Register”) and t_{DSDn} (Section 3.2, “DSTIM – DIMM Strobe Timing Register”) register values. The DMH provides an assist circuit to assist BIOS in ascertaining these values.

Electrical Specifications 5

5.1 Non-Operational Maximum Rating

The absolute maximum non-operational DC ratings are provided in Table 5-1. Functional operation at the absolute maximum and minimum ratings is neither implied nor guaranteed. The DMH should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and operational DC tables. Furthermore, although the DMH contains protective circuitry to resist damage from static discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 5-1. Absolute Maximum Non-Operational DC Ratings at the Package Pin

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	DMH Storage Temperature	–10	45	°C	
Vcc (All)	DMH Supply Voltage with Respect to Vss	–0.50	Operating voltage +0.50	V	
Vcc (CMOS)	CMOS Buffer DC Input Voltage with Respect to Vss	–0.50	Vcc (CMOS) +0.50	V	

5.2 Operation Power Delivery Specification

All parameters in Table 5-2 are specified at the pin of the package.

Table 5-2. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VCCRAC	DMH-core, and RAC I/O Supply	1.71	1.8	1.89	V	
VCCRAC-Icc	VCCRAC Supply Current			400	mA	
VCCRAC-dIccA/dt	Transient Current Slew Rate			0.25	A/ns	
VCC25	DDR I/O Interface	2.30	2.50	2.70	V	
VCC25-Icc	DDR I/O Interface Supply Current			1.0	A	
VCC25-dIccA/dt	DDR I/O Interface Transient Current Slew Rate			4	A/ns	

5.3 Main Channel Interface

Table 5-3. DMH Main Channel Signal Groups

Signal Group	Signal
RSL I/O Pins	DQA[8:0], DQB[8:0]
RSL Input Pins	RQ[7:0]
RSL Input Pins	CFM, CFMN (differential clock); CTM, CTMN (differential clock)
CMOS 1.8 Inputs Pins[a]	SCK, CMD, PWRGOOD
CMOS 1.8 I/O Pins[a]	SIO
Power/Other	VCCRAC, VCCRACA[b], VREF{A,B} RAC[c], VSS

a. See Table 5-7 for “CMOS 1.8” specification.
b. VCCRACA is the analog voltage input to DMH RAC. This is equal to the DMH core voltage and is generated via a filter network.
c. See Table 5-4 for Vref specification.

5.3.1 Main Channel Interface Reference Voltage Specification

Table 5-4. Main Channel Vref Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
Vref,r	Main Channel Reference Voltage	1.25	1.40	1.53	V	a

a. Vref is generated from 1.8V voltage (VCCRAC on the DMH).

5.3.2 DC Specifications

Table 5-5. RSL Data Group, DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Vil	Input Low Voltage	Vref, r –0.5	Vref, r –0.175	V	c
Vih	Input High Voltage	Vref, r +0.175	Vref, r +0.5	V	c
V_{DIS}	Data Voltage Swing	0.54	1.10	V	
A_{DI}	Data Input Asymmetry about V_{REF}	–15%	15%	V_{DIS}	
Iol	Output Low Current		30	mA	d
Ili	Input Leakage Current		5	µA	
Ilo	Output Leakage Current		5	µA	

a. All specifications are at the pin of the package.
b. Applies to RSL input, output and I/O buffers.
c. Vref here refers to “Typical” value of the main channel reference voltage. See Table 5-4 for Vref specification.
d. Current per I/O.

Table 5-6. RSL Clocks, DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
$V_{CIS,CTM}$	Clock Input Voltage Swing on CTM Pin	0.25	–	V/ns	
$V_{CIS,CFM}$	Clock Input Voltage Swing on CFM Pin	0.25	–	V/ns	
V_X	Clock Differential Crossing-point Voltage	1.30	1.80	V	
V_{CM}	Clock Input Common-Mode Voltage	1.40	1.70	V	

a. VCIS applies to both Clock and Clock#.
b. Parameters apply to RSL input, output, and I/O buffers.

Table 5-7. Main Channel "CMOS 1.8 I/O" DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Vil	Input Low Voltage	–0.3	1/2 (VCCRIO) –0.25	V	c
Vih	Input High Voltage	1/2 (VCCRIO) +0.25	VCCRAC +0.30	V	c
Ili	Input Leakage Current		20	µA	
Ilo	Output Leakage Current		20	µA	

a. All specifications are at the pin of the package.
b. Parameters apply to "CMOS 1.8" input, output, and I/O buffers.
c. VCCRIO is the VCC I/O as specified in *Intel® E8870 Scalable Node Controller (SNC) Datasheet.*

5.3.3 AC Specifications

For complete RAMBUS data sheet, including the AC specifications, timing relationships, etc., please refer to the RAMBUS website.

5.4 DDR Interface

5.4.1 Signal Group

Table 5-8 summarizes DMH DDR interface signals.

Table 5-8. DMH DDR Signal Groups

Signal Group	Signal
SSTL_2 Outputs	BC0CS[7:0]#, BC1CS[7:0], BC0RAS#, BC1RAS#, BC0CAS#, BC1CAS#, BC0WE#, BC1WE#, BC0A[14:0], BC1A[14:0], BC0BA[1:0], BC1BA[1:0], BC0CKE, BC1CKE, BC0SCLK[3:0], BC0SCLK[3:0]#, BC1SCLK[3:0], BC1SCLK[3:0]#
SSTL_2 I/O	BC0DQ[71:0], BC1DQ[71:0], BC0DQS#[17:0], BC1DQS#[17:0], SREFFB, SREF, BC{0,1}SRCAL[a]
CMOS2.5 Outputs OD[b]	SCL, SDA
Power/Other	AD{0,1}VREF, BC0VREF{A,B,C,D,E,F}[c], BC1VREF{A,B,C,D,E,F}, VCC25[d], VCCRAC[e], VCCDLY[f], VSS

a. Branch Channel 0 and 1 slew rate calibration inputs. Connect BC0SRCAL is pulled down to GND, and BC1SRCAL is pulled up to 2.5V, through a 50-ohm 1% resistor.
b. See Table 5-17 and Table 5-20 for CMOS 2.5 specifications.
c. See Table 5-9for Vref specification.
d. VCC25 is supply voltage to DDR-I/O buffer.
e. VCCRAC is supply voltage to main channel I/O and DMH core.
f. VCCDLY is the power to the delay cells. It is generated via a filter network.

5.4.2 DDR Reference Voltage Requirements

Table 5-9. DMH DDR Vref Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Vref, d	SSTL-2 Reference Voltage	(VCC25)/2 –0.025	(VCC25)/2	(VCC25)/2 +0.025	V	a, b
Vtt	SSTL-2 Termination Voltage	Vref –0.04	Vref	Vref +0.04	V	a, c

a. Vref = (VCC25)/2.
b. Vref noise of ±25 mV.
c. Vtt is the supply voltage that SSTL-2 signals are terminated to. This supply is not provided to the DMH.

5.4.3 DC Specifications

Table 5-10. SSTL_2 DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Vil	Input Low Voltage	–0.30	Vref, d –0.10	V	
Vih	Input High Voltage	Vref, d +0.10	(VCC25) +0.30	V	
Vol	Output Low Voltage		Vtt –0.52	V	b, c
Voh	Output High Voltage	Vtt +0.52		V	b, c
Iol	Output Low Current		16.4	mA	b, c
Ioh	Output High Current	–15.4		mA	b, c

a. All specifications are at the pin of the package.
b. The parameters also applies to Input, output and I/O buffers.
c. Under tester load of 50 ohms pulled up to 1.25V.

5.4.4 AC Specifications

Table 5-11. SSTL_2 Common Clock AC Specification

Symbol	Parameter	Min	Max	Unit	Figure	Notes
Tacck	Address and Control Valid before Clock	1.7		ns	5-1	
Tckac	Address and Control Valid after Clock	6.7		ns	5-1	
Thp	Common Clock Half Period	4.4		ns	5-1	
Tp	Common Clock Period	9.6	10.4	ns	5-1	
Tdqsck	Strobe Valid Delay from Common Clock	–75	120	ps	5-1	a

a. Specified by design characterization.

Table 5-12. SSTL_2 Source Synchronous AC Specification

Symbol	Parameter	Min	Max	Unit	Figure	Notes
Tvb	Data to Valid Before the Strobe	1.50		ns	5-2	
Tva	Data to Valid After the Strobe	1.50		ns	5-2	
Tds	Data to Strobe Setup Time	–1.65		ns	5-2	a, b
Tdh	Data to Strobe Hold Time	3.14		ns	5-2	b
Tsl (i)	Input Slew Rate	0.50		V/ns		a
Tsl (o)	Output Slew Rate	1.80	4.5	V/ns		
Tslmr	Output Slew Rate Matching Ratio	0.67	1.50			c

a. The following derating is required for inputs with slew rate below 0.5 V/ns.
   0.5 V/ns, no derating
   0.4 V/ns, + 50 ps
   0.3 V/ns, +100 ps
b. Specification is at the package pin.
c. The ratio of the rising slew rate to the falling slew rate is specified for the same temperature and voltage over the entire temperature and voltage range.

Table 5-13. SSTL_2 Output Clock Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
Tcl	Output Clock Low Time	0.45	0.55	ns	
Tch	Output Clock High Time	0.45	0.55	ns	

a. All specifications are at the pin of the package.
b. The parameters also apply to BC0SCLK[3:0] and BC1SCLK[3:0].

5.4.4.1 AC Waveforms

Figure 5-1. SSTL-2 Common Clock AC Timing

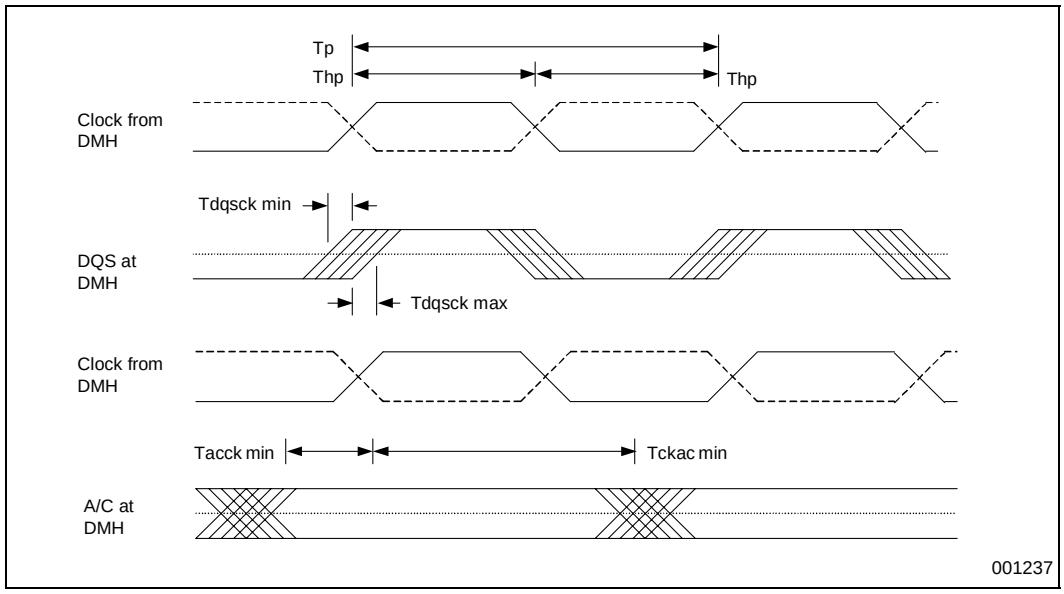
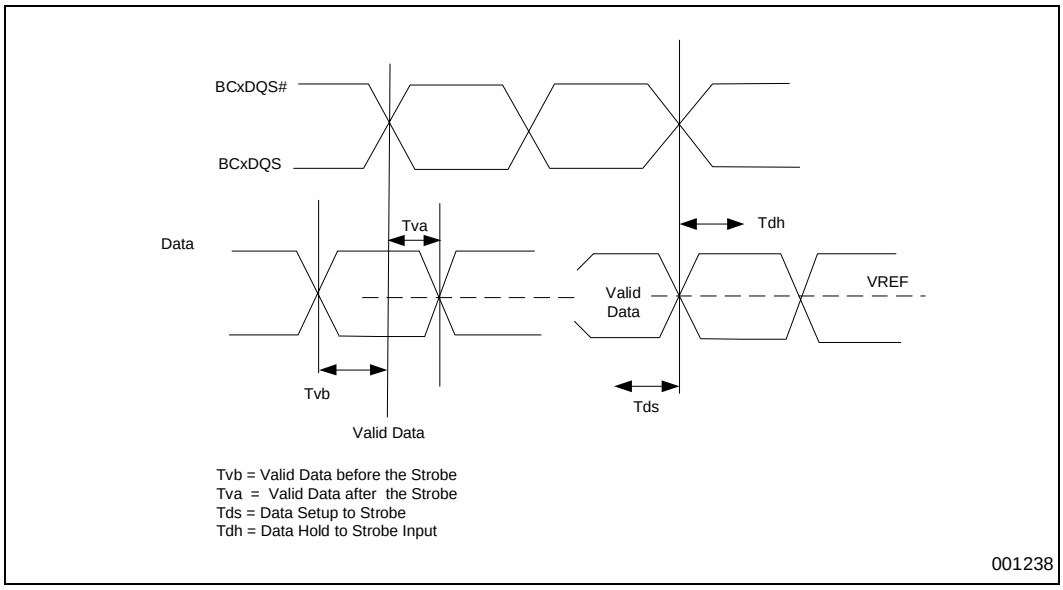


Figure 5-2. SSTL-2 Source Synchronous AC Timing



5.5 Miscellaneous Signals Interface

All buffer types that do not belong to one of the major buses in the system are listed as miscellaneous signals.

5.5.1 Signal Groups

Table 5-14. Signal Groups

Signal Group	Signal
CMOS1.8 Input	RESET#, PWRGOOD, XORIN
CMOS 1.8 Output	XOROUT
CMOS2.5 I/O[a]	SDA, SCL, TSO[b]

a. Requires external 1.5K ohm pull-up resistor.
b. This is an input only signal.

5.5.2 DC Characteristics

Table 5-15. CMOS 1.8V Input DC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	Input High Voltage	1.25	2.3	V	
V_{IL}	Input Low Voltage	–0.3	0.75	V	
V_{OH}	Output High Voltage	1.4		V	

Table 5-15. CMOS 1.8V Input DC Parameters (Continued)[a]

Symbol	Parameter	Min	Max	Unit	Notes
V_{OL}	Output Low Voltage		0.3	V	
I_{li}	Input Leakage Current	–10	10	µA	

a. Specified by design characterization.

Table 5-16. CMOS 1.8V Output DC Parameters [a, b]

Symbol	Parameter	Min	Max	Unit	Notes
V_{oH}	Output High Voltage	1.50		V	
V_{oL}	Output Low Voltage		0.20	V	
Ron	Output Impedance, Pull-Down	20	40	Ohms	
Ron	Output Impedance, Pull-Up	24	40	Ohms	
I_{li}	Input Leakage current	–500	500	µA	

a. Specified by design characterization.
b. Supply voltage at 1.5V ±5% tolerance.

Table 5-17. CMOS 2.5V DC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	Input High Voltage	0.7*(VCC25)	(VCC25 max) +0.5	V	
V_{IL}	Input Low Voltage	–0.5	0.3* (VCC25)	V	
V_{OH}	Output High Voltage[b]	VCC25 max	VCC25 max	V	
V_{OL}	Output Low Voltage		0.40	V	
I_{li}	Input Leakage Current	–10	10	µA	

a. Specified by design characterization.
b. Open Drain. $V_{OH,min}$ = pull-up voltage.

5.5.3 AC Specification

Table 5-18. CMOS 1.8V Input AC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
Ts1	CMD Setup Time to SCK Rising or Falling Edge	2.5		ns	
Th1	CMD Hold Time to SCK Rising or Falling Edge	2.5		ns	
Vih	Input High Voltage		VCCRAC +0.7	V	b
Vil	Input Low Voltage	–0.5		V	b
Tq1	SCK (neg) -to-SIO Delay		15	ns	c
Thr	SCK (pos) -to-SIO Delay	5		ns	d

a. Specified by design characterization.
b. Overshoot/undershoot duration less than 5 ns.
c. @CLOAD, max = 20pf (SD read data valid).
d. @CLOAD, max = 20pf (SD read data hold).

Table 5-19. CMOS 1.8V Output AC Parameters [a]

Symbol	Parameter	Min	Max	Unit	Notes
Tco	Clock to Output Valid Delay	0.5	2.5	ns	
Tsu	Input Setup Time	N/A		ns	
Thold	Input Hold Time	N/A		ns	
SRf	Output Slew Rate Fall	1	3	V/ns	
SRr	Output Slew Rate Rise	1	3	V/ns	

a. Specified by design characterization.

Table 5-20. CMOS 2.5V AC Parameters [a, b, c]

Symbol	Parameter	Min	Max	Unit	Notes
fSCL	SCL Clock Frequency		100	kHz	
tlow	Low Period of the SCL Clock	4.7		us	
thigh	High Period of the SCL Clock	4.0		us	
Thd	Data Hold Time		3.45	us	
Tsu	Data Setup Time	250		ns	
tr	Rise Time of SDA and SCL		1000	ns	
tf	Fall Time of SDA and SCL		300	ns	
Cb	Capacitive Load for each Bus Line		250	pf	

a. Specified by design characterization.
b. Supply voltage at 1.5V ±5% tolerance.
c. Clock delay is in reference to the 200 MHz clock.

Ballout and Package Information 6

Section 6.1 described the package used by DMH. Table 6-1 list the pins in alphabetical ballout number. Table 6-2 list the ballout numbers in alphabetical pin order.

6.1 567-Ball OLGA1 Package Information

The 567-ball OLGA1 package has an exposed die mounted on a package substrate. The package's coplanarity is controlled to a maximum of 8 mil. A heatsink, with appropriate interface material and retention capabilities, is required for proper operation.

Figure 6-1. 567-Ball (DMH) OLGA1 Package Dimensions – Top View

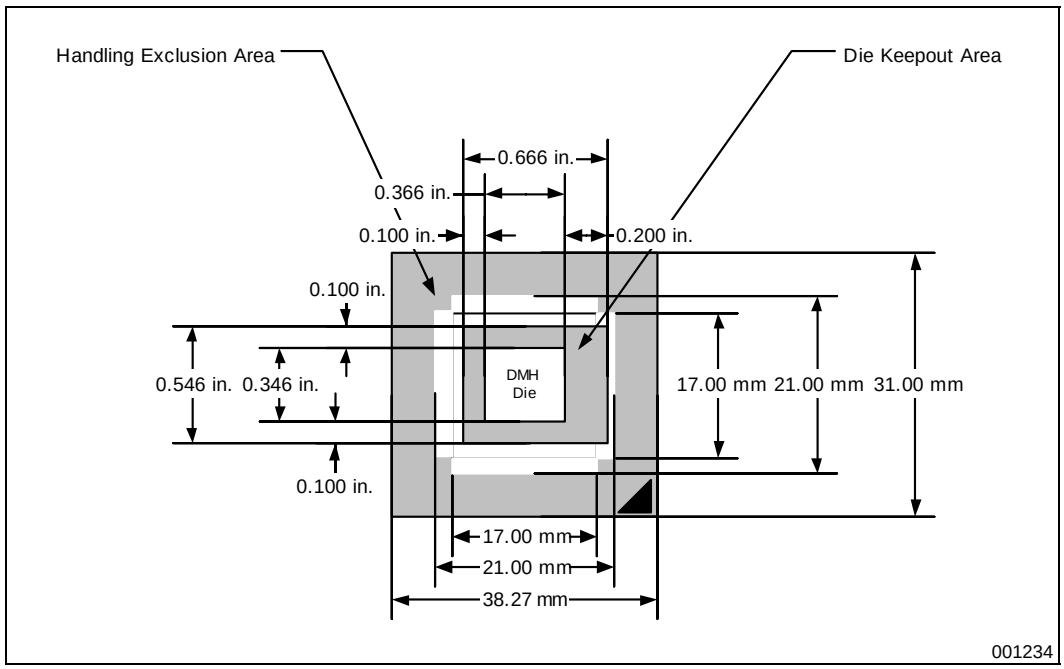
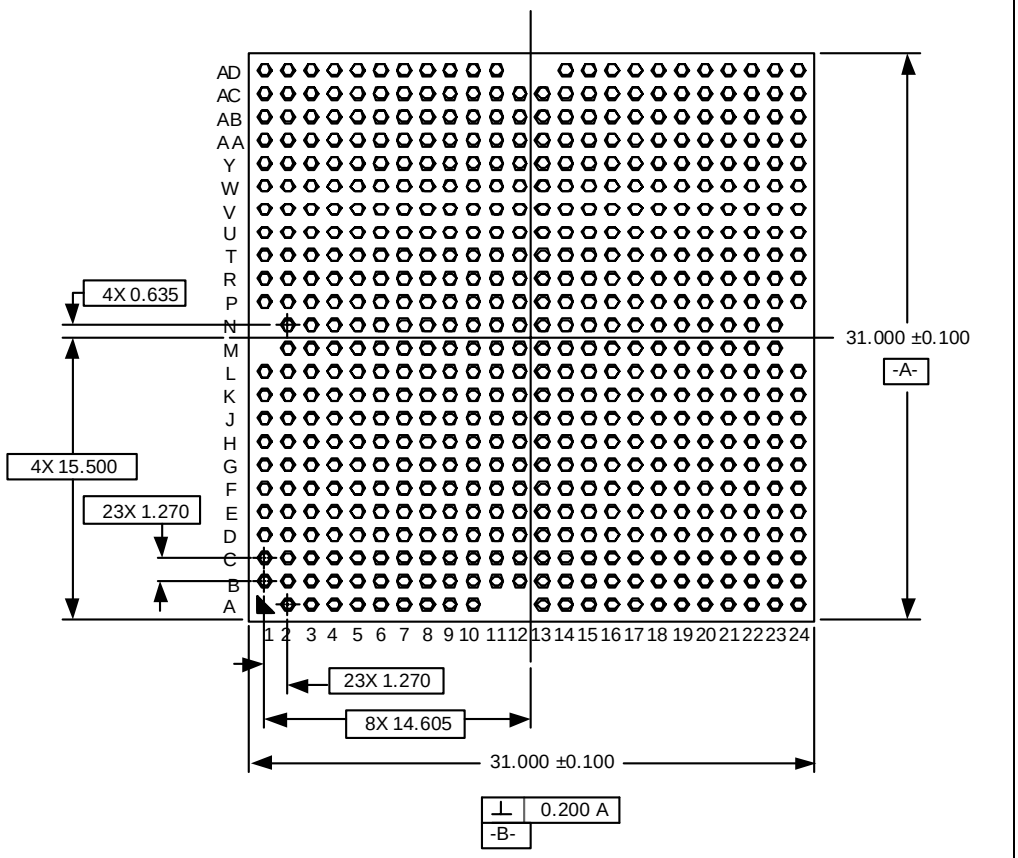


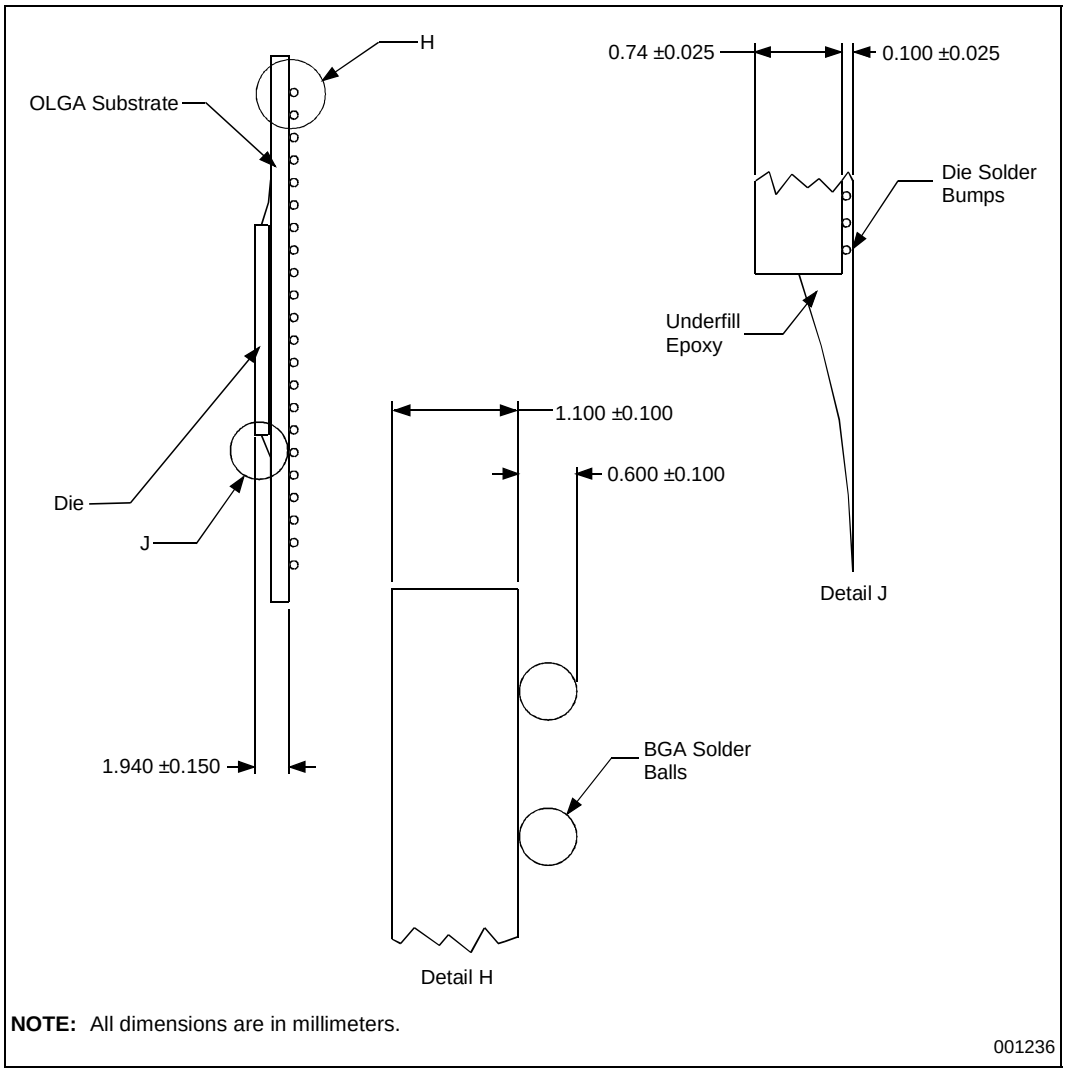
Figure 6-2. 567-Ball (DMH) OLGA1 Package Dimensions – Bottom View



NOTE: All dimensions are in millimeters.

001235

Figure 6-3. 567-Ball (DMH) OLGA1 Solder Balls Detail



6.2 Ballout Signal List

Table 6-1. DMH Ball List

Ball Number	Signal
A2	VCC25
A3	BC0SCLK#[1]
A4	BC0SCLK[1]
A5	VCC25
A6	BC0SCLK#[0]
A7	BC0SCLK[0]
A8	VCC25
A9	BC0A[3]
A10	BC0A[4]
A13	BC0A[12]
A14	BC1A[12]
A15	BC1A[4]
A16	BC1A[3]
A17	VCC25
A18	BC1SCLK[0]
A19	BC1SCLK#[0]
A20	VCC25
A21	BC1SCLK[1]
A22	BC1SCLK#[1]
A23	VCC25
A24	VSS
B1	BC0DQ[20]
B2	BC0DQ[16]
B3	VSS
B4	BC0SCLK#[2]
B5	BC0SCLK[2]
B6	VSS
B7	BC0CS#[0]
B8	BC0A[1]
B9	VSS
B10	BC0A[2]
B11	BC0A[8]
B12	VSS
B13	VSS
B14	BC1A[8]
B15	BC1A[2]
B16	VSS
B17	BC1A[1]

Ball Number	Signal
B18	BC1CS#[0]
B19	VSS
B20	BC1SCLK[2]
B21	BC1SCLK#[2]
B22	VSS
B23	BC1DQ[16]
B24	BC1DQ[20]
C1	VCC25
C2	BC0DQ[17]
C3	BC0DQ[21]
C4	VCC25
C5	BC0SCLK#[3]
C6	BC0SCLK[3]
C7	VCC25
C8	BC0CS#[1]
C9	BC0A[0]
C10	VCC25
C11	BC0A[7]
C12	BC0A[9]
C13	BC1A[9]
C14	BC1A[7]
C15	VCC25
C16	BC1A[0]
C17	BC1CS#[1]
C18	VCC25
C19	BC1SCLK[3]
C20	BC1SCLK#[3]
C21	VCC25
C22	BC1DQ[21]
C23	BC1DQ[17]
C24	VCC25
D1	BC0DQS[2]
D2	VSS
D3	BC0DQ[12]
D4	BC0DQ[8]
D5	VSS
D6	BC0CS#[2]
D7	BC0CS#[3]

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
D8	VSS
D9	BC0CS#[4]
D10	BC0A[6]
D11	VSS
D12	BC0A[13]
D13	BC1A[13]
D14	VSS
D15	BC1A[6]
D16	BC1CS#[4]
D17	VSS
D18	BC1CS#[3]
D19	BC1CS#[2]
D20	VSS
D21	BC1DQ[8]
D22	BC1DQ[12]
D23	VSS
D24	BC1DQS[2]
E1	BC0DQ[18]
E2	BC0DQS[11]
E3	VCC25
E4	BC0DQ[13]
E5	BC0DQ[9]
E6	VCC25
E7	BC0CS#[5]
E8	BC0CS#[6]
E9	VCC25
E10	BC0A[5]
E11	BC0A[11]
E12	VCC25
E13	VCC25
E14	BC1A[11]
E15	BC1A[5]
E16	VCC25
E17	BC1CS#[6]
E18	BC1CS#[5]
E19	VCC25
E20	BC1DQ[9]
E21	BC1DQ[13]
E22	VCC25

Ball Number	Signal
E23	BC1DQS[11]
E24	BC1DQ[18]
F1	VSS
F2	BC0DQ[22]
F3	BC0DQS[10]
F4	VSS
F5	BC0DQS[1]
F6	BC0DQ[7]
F7	VSS
F8	BC0CS#[7]
F9	BC0BA[0]
F10	BC0A[10]
F11	BC0A[14]
F12	BC0CKE
F13	BC1CKE
F14	BC1A[14]
F15	BC1A[10]
F16	BC1BA[0]
F17	BC1CS#[7]
F18	VSS
F19	BC1DQ[7]
F20	BC1DQS[1]
F21	VSS
F22	BC1DQS[10]
F23	BC1DQ[22]
F24	VSS
G1	BC0DQ[19]
G2	VCC25
G3	BC0DQ[15]
G4	BC0DQ[14]
G5	VCC25
G6	BC0DQ[5]
G7	BC0DQ[4]
G8	VCC25
G9	BC0SRCAL
G10	BC0BA[1]
G11	VSS
G12	BC0WE#
G13	BC1WE#

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
G14	VSS
G15	BC1BA[1]
G16	BC1SRCAL
G17	VCC25
G18	BC1DQ[4]
G19	BC1DQ[5]
G20	VCC25
G21	BC1DQ[14]
G22	BC1DQ[15]
G23	VCC25
G24	BC1DQ[19]
H1	BC0DQ[23]
H2	BC0DQ[24]
H3	VSS
H4	BC0DQ[10]
H5	BC0DQS[0]
H6	VSS
H7	BC0DQS[9]
H8	BC0DQ[0]
H9	SREFFB
H10	AD0VREF
H11	BC0CAS#
H12	BC0RAS#
H13	BC1RAS#
H14	BC1CAS#
H15	330-ohm P/D
H16	SREF
H17	BC1DQ[0]
H18	BC1DQS[9]
H19	VSS
H20	BC1DQS[0]
H21	BC1DQ[10]
H22	VSS
H23	BC1DQ[24]
H24	BC1DQ[23]
J1	VCC25
J2	BC0DQ[28]
J3	BC0DQ[11]
J4	VCC25

Ball Number	Signal
J5	BC0DQ[3]
J6	BC0DQ[2]
J7	VCC25
J8	N/C
J9	N/C
J10	VSS
J11	VCCRAC
J12	VSS
J13	VCCRAC
J14	VSS
J15	AD1VREF
J16	TSO[a]
J17	330-ohm P/D
J18	VCC25
J19	BC1DQ[2]
J20	BC1DQ[3]
J21	VCC25
J22	BC1DQ[11]
J23	BC1DQ[28]
J24	VCC25
K1	BC0DQ[29]
K2	VSS
K3	BC0DQ[25]
K4	BC0DQS[3]
K5	VSS
K6	BC0DQ[6]
K7	BC0DQ[1]
K8	BC0VSSAA
K9	VCCDLY
K10	VCC25
K11	VSS
K12	VCCRAC
K13	VSS
K14	VCCRAC
K15	VSS
K16	VCCDLY
K17	BC1VSSAA
K18	BC1DQ[1]
K19	BC1DQ[6]

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
K20	VSS
K21	BC1DQS[3]
K22	BC1DQ[25]
K23	VSS
K24	BC1DQ[29]
L1	BC0DQS[12]
L2	BC0DQ[30]
L3	VCC25
L4	BC0DQ[26]
L5	BC0DQ[69]
L6	VCC25
L7	BC0DQ[68]
L8	BC0VREFA
L9	VSS
L10	VSS
L11	VCCRAC
L12	VSS
L13	VCCRAC
L14	VSS
L15	VCC25
L16	VSS
L17	BC1VREFA
L18	BC1DQ[68]
L19	VCC25
L20	BC1DQ[69]
L21	BC1DQ[26]
L22	VCC25
L23	BC1DQ[30]
L24	BC1DQS[12]
M2	BC0DQ[27]
M3	BC0DQ[31]
M4	VSS
M5	BC0DQ[65]
M6	BC0DQ[64]
M7	VSS
M8	BC0VSSAB
M9	VCCDLY
M10	VCC25
M11	VSS

Ball Number	Signal
M12	VCCRAC
M13	VSS
M14	VCCRAC
M15	VSS
M16	VCCDLY
M17	BC1VSSAB
M18	VSS
M19	BC1DQ[64]
M20	BC1DQ[65]
M21	VSS
M22	BC1DQ[31]
M23	BC1DQ[27]
N2	VCC25
N3	BC0DQ[32]
N4	BC0DQ[36]
N5	VCC25
N6	BC0DQS[17]
N7	BC0DQS[8]
N8	BC0VREFB
N9	VSS
N10	VSS
N11	VCCRAC
N12	VSS
N13	VCCRAC
N14	VSS
N15	VCC25
N16	VSS
N17	BC1VREFB
N18	BC1DQS[8]
N19	BC1DQS[17]
N20	VCC25
N21	BC1DQ[36]
N22	BC1DQ[32]
N23	VCC25
P1	BC0DQ[37]
P2	BC0DQ[33]
P3	VSS
P4	BC0DQS[4]
P5	BC0DQ[70]

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
P6	VSS
P7	BC0DQ[66]
P8	BC0VSSAC
P9	VCCDLY
P10	VCC25
P11	VSS
P12	VCCRAC
P13	VSS
P14	VCCRAC
P15	VSS
P16	VCCDLY
P17	BC1VSSAC
P18	BC1DQ[66]
P19	VSS
P20	BC1DQ[70]
P21	BC1DQS[4]
P22	VSS
P23	BC1DQ[33]
P24	BC1DQ[37]
R1	VCC25
R2	BC0DQS[13]
R3	BC0DQ[34]
R4	VCC25
R5	BC0DQ[71]
R6	BC0DQ[67]
R7	VCC25
R8	BC0DQ[59]
R9	VSS
R10	VSS
R11	VCCRAC
R12	VSS
R13	VCCRAC
R14	VSS
R15	VCC25
R16	VSS
R17	BC1DQ[59]
R18	VCC25
R19	BC1DQ[67]
R20	BC1DQ[71]

Ball Number	Signal
R21	VCC25
R22	BC1DQ[34]
R23	BC1DQS[13]
R24	VCC25
T1	BC0DQ[38]
T2	VSS
T3	BC0DQ[39]
T4	BC0DQ[35]
T5	VSS
T6	BC0DQ[60]
T7	BC0DQ[61]
T8	VSS
T9	BC0VREFC
T10	VCC25
T11	VSS
T12	VCCRAC
T13	VSS
T14	VCCRAC
T15	VSS
T16	BC1VREFC
T17	VSS
T18	BC1DQ[61]
T19	BC1DQ[60]
T20	VSS
T21	BC1DQ[35]
T22	BC1DQ[39]
T23	VSS
T24	BC1DQ[38]
U1	BC0DQ[40]
U2	BC0DQ[44]
U3	VCC25
U4	BC0DQ[52]
U5	BC0DQ[48]
U6	VCC25
U7	BC0DQ[62]
U8	BC0DQ[63]
U9	330-ohm P/D
U10	PWRGOOD
U11	VCC25

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
U12	N/C
U13	330-ohm P/D
U14	VCC25
U15	N/C
U16	XORIN
U17	BC1DQ[63]
U18	BC1DQ[62]
U19	VCC25
U20	BC1DQ[48]
U21	BC1DQ[52]
U22	VCC25
U23	BC1DQ[44]
U24	BC1DQ[40]
V1	VSS
V2	BC0DQ[45]
V3	BC0DQ[53]
V4	VSS
V5	BC0DQ[49]
V6	BC0DQS[16]
V7	VSS
V8	BC0DQ[58]
V9	Reset#
V10	330-ohm P/U
V11	N/C
V12	N/C
V13	XOROUT
V14	330-ohm P/D
V15	VSS
V16	330-ohm P/D
V17	BC1DQ[58]
V18	VSS
V19	BC1DQS[16]
V20	BC1DQ[49]
V21	VSS
V22	BC1DQ[53]
V23	BC1DQ[45]
V24	VSS
W1	BC0DQ[41]
W2	VCC25

Ball Number	Signal
W3	BC0DQS[15]
W4	BC0DQ[54]
W5	VCC25
W6	BC0DQS[7]
W7	BC0DQ[56]
W8	VCC25
W9	SDA
W10	SCL
W11	VCC25
W12	N/C
W13	VCC25
W14	VSS
W15	330-ohm P/D
W16	N/C
W17	VCC25
W18	BC1DQ[56]
W19	BC1DQS[7]
W20	VCC25
W21	BC1DQ[54]
W22	BC1DQS[15]
W23	VCC25
W24	BC1DQ[41]
Y1	BC0DQS[14]
Y2	BC0DQS[5]
Y3	VSS
Y4	BC0DQ[55]
Y5	BC0DQS[6]
Y6	BC0DQ[57]
Y7	VSS
Y8	VCCRAC
Y9	VCCRAC
Y10	VCCRACA
Y11	VCCRACA
Y12	VCCRAC
Y13	VSS
Y14	VREFBRAC
Y15	VSS
Y16	VCCRAC
Y17	VSS

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
Y18	VCCRAC
Y19	BC1DQ[57]
Y20	BC1DQS[6]
Y21	BC1DQ[55]
Y22	VSS
Y23	BC1DQS[5]
Y24	BC1DQS[14]
AA1	VCC25
AA2	BC0DQ[42]
AA3	BC0DQ[50]
AA4	VCC25
AA5	N/C
AA6	VSS
AA7	DQB[3]
AA8	VSS
AA9	DQB[0]
AA10	VSS
AA11	VCCRAC
AA12	VSS
AA13	RQ[5]
AA14	VSS
AA15	CTMN
AA16	VSS
AA17	DQA[1]
AA18	VSS
AA19	VCCRAC
AA20	VSS
AA21	VCC25
AA22	BC1DQ[50]
AA23	BC1DQ[42]
AA24	VCC25
AB1	BC0DQ[46]
AB2	VSS
AB3	BC0DQ[51]
AB4	SIO
AB5	VSS
AB6	DQB[5]
AB7	VSS
AB8	DQB[1]
AB9	VSS

Ball Number	Signal
AB10	RQ[1]
AB11	VSS
AB12	RQ[4]
AB13	VSS
AB14	VREFARAC
AB15	VSS
AB16	CFMN
AB17	VSS
AB18	DQA[2]
AB19	VSS
AB20	DQA[5]
AB21	VSS
AB22	BC1DQ[51]
AB23	VSS
AB24	BC1DQ[46]
AC1	VSS
AC2	BC0DQ[43]
AC3	SCK
AC4	VSS
AC5	DQB[7]
AC6	VSS
AC7	DQB[4]
AC8	VSS
AC9	RQ[0]
AC10	VSS
AC11	RQ[3]
AC12	VSS
AC13	RQ[6]
AC14	VSS
AC15	CTM
AC16	VSS
AC17	DQA[0]
AC18	VSS
AC19	DQA[4]
AC20	VSS
AC21	DQA[7]
AC22	VSS
AC23	BC1DQ[43]
AC24	VSS

Table 6-1. DMH Ball List (Continued)

Ball Number	Signal
AD1	BC0DQ[47]
AD2	CMD
AD3	VSS
AD4	DQB[8]
AD5	VSS
AD6	DQB[6]
AD7	VSS
AD8	DQB[2]
AD9	VSS
AD10	RQ[2]
AD11	VSS
AD14	RQ[7]
AD15	VSS
AD16	CFM
AD17	VSS
AD18	DQA[3]
AD19	VSS
AD20	DQA[6]
AD21	VSS
AD22	DQA[8]
AD23	VSS
AD24	BC1DQ[47]

a. TSO strapped to GND for normal operation. When TSO is driven high, it will enter Parametric Test Mode. Refer to Section 7.1, “Parametric Test Mode” for more information.

Table 6-2. DMH Signal – Ball Number

Signal	Ball Number
AD0VREF	H10
AD1VREF	J15
BC0A[0]	C9
BC0A[1]	B8
BC0A[10]	F10
BC0A[11]	E11
BC0A[12]	A13
BC0A[13]	D12
BC0A[14]	F11
BC0A[2]	B10
BC0A[3]	A9
BC0A[4]	A10
BC0A[5]	E10
BC0A[6]	D10
BC0A[7]	C11
BC0A[8]	B11
BC0A[9]	C12
BC0BA[0]	F9
BC0BA[1]	G10
BC0CAS#	H11
BC0CKE	F12
BC0CS#[0]	B7
BC0CS#[1]	C8
BC0CS#[2]	D6
BC0CS#[3]	D7
BC0CS#[4]	D9
BC0CS#[5]	E7
BC0CS#[6]	E8
BC0CS#[7]	F8
BC0DQ[0]	H8
BC0DQ[1]	K7
BC0DQ[10]	H4
BC0DQ[11]	J3
BC0DQ[12]	D3
BC0DQ[13]	E4
BC0DQ[14]	G4
BC0DQ[15]	G3
BC0DQ[16]	B2
BC0DQ[51]	AB3
BC0DQ[52]	U4
BC0DQ[53]	V3
BC0DQ[54]	W4

Signal	Ball Number
BC0DQ[17]	C2
BC0DQ[18]	E1
BC0DQ[19]	G1
BC0DQ[2]	J6
BC0DQ[20]	B1
BC0DQ[21]	C3
BC0DQ[22]	F2
BC0DQ[23]	H1
BC0DQ[24]	H2
BC0DQ[25]	K3
BC0DQ[26]	L4
BC0DQ[27]	M2
BC0DQ[28]	J2
BC0DQ[29]	K1
BC0DQ[3]	J5
BC0DQ[30]	L2
BC0DQ[31]	M3
BC0DQ[32]	N3
BC0DQ[33]	P2
BC0DQ[34]	R3
BC0DQ[35]	T4
BC0DQ[36]	N4
BC0DQ[37]	P1
BC0DQ[38]	T1
BC0DQ[39]	T3
BC0DQ[4]	G7
BC0DQ[40]	U1
BC0DQ[41]	W1
BC0DQ[42]	AA2
BC0DQ[43]	AC2
BC0DQ[44]	U2
BC0DQ[45]	V2
BC0DQ[46]	AB1
BC0DQ[47]	AD1
BC0DQ[48]	U5
BC0DQ[49]	V5
BC0DQ[5]	G6
BC0DQ[50]	AA3
BC0DQS[6]	Y5
BC0DQS[7]	W6
BC0DQS[8]	N7
BC0DQS[9]	H7

Table 6-2. DMH Signal – Ball Number (Continued)

Signal	Ball Number
BC0DQ[55]	Y4
BC0DQ[56]	W7
BC0DQ[57]	Y6
BC0DQ[58]	V8
BC0DQ[59]	R8
BC0DQ[6]	K6
BC0DQ[60]	T6
BC0DQ[61]	T7
BC0DQ[62]	U7
BC0DQ[63]	U8
BC0DQ[64]	M6
BC0DQ[65]	M5
BC0DQ[66]	P7
BC0DQ[67]	R6
BC0DQ[68]	L7
BC0DQ[69]	L5
BC0DQ[7]	F6
BC0DQ[70]	P5
BC0DQ[71]	R5
BC0DQ[8]	D4
BC0DQ[9]	E5
BC0DQS[0]	H5
BC0DQS[1]	F5
BC0DQS[10]	F3
BC0DQS[11]	E2
BC0DQS[12]	L1
BC0DQS[13]	R2
BC0DQS[14]	Y1
BC0DQS[15]	W3
BC0DQS[16]	V6
BC0DQS[17]	N6
BC0DQS[2]	D1
BC0DQS[3]	K4
BC0DQS[4]	P4
BC0DQS[5]	Y2
BC1CKE	F13
BC1CS#[0]	B18
BC1CS#[1]	C17
BC1CS#[2]	D19
BC1CS#[3]	D18
BC1CS#[4]	D16
BC1CS#[5]	E18

Signal	Ball Number
BC0RAS#	H12
BC0SCLK[0]	A7
BC0SCLK[1]	A4
BC0SCLK[2]	B5
BC0SCLK[3]	C6
BC0SCLK#[0]	A6
BC0SCLK#[1]	A3
BC0SCLK#[2]	B4
BC0SCLK#[3]	C5
BC0SRCAL	G9
BC0VREFA	L8
BC0VREFB	N8
BC0VREFC	T9
BC0VSSAA	K8
BC0VSSAB	M8
BC0VSSAC	P8
BC0WE#	G12
BC1A[0]	C16
BC1A[1]	B17
BC1A[10]	F15
BC1A[11]	E14
BC1A[12]	A14
BC1A[13]	D13
BC1A[14]	F14
BC1A[2]	B15
BC1A[3]	A16
BC1A[4]	A15
BC1A[5]	E15
BC1A[6]	D15
BC1A[7]	C14
BC1A[8]	B14
BC1A[9]	C13
BC1BA[0]	F16
BC1BA[1]	G15
BC1CAS#	H14
BC1DQ[36]	N21
BC1DQ[37]	P24
BC1DQ[38]	T24
BC1DQ[39]	T22
BC1DQ[4]	G18
BC1DQ[40]	U24
BC1DQ[41]	W24

Table 6-2. DMH Signal – Ball Number (Continued)

Signal	Ball Number
BC1CS#[6]	E17
BC1CS#[7]	F17
BC1DQ[0]	H17
BC1DQ[1]	K18
BC1DQ[10]	H21
BC1DQ[11]	J22
BC1DQ[12]	D22
BC1DQ[13]	E21
BC1DQ[14]	G21
BC1DQ[15]	G22
BC1DQ[16]	B23
BC1DQ[17]	C23
BC1DQ[18]	E24
BC1DQ[19]	G24
BC1DQ[2]	J19
BC1DQ[20]	B24
BC1DQ[21]	C22
BC1DQ[22]	F23
BC1DQ[23]	H24
BC1DQ[24]	H23
BC1DQ[25]	K22
BC1DQ[26]	L21
BC1DQ[27]	M23
BC1DQ[28]	J23
BC1DQ[29]	K24
BC1DQ[3]	J20
BC1DQ[30]	L23
BC1DQ[31]	M22
BC1DQ[32]	N22
BC1DQ[33]	P23
BC1DQ[34]	R22
BC1DQ[35]	T21
BC1DQ[71]	R20
BC1DQ[8]	D21
BC1DQ[9]	E20
BC1DQS[0]	H20
BC1DQS[1]	F20
BC1DQS[10]	F22
BC1DQS[11]	E23
BC1DQS[12]	L24
BC1DQS[13]	R23
BC1DQS[14]	Y24

Signal	Ball Number
BC1DQ[42]	AA23
BC1DQ[43]	AC23
BC1DQ[44]	U23
BC1DQ[45]	V23
BC1DQ[46]	AB24
BC1DQ[47]	AD24
BC1DQ[48]	U20
BC1DQ[49]	V20
BC1DQ[5]	G19
BC1DQ[50]	AA22
BC1DQ[51]	AB22
BC1DQ[52]	U21
BC1DQ[53]	V22
BC1DQ[54]	W21
BC1DQ[55]	Y21
BC1DQ[56]	W18
BC1DQ[57]	Y19
BC1DQ[58]	V17
BC1DQ[59]	R17
BC1DQ[6]	K19
BC1DQ[60]	T19
BC1DQ[61]	T18
BC1DQ[62]	U18
BC1DQ[63]	U17
BC1DQ[64]	M19
BC1DQ[65]	M20
BC1DQ[66]	P18
BC1DQ[67]	R19
BC1DQ[68]	L18
BC1DQ[69]	L20
BC1DQ[7]	F19
BC1DQ[70]	P20
330-ohm P/U	V10
CFM	AD16
CFMN	AB16
CMD	AD2
CTM	AC15
CTMN	AA15
DQA[0]	AC17
DQA[1]	AA17
DQA[2]	AB18
DQA[3]	AD18

Table 6-2. DMH Signal – Ball Number (Continued)

Signal	Ball Number
BC1DQS[15]	W22
BC1DQS[16]	V19
BC1DQS[17]	N19
BC1DQS[2]	D24
BC1DQS[3]	K21
BC1DQS[4]	P21
BC1DQS[5]	Y23
BC1DQS[6]	Y20
BC1DQS[7]	W19
BC1DQS[8]	N18
BC1DQS[9]	H18
BC1RAS#	H13
BC1SCLK[0]	A18
BC1SCLK[1]	A21
BC1SCLK[2]	B20
BC1SCLK[3]	C19
BC1SCLK#[0]	A19
BC1SCLK#[1]	A22
BC1SCLK#[2]	B21
BC1SCLK#[3]	C20
BC1SRCAL	G16
BC1VREFA	L17
BC1VREFB	N17
BC1VREFC	T16
BC1VSSAA	K17
BC1VSSAB	M17
BC1VSSAC	P17
BC1WE#	G13
330-ohm P/D	U9
RQ[4]	AB12
RQ[5]	AA13
RQ[6]	AC13
RQ[7]	AD14
SREFFB	H9
SREF	H16
SCK	AC3
SCL	W10
SDA	W9
330-ohm P/D	W15
N/C	U15
SIO	AB4
N/C	V11

Signal	Ball Number
DQA[4]	AC19
DQA[5]	AB20
DQA[6]	AD20
DQA[7]	AC21
DQA[8]	AD22
DQB[0]	AA9
DQB[1]	AB8
DQB[2]	AD8
DQB[3]	AA7
DQB[4]	AC7
DQB[5]	AB6
DQB[6]	AD6
DQB[7]	AC5
DQB[8]	AD4
N/C	W16
330-ohm P/D	H15
330-ohm P/D	J17
330-ohm P/D	V16
330-ohm P/D	U13
330-ohm P/D	V14
PWRGOOD	U10
N/C	J8
N/C	J9
N/C	AA5
RESET#	V9
RQ[0]	AC9
RQ[1]	AB10
RQ[2]	AD10
RQ[3]	AC11
VCC25	AA1
VCC25	AA4
VCC25	AA21
VCC25	AA24
VCC25	C1
VCC25	C4
VCC25	C7
VCC25	C10
VCC25	C15
VCC25	C18
VCC25	C21
VCC25	C24
VCC25	E3

Table 6-2. DMH Signal – Ball Number (Continued)

Signal	Ball Number
N/C	U12
N/C	V12
N/C	W12
TSO[a]	J16
VCCRAC	J11
VCCRAC	J13
VCCRAC	K12
VCCRAC	K14
VCCRAC	L11
VCCRAC	L13
VCCRAC	M12
VCCRAC	M14
VCCRAC	N11
VCCRAC	N13
VCCRAC	P12
VCCRAC	P14
VCCRAC	R11
VCCRAC	R13
VCCRAC	T12
VCCRAC	T14
VCC25	A2
VCC25	A5
VCC25	A8
VCC25	A17
VCC25	A20
VCC25	A23
VCC25	N2
VCC25	N5
VCC25	N15
VCC25	N20
VCC25	N23
VCC25	P10
VCC25	R1
VCC25	R4
VCC25	R7
VCC25	R15
VCC25	R18
VCC25	R21
VCC25	R24
VCC25	T10
VCC25	U3
VCC25	U6

Signal	Ball Number
VCC25	E6
VCC25	E9
VCC25	E12
VCC25	E13
VCC25	E16
VCC25	E19
VCC25	E22
VCC25	G2
VCC25	G5
VCC25	G8
VCC25	G17
VCC25	G20
VCC25	G23
VCC25	J1
VCC25	J4
VCC25	J7
VCC25	J18
VCC25	J21
VCC25	J24
VCC25	K10
VCC25	L3
VCC25	L6
VCC25	L15
VCC25	L19
VCC25	L22
VCC25	M10
VCCRAC	Y16
VCCRAC	Y18
VCCRACA	Y10
VCCRACA	Y11
VREFARAC	AB14
VREFBRAC	Y14
VSS	A24
VSS	AA6
VSS	AA8
VSS	AA10
VSS	AA12
VSS	AA14
VSS	AA16
VSS	AA18
VSS	AA20
VSS	AB2

Table 6-2. DMH Signal – Ball Number (Continued)

Signal	Ball Number
VCC25	U11
VCC25	U14
VCC25	U19
VCC25	U22
VCC25	W2
VCC25	W5
VCC25	W8
VCC25	W11
VCC25	W13
VCC25	W17
VCC25	W20
VCC25	W23
VCCDLY	K9
VCCDLY	K16
VCCDLY	M9
VCCDLY	M16
VCCDLY	P9
VCCDLY	P16
VCCRAC	AA11
VCCRAC	AA19
VCCRAC	Y8
VCCRAC	Y9
VCCRAC	Y12
VSS	AD5
VSS	AD7
VSS	AD9
VSS	AD11
VSS	AD15
VSS	AD17
VSS	AD19
VSS	AD21
VSS	AD23
VSS	B3
VSS	B6
VSS	B9
VSS	B12
VSS	B13
VSS	B16
VSS	B19
VSS	B22
VSS	D2
VSS	D5

Signal	Ball Number
VSS	AB5
VSS	AB7
VSS	AB9
VSS	AB11
VSS	AB13
VSS	AB15
VSS	AB17
VSS	AB19
VSS	AB21
VSS	AB23
VSS	AC1
VSS	AC4
VSS	AC6
VSS	AC8
VSS	AC10
VSS	AC12
VSS	AC14
VSS	AC16
VSS	AC18
VSS	AC20
VSS	AC22
VSS	AC24
VSS	AD3
VSS	J14
VSS	K2
VSS	K5
VSS	K11
VSS	K13
VSS	K15
VSS	K20
VSS	K23
VSS	L9
VSS	L10
VSS	L12
VSS	L14
VSS	L16
VSS	M4
VSS	M7
VSS	M11
VSS	M13
VSS	V21
VSS	V24

Table 6-2. DMH Signal – Ball Number (Continued)

Signal	Ball Number
VSS	D8
VSS	D11
VSS	D14
VSS	D17
VSS	D20
VSS	D23
VSS	F1
VSS	F4
VSS	F7
VSS	F18
VSS	F21
VSS	F24
VSS	G11
VSS	G14
VSS	H3
VSS	H6
VSS	H19
VSS	H22
VSS	J10
VSS	J12
VSS	T8
VSS	T11
VSS	T13
VSS	T15
VSS	T17
VSS	T20
VSS	T23
VSS	V1
VSS	V4
VSS	V7
VSS	V15
VSS	V18
VSS	W14
VSS	Y3

Signal	Ball Number
VSS	Y7
VSS	Y13
VSS	Y15
VSS	Y17
VSS	M15
VSS	M18
VSS	M21
VSS	N9
VSS	N10
VSS	N12
VSS	N14
VSS	N16
VSS	P3
VSS	P6
VSS	P11
VSS	P13
VSS	P15
VSS	P19
VSS	P22
VSS	R9
VSS	R10
VSS	R12
VSS	R14
VSS	R16
VSS	T2
VSS	T5
VSS	Y22
XORIN	U16
XOROUT	V13
XORIN	U16
XOROUT	V13

a. TSO strapped to GND for normal operation. When TSO is driven high, it will enter Parametric Test Mode. Refer to Section 7.1, "Parametric Test Mode" for more information.

Testability 7

There is no JTAG circuitry in the DMH. To check the connectivity of the pins, the DMH supports the use of the parametric XOR tree test mode. Table 7-1 lists the signals needed for enabling the parametric test.

Table 7-1. Parametric Test Control Signals

Function	Signal	I/O	Description
Tristate Outputs	TSO	I	Tristate all outputs except XOROUT.
Parametric Data In	XORIN	I	Input pin to the Parametric Tree.
Parametric Data Out	XOROUT	O	Output pin from the Parametric Tree.

7.1 Parametric Test Mode

A single XOR chain is provided in the DMH. The TSO signal needs to be asserted (active high) during XOR chain mode. The pin orders are shown in Table 7-2.

Table 7-2. Parametric Test Pin Order

Pin Order	Pin Names	Pin Order	Pin Names
1	XORIN	24	DQB[1]
2	DQA[8]	25	DQB[2]
3	DQA[7]	26	DQB[3]
4	DQA[6]	27	DQB[4]
5	DQA[5]	28	DQB[5]
6	DQA[4]	29	DQB[6]
7	DQA[3]	30	DQB[7]
8	DQA[2]	31	DQB[8]
9	DQA[1]	32	CMD
10	DQA[0]	33	SCK
11	CTM	34	SIO
12	CTMN	35	RESET#
13	CFM	36	PWRGOOD
14	CFMN	37	Reserved (Ball Number: U9)
15	RQ[7]	38	Reserved (Ball Number: V10)
16	RQ[6]	39	SCL
17	RQ[5]	40	SDA
18	RQ[4]	41	BC0DQ[56]
19	RQ[3]	42	BC0DQ[60]
20	RQ[2]	43	BC0DQ[63]
21	RQ[1]	44	BC0DQ[61]
22	RQ[0]	45	BC0DQS[16]
23	DQB[0]	46	BC0DQS[7]

Table 7-2. Parametric Test Pin Order (Continued)

Pin Order	Pin Names	Pin Order	Pin Names
47	BC0DQ[58]	92	BC0DQ[28
48	BC0DQ[57]	93	BC0DQ[31]
49	BC0DQ[59]	94	BC0DQ[29]
50	BC0DQ[62]	95	BC0DQS[12]
51	BC0DQ[48]	96	BC0DQS[3]
52	BC0DQ[52]	97	BC0DQ[26]
53	BC0DQ[55]	98	BC0DQ[25]
54	BC0DQ[53]	99	BC0DQ[27]
55	BC0DQS[15]	100	BC0DQ[30]
56	BC0DQS[6]	101	BC0DQ[0]
57	BC0DQ[50]	102	BC0DQ[4]
58	BC0DQ[49]	103	BC0DQ[7]
59	BC0DQ[51]	104	BC0DQ[5]
60	BC0DQ[54]	105	BC0DQS[9]
61	BC0DQ[40]	106	BC0DQS[0]
62	BC0DQ[44]	107	BC0DQ[2]
63	BC0DQ[47]	108	BC0DQ[1]
64	BC0DQ[45]	109	BC0DQ[3]
65	BC0DQS[14]	110	BC0DQ[6]
66	BC0DQS[5]	111	BC0DQ[8]
67	BC0DQ[42]	112	BC0DQ[12]
68	BC0DQ[41]	113	BC0DQ[15]
69	BC0DQ[43]	114	BC0DQ[13]
70	BC0DQ[46]	115	BC0DQS[10]
71	BC0DQ[64]	116	BC0DQS[1]
72	BC0DQ[68]	117	BC0DQ[10]
73	BC0DQ[71]	118	BC0DQ[9]
74	BC0DQ[69]	119	BC0DQ[11]
75	BC0DQS[17]	120	BC0DQ[14]
76	BC0DQS[8]	121	BC0DQ[16]
77	BC0DQ[66]	122	BC0DQ[20]
78	BC0DQ[65]	123	BC0DQ[23]
79	BC0DQ[67]	124	BC0DQ[21]
80	BC0DQ[70]	125	BC0DQS[11]
81	BC0DQ[32]	126	BC0DQS[2]
82	BC0DQ[36]	127	BC0DQ[18]
83	BC0DQ[39]	128	BC0DQ[17]
84	BC0DQ[37]	129	BC0DQ[19]
85	BC0DQS[13]	130	BC0DQ[22]
86	BC0DQS[4]	131	SREFFB
87	BC0DQ[34]	132	BC0SCLK#[1]
88	BC0DQ[33]	133	BC0SCLK#[2]
89	BC0DQ[35]	134	BC0SCLK[2]
90	BC0DQ[38]	135	BC0SCLK[1]
91	BC0DQ[24]	136	BC0SCLK[3]

Table 7-2. Parametric Test Pin Order (Continued)

Pin Order	Pin Names	Pin Order	Pin Names
137	BC0SCLK#[3]	180	BC1CS#[7]
138	BC0SCLK#[0]	181	BC1CS#[3]
139	BC0CS#[5]	182	BC1CS#[0]
140	BC0CS#[2]	183	BC1CS#[6]
141	BC0SCLK[0]	184	BC1BA[0]
142	BC0CS#[7]	185	BC1CS#[1]
143	BC0CS#[3]	186	BC1A[10]
144	BC0CS#[0]	187	BC1BA[1]
145	BC0CS#[6]	188	BC1CS#[4]
146	BC0BA[0]	189	BC1A[5]
147	BC0CS#[1]	190	BC1A[0]
148	BC0A[10]	191	BC1A[1]
149	BC0BA[1]	192	BC1A[11]
150	BC0CS#[4]	193	BC1A[6]
151	BC0A[5]	194	BC1A[3]
152	BC0A[0]	195	BC1A[7]
153	BC0A[1]	196	BC1A[14]
154	BC0A[11]	197	BC1A[2]
155	BC0A[6]	198	BC1A[8]
156	BC0A[3]	199	BC1A[9]
157	BC0A[7]	200	BC1A[4]
158	BC0A[14]	201	BC1CAS#
159	BC0A[2]	202	BC1A[13]
160	BC0A[8]	203	BC1A[12]
161	BC0A[9]	204	BC1WE#
162	BC0A[4]	205	BC1RAS#
163	BC0CAS#	206	BC1CKE
164	BC0A[13]	207	Reserved (Ball Number: J17)
165	BC0A[12]	208	BC1DQ[0]
166	BC0WE#	209	BC1DQ[4]
167	BC0RAS#	210	BC1DQ[7]
168	BC0CKE	211	BC1DQ[5]
169	SREF	212	BC1DQS[9]
170	BC1SCLK#[1]	213	BC1DQS[0]
171	BC1SCLK#[2]	214	BC1DQ[2]
172	BC1SCLK[2]	215	BC1DQ[1]
173	BC1SCLK[1]	216	BC1DQ[3]
174	BC1SCLK[3]	217	BC1DQ[6]
175	BC1SCLK#[3]	218	BC1DQ[8]
176	BC1SCLK#[0]	219	BC1DQ[12]
177	BC1CS#[5]	220	BC1DQ[15]
178	BC1CS#[2]	221	BC1DQ[13]
179	BC1SCLK[0]	222	BC1DQS[10]

Table 7-2. Parametric Test Pin Order (Continued)

Pin Order	Pin Names	Pin Order	Pin Names
223	BC1DQS[1]	265	BC1DQ[25]
224	BC1DQ[10]	266	BC1DQ[27]
225	BC1DQ[9]	267	BC1DQ[30]
226	BC1DQ[11]	268	BC1DQ[56]
227	BC1DQ[14]	269	BC1DQ[60]
228	BC1DQ[16]	270	BC1DQ[63]
229	BC1DQ[20]	271	BC1DQ[61]
230	BC1DQ[23]	272	BC1DQS[16]
231	BC1DQ[21]	273	BC1DQS[7]
232	BC1DQS[11]	274	BC1DQ[58]
233	BC1DQS[2]	275	BC1DQ[57]
234	BC1DQ[18]	276	BC1DQ[59]
235	BC1DQ[17]	277	BC1DQ[62]
236	BC1DQ[19]	278	BC1DQ[48]
237	BC1DQ[22]	279	BC1DQ[52]
238	BC1DQ[64]	280	BC1DQ[55]
239	BC1DQ[68]	281	BC1DQ[53]
240	BC1DQ[71]	282	BC1DQS[15]
241	BC1DQ[69]	283	BC1DQS[6]
242	BC1DQS[17]	284	BC1DQ[50]
243	BC1DQS[8]	285	BC1DQ[49]
244	BC1DQ[66]	286	BC1DQ[51]
245	BC1DQ[65]	287	BC1DQ[54]
246	BC1DQ[67]	288	BC1DQ[40]
247	BC1DQ[70]	289	BC1DQ[44]
248	BC1DQ[32]	290	BC1DQ[47]
249	BC1DQ[36]	291	BC1DQ[45]
250	BC1DQ[39]	292	BC1DQS[14]
251	BC1DQ[37]	293	BC1DQS[5]
252	BC1DQS[13]	294	BC1DQ[42]
253	BC1DQS[4]	295	BC1DQ[41]
254	BC1DQ[34]	296	BC1DQ[43]
255	BC1DQ[33]	297	BC1DQ[46]
256	BC1DQ[35]	298	Reserved (Ball Number: W15)
257	BC1DQ[38]	299	Reserved (Ball Number: V14)
258	BC1DQ[24]	300	Reserved (Ball Number: U13)
259	BC1DQ[28]	301	XOROUT
260	BC1DQ[31]		
261	BC1DQ[29]		
262	BC1DQS[12]		
263	BC1DQS[3]		
264	BC1DQ[26]		