80960JA/JF/JD/JS/JC/JT 3.3 V Embedded 32-Bit Microprocessor

Datasheet

Product Features

- Code Compatible with all 80960Jx Processors
- High-Performance Embedded Architecture
  - —One Instruction/Clock Execution
  - —Core Clock Rate is:
    1x the Bus Clock for 80960JA/JF/JS
    2x the Bus Clock for 80960JD/JC
    3x the Bus Clock for 80960JT
  - —Load/Store Programming Model
  - —Sixteen 32-Bit Global Registers
  - —Sixteen 32-Bit Local Registers (8 sets)
  - —Nine Addressing Modes
  - —User/Supervisor Protection Model
- Two-Way Set Associative Instruction Cache
  - —80960JA - 2 Kbyte
  - —80960JF/JD - 4 Kbyte
  - —80960JS/JC/JT - 16 Kbyte
  - —Programmable Cache-Locking Mechanism
- Direct Mapped Data Cache
  - —80960JA - 1 Kbyte
  - —80960JF/JD - 2 Kbyte
  - —80960JS/JC/JT - 4 Kbyte
  - —Write Through Operation
- On-Chip Stack Frame Cache
  - —Seven Register Sets May Be Saved
  - —Automatic Allocation on Call/Return
  - —0-7 Frames Reserved for High-Priority Interrupts
- On-Chip Data RAM
  - —1 Kbyte Critical Variable Storage
  - —Single-Cycle Access
- 3.3 V Supply Voltage
  - —5 V Tolerant Inputs
  - —TTL Compatible Outputs
- High Bandwidth Burst Bus
  - —32-Bit Multiplexed Address/Data
  - —Programmable Memory Configuration
  - —Selectable 8-, 16-, 32-Bit Bus Widths
  - —Supports Unaligned Accesses
  - —Big or Little Endian Byte Ordering
- High-Speed Interrupt Controller
  - —31 Programmable Priorities
  - —Eight Maskable Pins plus NMI#
  - —Up to 240 Vectors in Expanded Mode
- Two On-Chip Timers
  - —Independent 32-Bit Counting
  - —Clock Prescaling by 1, 2, 4 or 8
  - —Internal Interrupt Sources
- Halt Mode for Low Power
- IEEE 1149.1 (JTAG) Boundary Scan Compatibility
- Packages
  - —132-Lead Pin Grid Array (PGA)
  - —132-Lead Plastic Quad Flat Pack (PQFP)
  - —196-Ball Mini Plastic Ball Grid Array (MPBGA)

Order Number: 273159-005
September 2002

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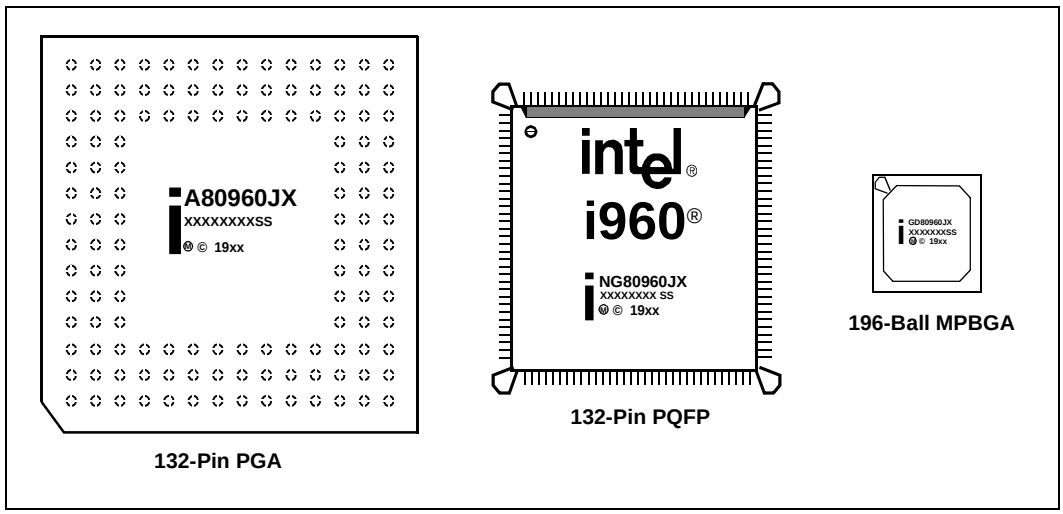
Revision History

Date	Revision	Description
September 2002	005	Removed reference to A80960JF-16 from Table 3 on page 15. Removed reference to NG80960JC-40, NG80960JC-33, NG80960JS-16, and NG80960JF-16 from Table 4 on page 15. Removed reference to GD80960JC-40, GD80960JC-33, and 80960JS-16 in Table 6 on page 16. Removed reference to 80960JC-40, 80960JC-33, 80960JS-16, and 80960JF-16 in Table 18 on page 35. Removed reference to 80960JC-40, 80960JC-33, 80960JS-16, and 80960JF-16 from Table 21 on page 39. Removed reference to 80960JC-40, 80960JC-33, 80960JS-16 and 80960JF-16 from Table 22 on page 42.
September 1999	004	Added new extended temp device offerings. See Table 5 on page 16. Removed PGA package availability from JS/JC/JT processors. Changed AC timing parameter T_{OV1} (min) for extended temp devices only. See Table 22 on page 42.
June 1999	003	Merged the 80960JS/JC datasheet information into this datasheet (previously named *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor* datasheet). Updated I_{CC} values for the 80960JS/JC/JT processors. Increased TIH1 specification for the 80960JS/JC/JT processors. Updated MPBGA thermal specifications.
December 1998	002	Corrected orientation of MPBGA package diagrams (Figure 6 on page 30 and Figure 7 on page 31). Added Figure 11 on page 46, Figure 12 on page 46, Figure 14 on page 47, and Figure 15 on page 48 to distinguish 80960JT 3.3-V and 5-V signal derating curves from the 80960JA/JF/JD derating curves.
March 1998	001	This datasheet supersedes revisions to the following 80960Jx datasheets: #273109 (JT), #272971-002 (JD), and #276146-001 (JA/JF). In addition to combining the documents into one, the following content was changed: Figure 1 on page 7: Added MPBGA package to diagram. Section 3.2.4, “80960Jx 196-Ball MPBGA Pinout” on page 30: Added new Figures 6 and 7, Tables 10, 11 and 13. Figure 16 on page 48: Added with the note that follows the figure.

1.0 Introduction

This document contains information for the 80960Jx microprocessors, including electrical characteristics and package pinout information. Detailed functional descriptions, other than parametric performance, are published in the *i960® Jx Microprocessor Developer's Manual* (272483) and may be viewed online at http://developer.intel.com/design/i960/Techinfo/80960JX/.

Figure 1. 80960Jx Microprocessor Package Options



Throughout this datasheet, references to '80960Jx' indicate features that apply to the 3.3-V Jx processors only:

Table 1. 80960Jx 3.3-V Microprocessor Family

Processor	Voltage	Instruction Cache	Data Cache	Core Clock
80960JA	3.3 V (5 V Tolerant)	2 Kbyte	1 Kbyte	1x
80960JF	3.3 V (5 V Tolerant)	4 Kbyte	2 Kbyte	1x
80960JD	3.3 V (5 V Tolerant)	4 Kbyte	2 Kbyte	2x
80960JS	3.3 V (5 V Tolerant)	16 Kbyte	4 Kbyte	1x
80960JC	3.3 V (5 V Tolerant)	16 Kbyte	4 Kbyte	2x
80960JT	3.3 V (5 V Tolerant)	16 Kbyte	4 Kbyte	3x

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2.0 80960Jx Overview

The 80960Jx processor offers high performance to cost-sensitive 32-bit embedded applications. The 80960Jx is object code compatible with the 80960 core architecture and is capable of sustained execution at the rate of one instruction per clock. This processor's features include generous instruction cache, data cache, and data RAM. It also boasts a fast interrupt mechanism and dual-programmable timer units.

The 80960Jx processor's clock multiplication operates the processor core at two or three times the bus clock rate to improve execution performance without increasing the complexity of board designs.

Memory subsystems for cost-sensitive embedded applications often impose substantial wait state penalties. The 80960Jx integrates considerable storage resources on-chip to decouple CPU execution from the external bus.

The 80960Jx rapidly allocates and de-allocates local register sets during context switches. The processor must flush a register set to the stack only when it saves more than seven sets to its local register cache.

A 32-bit multiplexed burst bus provides a high-speed interface to system memory and I/O. A full complement of control signals simplifies the connection of the 80960Jx to external components. The user programs physical and logical memory attributes through memory-mapped control registers (MMRs), an extension not found on the i960® Kx, Sx or Cx processors. Physical and logical configuration registers enable the processor to operate with all combinations of bus width and data object alignment. The processor supports a homogeneous byte ordering model.

This processor integrates two important peripherals: a timer unit and an interrupt controller. These and other hardware resources are programmed through memory-mapped control registers, an extension to the familiar i960 processor architecture.

The timer unit (TU) offers two independent 32-bit timers for use as real-time system clocks and general-purpose system timing. These operate in either single-shot or auto-reload mode and may generate interrupts.

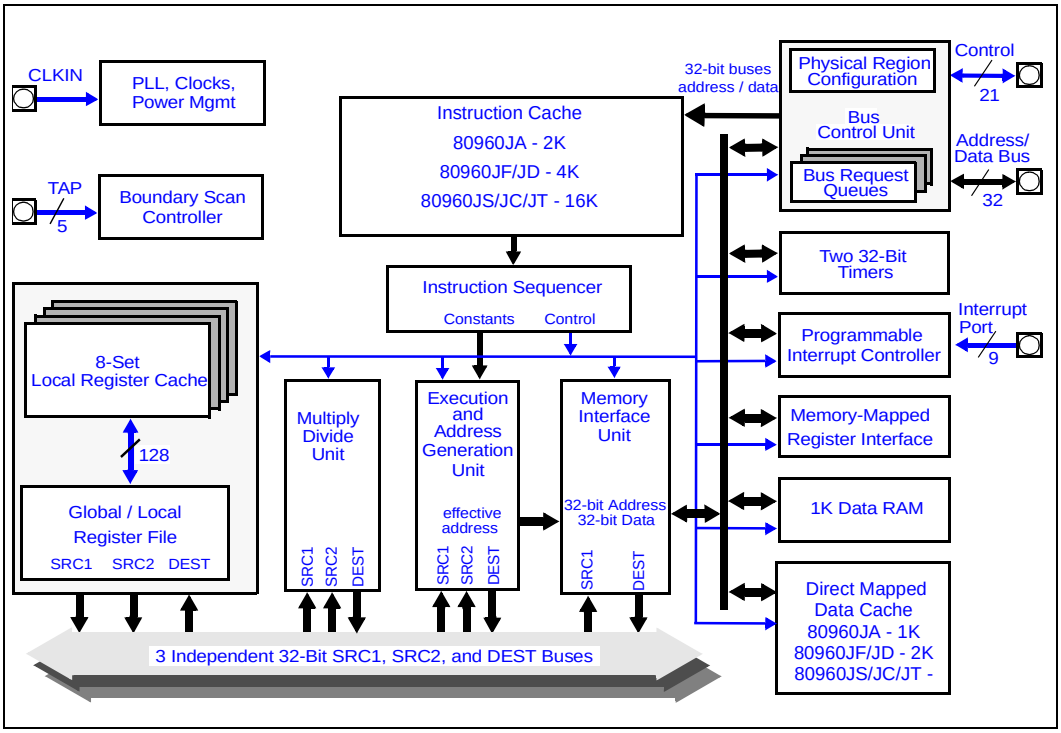
The interrupt controller unit (ICU) provides a flexible, low-latency means for requesting interrupts. The ICU provides full programmability of up to 240 interrupt sources into 31 priority levels. The ICU takes advantage of a cached priority table and optional routine caching to minimize interrupt latency. Clock doubling on the 80960JD/JC processors reduces interrupt latency by 40% compared to the 80960JA/JF, and clock tripling on the 80960JT reduces interrupt latency by 20% compared to the 80960JD/JC. Local registers may be dedicated to high-priority interrupts to further reduce latency. Acting independently from the core, the ICU compares the priorities of posted interrupts with the current process priority, off-loading this task from the core. The ICU also supports the integrated timer interrupts.

The 80960Jx features a Halt mode designed to support applications where low power consumption is critical. The **halt** instruction shuts down instruction execution, resulting in a power savings of up to 90 percent.

The 80960Jx's testability features, including ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG), provide a powerful environment for design debug and fault diagnosis.

The *Solutions960*® program features a wide variety of development tools which support the i960 processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

Figure 2. 80960Jx Block Diagram



2.1 80960 Processor Core

The 80960Jx family is a scalar implementation of the 80960 core architecture. Intel designed this processor core as a very high performance device that is also cost-effective. Factors that contribute to the core's performance include:

- Core operates at the bus speed with the 80960JA/JF/JS
- Core operates at two or three times the bus speed with the 80960JD/JC and 80960JT, respectively
- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- Two-way set associative, integrated instruction cache
- Direct-mapped, integrated data cache
- 1-Kbyte integrated data RAM delivers zero wait state program data

2.2 Burst Bus

A 32-bit high-performance Bus Controller Unit (BCU) interfaces the 80960Jx to external memory and peripherals. The BCU fetches instructions and transfers data at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Users may configure the 80960Jx's bus controller to match an application's fundamental memory organization. Physical bus width is register-programmed for up to eight regions. Byte ordering and data caching are programmed through a group of logical memory templates and a defaults register.

The BCU's features include:

- Multiplexed external bus to minimize pin count
- 32-, 16-, and 8-bit bus widths to simplify I/O interfaces
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Support for big or little endian byte ordering to facilitate the porting of existing program code
- Unaligned bus accesses performed transparently
- Three-deep load/store queue to decouple the bus from the core

Upon reset, the 80960Jx conducts an internal self-test. Then, before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the initialization boot record (IBR).

2.3 Timer Unit

The timer unit (TU) contains two independent 32-bit timers that are capable of counting at several clock rates and generating interrupts. Each is programmed by use of the TU registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960Jx's interrupt controller. The TU may generate a fault when unauthorized writes from user mode are detected. Clock prescaling is supported.

2.4 Priority Interrupt Controller

A programmable interrupt controller manages up to 240 external sources through an 8-bit external interrupt port. Alternatively, the interrupt inputs may be configured for individual edge- or level-triggered inputs. The interrupt unit (IU) also accepts interrupts from the two on-chip timer channels and a single Non-Maskable Interrupt (NMI#) pin. Interrupts are serviced according to their priority levels relative to the current process priority.

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960Jx exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines may be reserved on-chip.
- Register frames for high-priority interrupt handlers may be cached on-chip.
- The interrupt stack may be placed in cacheable memory space.
- Interrupt microcode executes at two or three times the bus frequency for the 80960JD/JC and 80960JT, respectively.

2.5 Instruction Set Summary

The 80960Jx adds several new instructions to the i960 processor core architecture. The new instructions are:

- Conditional Move
- Conditional Add
- Conditional Subtract
- Byte Swap
- Halt
- Cache Control
- Interrupt Control

Table 2 identifies the instructions that the 80960Jx supports. Refer to the *i960® Jx Microprocessor Developer's Manual* (272483) for a detailed description of each instruction.

2.6 Faults and Debugging

The 80960Jx employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. In software, the 80960Jx may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions may generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.7 Low Power Operation

Intel fabricates the 80960Jx using an advanced sub-micron manufacturing process. The processor's sub-micron topology provides the circuit density for optimal cache size and high operating speeds while dissipating modest power. The processor also uses dynamic power management to turn off clocks to unused circuits.

Users may program the 80960Jx to enter Halt mode for maximum power savings. In Halt mode, the processor core stops completely while the integrated peripherals continue to function, reducing overall power requirements up to 90 percent. Processor execution resumes from internally or externally generated interrupts.

2.8 Test Features

The 80960Jx incorporates numerous features that enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960Jx provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode may also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960Jx to electrically “remove” itself from a circuit board. This allows for system-level testing in which a remote tester, such as an in-circuit emulator, may exercise the processor system.

The provided test logic does not interfere with component or circuit board behavior and ensures that components function correctly, connections between various components are correct, and various components interact correctly on the printed circuit board.

The JTAG Boundary Scan feature is an attractive alternative to conventional “bed-of-nails” testing. It may examine connections that might otherwise be inaccessible to a test system.

2.9 Memory-Mapped Control Registers

The 80960Jx, although compliant with the i960 processor core, has the added advantage of memory-mapped, internal control registers not found on the i960 Kx, Sx or Cx processors. These registers give software the interface to easily read and modify internal control registers.

Each of these registers is accessed as a memory-mapped, 32-bit register. Access is accomplished through regular memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.10 Data Types and Memory Addressing Modes

As with all i960 processors, the 80960Jx instruction set supports several data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960Jx provides a full set of addressing modes for C and assembly programming:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement
- IP with displacement

Table 2. 80960Jx Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load Store Move Conditional Select† Load Address	Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Conditional Add† Conditional Subtract† Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal Byte Swap†
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Processor Management**	**Atomic**	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls Halt† System Control Cache Control† Interrupt Control†	Atomic Add Atomic Modify	

† Denotes new 80960 instructions unavailable on 80960CA/CF, 80960KA/KB and 80960SA/SB processors.

3.0 Packaging Information

3.1 Available Processors and Packages

The 80960Jx is offered in various speed grades and three package types.

The 132-pin Pin Grid Array (PGA) device is specified for operation at V_{CC} = 3.3 V ± 0.15 V over a case temperature range of 0° C to 100° C. The following processor versions are available in the PGA package:

Table 3. 80960Jx Processors Available in 132-Pin PGA Package

Processor	Core Speed	Bus Speed
A80960JD-66	66 MHz	33 MHz
A80960JD-33	33 MHz	16 MHz
A80960JA/JF-33	33 MHz	33 MHz
A80960JF-25	25 MHz	25 MHz

For pinout diagrams for the PGA package, see Section 3.2.2, “80960Jx 132-Lead PGA Pinout” on page 23.

The 132-pin Plastic Quad Flatpack (PQFP) devices are specified for operation at V_{CC} = 3.3 V ± 0.15 V over a case temperature range of 0° C to 100° C. Table 4 presents 80960Jx processor versions that are available in the 132-pin PQFP package:

Table 4. 80960Jx Processors Available in 132-Pin PQFP Package

Processor	Core Speed	Bus Speed
NG80960JT-100	100 MHz	33 MHz
NG80960JC-66	66 MHz	33 MHz
NG80960JC-50	50 MHz	25 MHz
NG80960JS-33	33 MHz	33 MHz
NG80960JS-25	25 MHz	25 MHz
NG80960JD-66	66 MHz	33 MHz
NG80960JD-40	40 MHz	20 MHz
NG80960JA/JF-33	33 MHz	33 MHz
NG80960JA/JF-25	25 MHz	25 MHz
NG80960JA-16	16 MHz	16 MHz

For pinout diagrams of the PQFP package, see Section 3.2.3, “80960Jx 132-Lead PQFP Pinout” on page 27.

Extended temperature devices are specified for operation at V_{CC} = 3.3 V ± 0.15 V over a case temperature range of -40° C to 100° C. Table 5 presents 80960Jx processor versions that are available in the extended temperature 132-pin PQFP package and MPBGA package:

Table 5. 80960Jx Processors Available in Extended Temperature

Processor	Core Speed	Bus Speed	Package Type
TG80960JA-25	25 MHz	25 MHz	PQFP
TG80960JS-25	25 MHz	25 MHz	PQFP
TG80960JS-33	33 MHz	33 MHz	PQFP
TG80960JC-66	66 Mhz	33 MHz	PQFP
TG80960JT-100	100 MHz	33 MHz	PQFP
GD80960JC-66ET	66 MHz	33 MHz	MPBGA

The 196-ball Mini Plastic Ball Grid Array (MPBGA) device is specified for operation at V_{CC} = 3.3 V ± 0.15 V over a case temperature range of 0° C to 100° C. Table 6 presents the 80960Jx processor versions that are available in the 196-ball MPBGA package:

Table 6. 80960Jx Processors Available in 196-Ball MPBGA Package

Processor	Core Speed	Bus Speed
GD80960JT-100	100 MHz	33 MHz
GD80960JC-66	66 MHz	33 MHz
GD80960JS-33	33 MHz	33 MHz
GD80960JS-25	25 MHz	25 MHz
GD80960JD-50	50 MHz	25 MHz
GD80960JA/JF-33	33 MHz	33 MHz

For pinout diagrams of the PQFP package, see Section 3.2.4, “80960Jx 196-Ball MPBGA Pinout” on page 30.

For additional package specifications and information, refer to the *Intel Packaging Databook*, available in individual chapters, at http://www.intel.com.

3.2 Pin Descriptions

This section describes the pins for the 80960Jx processors. For a description of pin function, see Section 3.2.1, “Functional Pin Definitions” on page 16. Refer to the following sections for pinout information for the three package types:

- Section 3.2.2, “80960Jx 132-Lead PGA Pinout” on page 23.
- Section 3.2.3, “80960Jx 132-Lead PQFP Pinout” on page 27.
- Section 3.2.4, “80960Jx 196-Ball MPBGA Pinout” on page 30.

3.2.1 Functional Pin Definitions

Table 7 presents the legend for interpreting the three pin description tables that follow. These tables define the pins associated with the bus interface, basic control and test functions, and the Interrupt Unit.

Table 7. Pin Description Nomenclature

Symbol	Description
I	Input pin only.
O	Output pin only.
I/O	Pin may be either an input or output.
–	Pin must be connected as described.
S	Synchronous. Inputs must meet setup and hold times relative to CLKIN for proper operation. S(E) Edge sensitive input S(L) Level sensitive input
A (...)	Asynchronous. Inputs may be asynchronous relative to CLKIN. A(E) Edge sensitive input A(L) Level sensitive input
R (...)	While the processor's RESET# pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Q) is a valid output R(X) is driven to unknown state R(H) is pulled up to V_{CC}
H (...)	While the processor is in the hold state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Q) Maintains previous state or continues to be a valid output H(Z) Floats
P (...)	While the processor is halted, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Q) Maintains previous state or continues to be a valid output

Table 8. Pin Description—External Bus Signals (Sheet 1 of 4)

NAME	TYPE	DESCRIPTION
AD[31:0]	**I/O** S(L) R(X) H(Z) P(Q)	**ADDRESS / DATA BUS** carries 32-bit physical addresses and 8-, 16- or 32-bit data to and from memory. During an address (T_a) cycle, bits 31:2 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising AD[31:24], AD[23:16], AD[15:8] and AD[7:0]. During write operations, unused pins are driven to determinate values. SIZE, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction. AD1 AD0 Bus Transfers 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers When the processor enters Halt mode, if the previous bus operation was a: • write — AD[31:2] are driven with the last data value on the AD bus. • read — AD[31:4] are driven with the last address value on the AD bus; AD[3:2] are driven with the value of A[3:2] from the last data cycle. Typically, AD[1:0] reflect the SIZE information of the last bus transaction (either instruction fetch or load/store) that was executed before entering Halt mode.
ALE	**O** R(0) H(Z) P(0)	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).
ALE#	**O** R(1) H(Z) P(1)	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. ALE# is the inverted version of ALE. This signal gives the 80960Jx a high degree of compatibility with existing 80960Kx systems.
ADS#	**O** R(1) H(Z) P(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. The processor asserts ADS# for the entire T_a cycle. External bus control logic typically samples ADS# at the end of the cycle.
A[3:2]	**O** R(X) H(Z) P(Q)	**ADDRESS[3:2]** comprise a partial demultiplexed address bus. *32-bit memory accesses:* the processor asserts address bits A[3:2] during T_a. The partial word address increments with each assertion of RDYRCV# during a burst. *16-bit memory accesses:* the processor asserts address bits A[3:1] during T_a with A1 driven on the BE1# pin. The partial short word address increments with each assertion of RDYRCV# during a burst. *8-bit memory accesses:* the processor asserts address bits A[3:0] during T_a, with A[1:0] driven on BE[1:0]#. The partial byte address increments with each assertion of RDYRCV# during a burst.

Table 8. Pin Description—External Bus Signals (Sheet 2 of 4)

NAME	TYPE	DESCRIPTION
BE[3:0]#	**O** R(1) H(Z) P(1)	**BYTE ENABLES** select which of up to four data bytes on the bus participate in the current bus access. Byte enable encoding is dependent on the bus width of the memory region accessed: *32-bit bus:* BE3# enables data on AD[31:24] BE2# enables data on AD[23:16] BE1# enables data on AD[15:8] BE0# enables data on AD[7:0] *16-bit bus:* BE3# becomes Byte High Enable (enables data on AD[15:8]) BE2# is not used (state is high) BE1# becomes Address Bit 1 (A1) BE0# becomes Byte Low Enable (enables data on AD[7:0]) *8-bit bus:* BE3# is not used (state is high) BE2# is not used (state is high) BE1# becomes Address Bit 1 (A1) BE0# becomes Address Bit 0 (A0) The processor asserts byte enables, byte high enable and byte low enable during T_a. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during a burst. They remain active through the last T_d cycle. For accesses to 8- and 16-bit memory, the processor asserts the address bits in conjunction with A[3:2] described above.
WIDTH/ HLTD[1:0]	**O** R(0) H(Z) P(1)	**WIDTH/HALTED** signals denote the physical memory attributes for a bus transaction: WIDTH/ HLTD1 — WIDTH/ HLTD0 0 — 0 — 8 Bits Wide 0 — 1 — 16 Bits Wide 1 — 0 — 32 Bits Wide 1 — 1 — Processor Halted The processor floats the WIDTH/HLTD pins whenever it relinquishes the bus in response to a HOLD request, regardless of prior operating state.
D/C#	**O** R(X) H(Z) P(Q)	**DATA/CODE** indicates that a bus access is a data access (1) or an instruction access (0). D/C# has the same timing as W/R#. 0 = instruction access 1 = data access
W/R#	**O** R(0) H(Z) P(Q)	**WRITE/READ** specifies, during a T_a cycle, whether the operation is a write (1) or read (0). It is latched on-chip and remains valid during T_d cycles. 0 = read 1 = write
DT/R#	**O** R(0) H(Z) P(Q)	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the address/data bus. It is low during T_a and T_w/T_d cycles for a read; it is high during T_a and T_w/T_d cycles for a write. DT/R# never changes state when DEN# is asserted. 0 = receive 1 = transmit

Table 8. Pin Description—External Bus Signals (Sheet 3 of 4)

NAME	TYPE	DESCRIPTION
DEN#	**O** R(1) H(Z) P(1)	**DATA ENABLE** indicates data transfer cycles during a bus access. DEN# is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. DEN# is used with DT/R# to provide control for data transceivers connected to the data bus. 0 = data cycle 1 = not data cycle
BLAST#	**O** R(1) H(Z) P(1)	**BURST LAST** indicates the last transfer in a bus access. BLAST# is asserted in the last data transfer of burst and non-burst accesses. BLAST# remains active as long as wait states are inserted through the RDYRCV# pin. BLAST# becomes inactive after the final data transfer in a bus cycle. 0 = last data transfer 1 = not last data transfer
RDYRCV#	**I** S(L)	**READY/RECOVER** indicates that data on AD lines may be sampled or removed. When RDYRCV# is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w). 0 = sample data 1 = don't sample data The RDYRCV# pin has another function during the recovery (T_r) state. The processor continues to insert additional recovery states until it samples the pin HIGH. This function gives slow external devices more time to float their buffers before the processor begins to drive address again. 0 = insert wait states 1 = recovery complete
LOCK#/ ONCE#	**I/O** S(L) R(H) H(Z) P(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. The LOCK# output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant HOLDA while it is asserting LOCK#. This prevents external agents from accessing memory involved in semaphore operations. 0 = Atomic read-modify-write in progress 1 = Atomic read-modify-write not in progress **ONCE MODE:** The processor samples the ONCE# input during reset. When it is asserted LOW at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins. The pin has a weak internal pullup which is active during reset to ensure normal operation when the pin is left unconnected. 0 = ONCE mode enabled 1 = ONCE mode not enabled
HOLD	**I** S(L)	**HOLD**: A request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it asserts HOLDA, floats the address/data and control lines and enters the T_h state. When HOLD is deasserted, the processor deasserts HOLDA and enters either the T_i or T_a state, resuming control of the address/data and control lines. 0 = no hold request 1 = hold request

Table 8. Pin Description—External Bus Signals (Sheet 4 of 4)

NAME	TYPE	DESCRIPTION
HOLDA	**O** R(Q) H(1) P(Q)	**HOLD ACKNOWLEDGE** indicates to an external bus master that the processor has relinquished control of the bus. The processor may grant HOLD requests and enter the T_h state during reset and while halted as well as during regular operation. 0 = hold not acknowledged 1 = hold acknowledged
BSTAT	**O** R(0) H(Q) P(0)	**BUS STATUS** indicates that the processor may soon stall unless it has sufficient access to the bus; see *i960® Jx Microprocessor Developer's Manual* (272483). Arbitration logic may examine this signal to determine when an external bus master should acquire/relinquish the bus. 0 = no potential stall 1 = potential stall

Table 9. Pin Description—Processor Control Signals, Test Signals, and Power (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLKIN	**I**	**CLOCK INPUT** provides the processor's fundamental time base; both the processor core and the external bus run at the CLKIN rate. All input and output timings are specified relative to a rising CLKIN edge.
RESET#	**I** A(L)	**RESET** initializes the processor and clears its internal logic. During reset, the processor places the address/data bus and control output pins in their idle (inactive) states. During reset, the input pins are ignored with the exception of LOCK#/ONCE#, STEST and HOLD. The RESET# pin has an internal synchronizer. To ensure predictable processor initialization during power up, RESET# must be asserted a minimum of 10,000 CLKIN cycles with V_{CC} and CLKIN stable. On a warm reset, RESET# should be asserted for a minimum of 15 cycles.
STEST	**I** S(L)	**SELF TEST** enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of reset. When STEST is asserted, the processor performs its internal self-test and the external bus confidence test. When STEST is deasserted, the processor performs only the external bus confidence test. 0 = self test disabled 1 = self test enabled
FAIL#	**O** R(0) H(Q) P(1)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. FAIL# is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: • When self-test passes, the processor deasserts FAIL# and begins operation from user code. • When self-test fails, the processor asserts FAIL# and then stops executing. 0 = self test failed 1 = self test passed
TCK	**I**	**TEST CLOCK** is a CPU input which provides the clocking function for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the processor on the rising edge; data is clocked out of the processor on the falling edge.
TDI	**I** S(L)	**TEST DATA INPUT** is the serial input pin for JTAG. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port.

Table 9. Pin Description—Processor Control Signals, Test Signals, and Power (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
TDO	**O** R(Q) HQ) P(Q)	**TEST DATA OUTPUT** is the serial output pin for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats. TDO does not float during ONCE mode.
TRST#	**I** A(L)	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan testing (JTAG). When using the Boundary Scan feature, connect a pull-down resistor between this pin and V_{SS}. When TAP is not used, this pin must be connected to V_{SS}; however, no resistor is required. See Section 4.3, “Connection Recommendations” on page 36.
TMS	**I** S(L)	**TEST MODE SELECT** is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing.
V_{CC}	–	**POWER** pins intended for external connection to a V_{CC} board plane.
VCCPLL	–	**PLL POWER** is a separate V_{CC} supply pin for the phase lock loop clock generator. It is intended for external connection to the V_{CC} board plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
VCC5	–	**5 V REFERENCE VOLTAGE** input is the reference voltage for the 5 V-tolerant I/O buffers. This signal should be connected to +5 V for use with inputs which exceed 3.3 V. When all inputs are from 3.3 V components, this pin should be connected to 3.3 V.
V_{SS}	–	**GROUND** pins intended for external connection to a V_{SS} board plane.
NC	–	**NO CONNECT** pins. Do not make any system connections to these pins.

Table 10. Pin Description—Interrupt Unit Signals

NAME	TYPE	DESCRIPTION
XINT[7:0]#	**I** A(E/L)	**EXTERNAL INTERRUPT** pins are used to request interrupt service. The XINT[7:0]# pins may be configured in three modes: **Dedicated Mode**: Each pin is assigned a dedicated interrupt level. Dedicated inputs may be programmed to be level (low) or edge (falling) sensitive. **Expanded Mode**: All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode. **Mixed Mode**: The XINT[7:5]# pins act as dedicated sources and the XINT[4:0]# pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to 010_2 internally. Unused external interrupt pins should be connected to V_{CC}.
NMI#	**I** A(E)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. NMI# is the highest priority interrupt source and is falling edge-triggered. when NMI# is unused, it should be connected to V_{CC}.

3.2.2 80960Jx 132-Lead PGA Pinout

Figure 3. 132-Lead Pin Grid Array Top View-Pins Facing Down

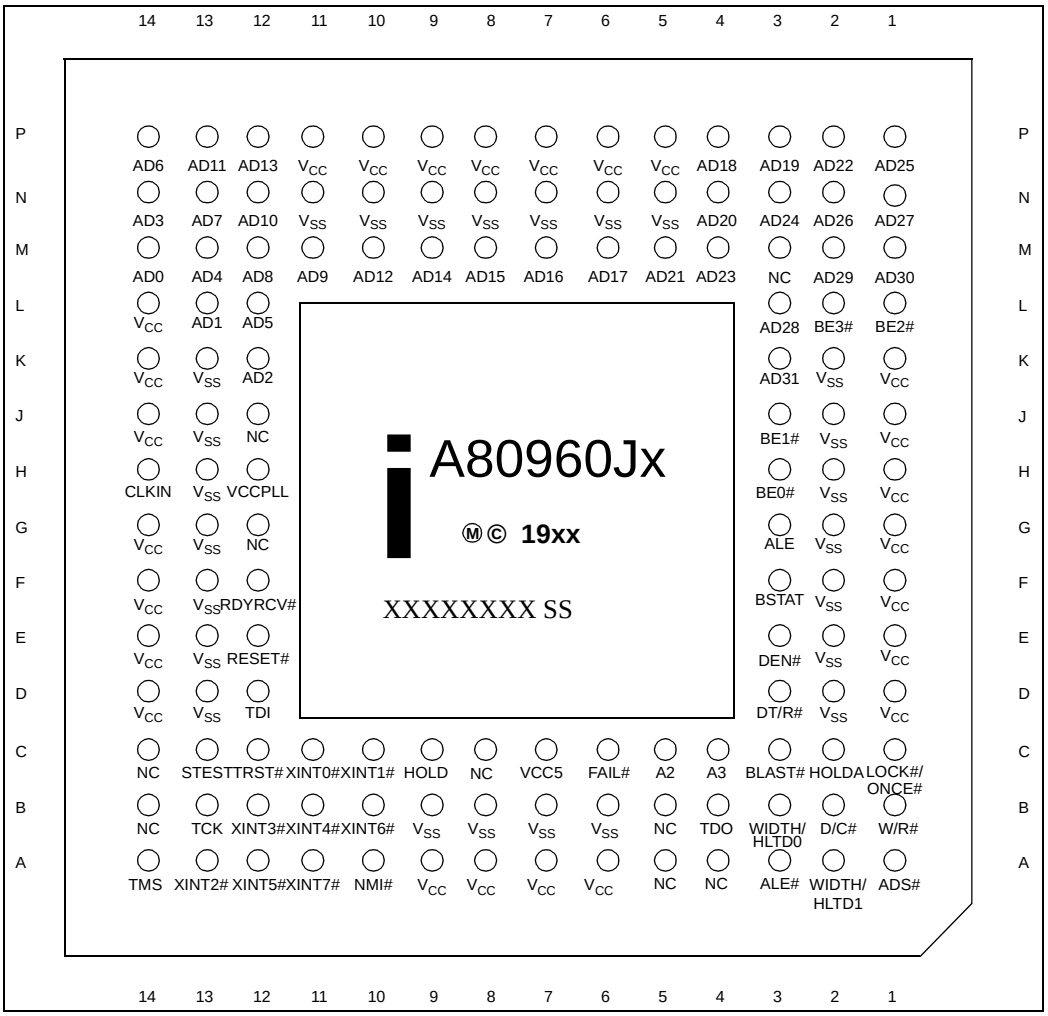


Figure 4. 132-Lead Pin Grid Array Bottom View-Pins Facing Up

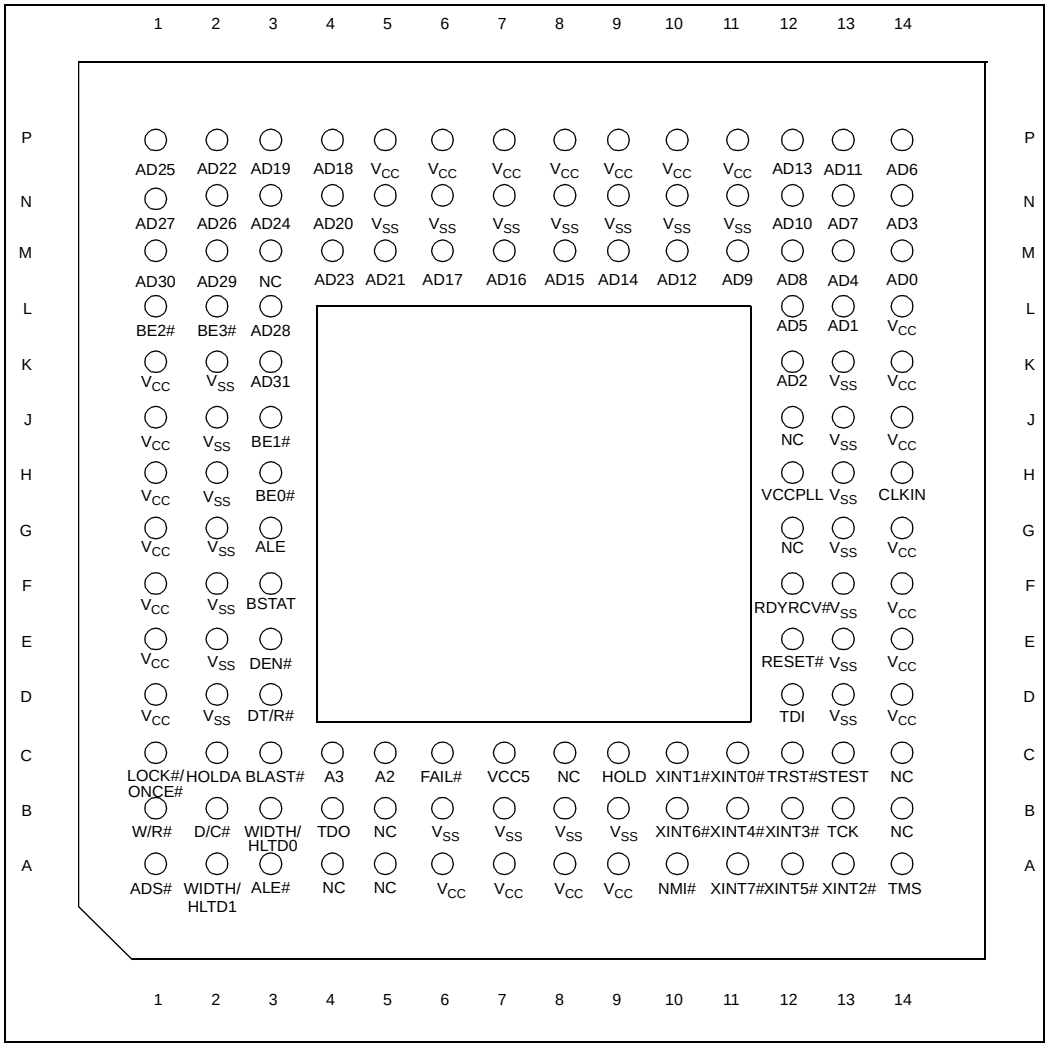


Table 11. 132-Lead PGA Pinout—In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	C5	**AD31**	K3	**TDO**	B4	**V_{SS}**	B9
A3	C4	**ADS#**	A1	**TMS**	A14	**V_{SS}**	D2
AD0	M14	**ALE**	G3	**TRST#**	C12	**V_{SS}**	D13
AD1	L13	**ALE#**	A3	**V_{CC}**	A6	**V_{SS}**	E2
AD2	K12	**BE0#**	H3	**V_{CC}**	A7	**V_{SS}**	E13
AD3	N14	**BE1#**	J3	**V_{CC}**	A8	**V_{SS}**	F2
AD4	M13	**BE2#**	L1	**V_{CC}**	A9	**V_{SS}**	F13
AD5	L12	**BE3#**	L2	**V_{CC}**	D1	**V_{SS}**	G2
AD6	P14	**BLAST#**	C3	**V_{CC}**	D14	**V_{SS}**	G13
AD7	N13	**BSTAT**	F3	**V_{CC}**	E1	**V_{SS}**	H2
AD8	M12	**CLKIN**	H14	**V_{CC}**	E14	**V_{SS}**	H13
AD9	M11	**D/C#**	B2	**V_{CC}**	F1	**V_{SS}**	J2
AD10	N12	**DEN#**	E3	**V_{CC}**	F14	**V_{SS}**	J13
AD11	P13	**DT/R#**	D3	**V_{CC}**	G1	**V_{SS}**	K2
AD12	M10	**FAIL#**	C6	**V_{CC}**	G14	**V_{SS}**	K13
AD13	P12	**HOLD**	C9	**V_{CC}**	H1	**V_{SS}**	N5
AD14	M9	**HOLDA**	C2	**V_{CC}**	J1	**V_{SS}**	N6
AD15	M8	**LOCK#/ONCE#**	C1	**V_{CC}**	J14	**V_{SS}**	N7
AD16	M7	**NC**	A4	**V_{CC}**	K1	**V_{SS}**	N8
AD17	M6	**NC**	A5	**V_{CC}**	K14	**V_{SS}**	N9
AD18	P4	**NC**	B5	**V_{CC}**	L14	**V_{SS}**	N10
AD19	P3	**NC**	B14	**V_{CC}**	P5	**V_{SS}**	N11
AD20	N4	**NC**	C8	**V_{CC}**	P6	**W/R#**	B1
AD21	M5	**NC**	C14	**V_{CC}**	P7	**WIDTH/HLTD0**	B3
AD22	P2	**NC**	G12	**V_{CC}**	P8	**WIDTH/HLTD1**	A2
AD23	M4	**NC**	J12	**V_{CC}**	P9	**XINT0#**	C11
AD24	N3	**NC**	M3	**V_{CC}**	P10	**XINT1#**	C10
AD25	P1	**NMI#**	A10	**V_{CC}**	P11	**XINT2#**	A13
AD26	N2	**RDYRCV#**	F12	**VCCPLL**	H12	**XINT3#**	B12
AD27	N1	**RESET#**	E12	**VCC5**	C7	**XINT4#**	B11
AD28	L3	**STEST**	C13	**V_{SS}**	B6	**XINT5#**	A12
AD29	M2	**TCK**	B13	**V_{SS}**	B7	**XINT6#**	B10
AD30	M1	**TDI**	D12	**V_{SS}**	B8	**XINT7#**	A11

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 12. 132-Lead PGA Pinout—In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	**ADS#**	C6	**FAIL#**	H1	**V_{CC}**	M10	**AD12**
A2	**WIDTH/HLTD1**	C7	**VCC5**	H2	**V_{SS}**	M11	**AD9**
A3	**ALE#**	C8	**NC**	H3	**BE0#**	M12	**AD8**
A4	**NC**	C9	**HOLD**	H12	**VCCPLL**	M13	**AD4**
A5	**NC**	C10	**XINT1#**	H13	**V_{SS}**	M14	**AD0**
A6	**V_{CC}**	C11	**XINT0#**	H14	**CLKIN**	N1	**AD27**
A7	**V_{CC}**	C12	**TRST#**	J1	**V_{CC}**	N2	**AD26**
A8	**V_{CC}**	C13	**STEST**	J2	**V_{SS}**	N3	**AD24**
A9	**V_{CC}**	C14	**NC**	J3	**BE1#**	N4	**AD20**
A10	**NMI#**	D1	**V_{CC}**	J12	**NC**	N5	**V_{SS}**
A11	**XINT7#**	D2	**V_{SS}**	J13	**V_{SS}**	N6	**V_{SS}**
A12	**XINT5#**	D3	**DT/R#**	J14	**V_{CC}**	N7	**V_{SS}**
A13	**XINT2#**	D12	**TDI**	K1	**V_{CC}**	N8	**V_{SS}**
A14	**TMS**	D13	**V_{SS}**	K2	**V_{SS}**	N9	**V_{SS}**
B1	**W/R#**	D14	**V_{CC}**	K3	**AD31**	N10	**V_{SS}**
B2	**D/C#**	E1	**V_{CC}**	K12	**AD2**	N11	**V_{SS}**
B3	**WIDTH/HLTD0**	E2	**V_{SS}**	K13	**V_{SS}**	N12	**AD10**
B4	**TDO**	E3	**DEN#**	K14	**V_{CC}**	N13	**AD7**
B5	**NC**	E12	**RESET#**	L1	**BE2#**	N14	**AD3**
B6	**V_{SS}**	E13	**V_{SS}**	L2	**BE3#**	P1	**AD25**
B7	**V_{SS}**	E14	**V_{CC}**	L3	**AD28**	P2	**AD22**
B8	**V_{SS}**	F1	**V_{CC}**	L12	**AD5**	P3	**AD19**
B9	**V_{SS}**	F2	**V_{SS}**	L13	**AD1**	P4	**AD18**
B10	**XINT6#**	F3	**BSTAT**	L14	**V_{CC}**	P5	**V_{CC}**
B11	**XINT4#**	F12	**RDYRCV#**	M1	**AD30**	P6	**V_{CC}**
B12	**XINT3#**	F13	**V_{SS}**	M2	**AD29**	P7	**V_{CC}**
B13	**TCK**	F14	**V_{CC}**	M3	**NC**	P8	**V_{CC}**
B14	**NC**	G1	**V_{CC}**	M4	**AD23**	P9	**V_{CC}**
C1	**LOCK#/ONCE#**	G2	**V_{SS}**	M5	**AD21**	P10	**V_{CC}**
C2	**HOLDA**	G3	**ALE**	M6	**AD17**	P11	**V_{CC}**
C3	**BLAST#**	G12	**NC**	M7	**AD16**	P12	**AD13**
C4	**A3**	G13	**V_{SS}**	M8	**AD15**	P13	**AD11**
C5	**A2**	G14	**V_{CC}**	M9	**AD14**	P14	**AD6**

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.2.3 80960Jx 132-Lead PQFP Pinout

Figure 5. 132-Lead PQFP - Top View

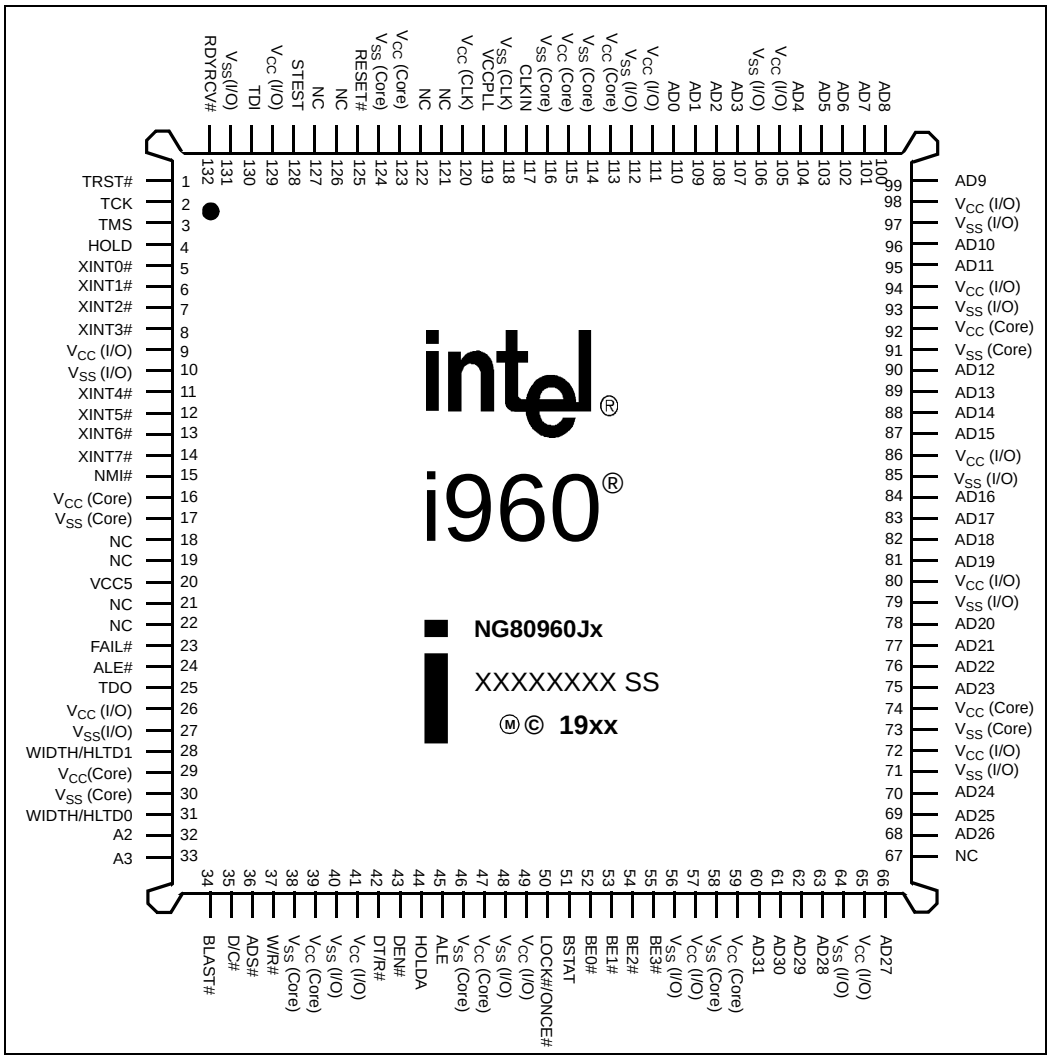


Table 13. 132-Lead PQFP Pinout—In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD31	60	ALE#	24	V_{CC} (Core)	47	V_{SS} (Core)	124
AD30	61	ADS#	36	V_{CC} (Core)	59	V_{SS} (I/O)	10
AD29	62	A3	33	V_{CC} (Core)	74	V_{SS} (I/O)	27
AD28	63	A2	32	V_{CC} (Core)	92	V_{SS} (I/O)	40
AD27	66	BE3#	55	V_{CC} (Core)	113	V_{SS} (I/O)	48
AD26	68	BE2#	54	V_{CC} (Core)	115	V_{SS} (I/O)	56
AD25	69	BE1#	53	V_{CC} (Core)	123	V_{SS} (I/O)	64
AD24	70	BE0#	52	V_{CC} (I/O)	9	V_{SS} (I/O)	71
AD23	75	WIDTH/HLTD1	28	V_{CC} (I/O)	26	V_{SS} (I/O)	79
AD22	76	WIDTH/HLTD0	31	V_{CC} (I/O)	41	V_{SS} (I/O)	85
AD21	77	D/C#	35	V_{CC} (I/O)	49	V_{SS} (I/O)	93
AD20	78	W/R#	37	V_{CC} (I/O)	57	V_{SS} (I/O)	97
AD19	81	DT/R#	42	V_{CC} (I/O)	65	V_{SS} (I/O)	106
AD18	82	DEN#	43	V_{CC} (I/O)	72	V_{SS} (I/O)	112
AD17	83	BLAST#	34	V_{CC} (I/O)	80	V_{SS} (I/O)	131
AD16	84	RDYRCV#	132	V_{CC} (I/O)	86	NC	18
AD15	87	LOCK#/ONCE#	50	V_{CC} (I/O)	94	NC	19
AD14	88	HOLD	4	V_{CC} (I/O)	98	NC	21
AD13	89	HOLDA	44	V_{CC} (I/O)	105	NC	22
AD12	90	BSTAT	51	V_{CC} (I/O)	111	NC	67
AD11	95	CLKIN	117	V_{CC} (I/O)	129	NC	121
AD10	96	RESET#	125	VCCPLL	119	NC	122
AD9	99	STEST	128	VCC5	20	NC	126
AD8	100	FAIL#	23	V_{SS} (CLK)	118	NC	127
AD7	101	TCK	2	V_{SS} (Core)	17	XINT7#	14
AD6	102	TDI	130	V_{SS} (Core)	30	XINT6#	13
AD5	103	TDO	25	V_{SS} (Core)	38	XINT5#	12
AD4	104	TRST#	1	V_{SS} (Core)	46	XINT4#	11
AD3	107	TMS	3	V_{SS} (Core)	58	XINT3#	8
AD2	108	V_{CC} (CLK)	120	V_{SS} (Core)	73	XINT2#	7
AD1	109	V_{CC} (Core)	16	V_{SS} (Core)	91	XINT1#	6
AD0	110	V_{CC} (Core)	29	V_{SS} (Core)	114	XINT0#	5
ALE	45	V_{CC} (Core)	39	V_{SS} (Core)	116	NMI#	15

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 14. 132-Lead PQFP Pinout—In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TRST#	34	BLAST#	67	NC	100	AD8
2	TCK	35	D/C#	68	AD26	101	AD7
3	TMS	36	ADS#	69	AD25	102	AD6
4	HOLD	37	W/R#	70	AD24	103	AD5
5	XINT0#	38	V_{SS} (Core)	71	V_{SS} (I/O)	104	AD4
6	XINT1#	39	V_{CC} (Core)	72	V_{CC} (I/O)	105	V_{CC} (I/O)
7	XINT2#	40	V_{SS} (I/O)	73	V_{SS} (Core)	106	V_{SS} (I/O)
8	XINT3#	41	V_{CC} (I/O)	74	V_{CC} (Core)	107	AD3
9	V_{CC} (I/O)	42	DT/R#	75	AD23	108	AD2
10	V_{SS} (I/O)	43	DEN#	76	AD22	109	AD1
11	XINT4#	44	HOLDA	77	AD21	110	AD0
12	XINT5#	45	ALE	78	AD20	111	V_{CC} (I/O)
13	XINT6#	46	V_{SS} (Core)	79	V_{SS} (I/O)	112	V_{SS} (I/O)
14	XINT7#	47	V_{CC} (Core)	80	V_{CC} (I/O)	113	V_{CC} (Core)
15	NMI#	48	V_{SS} (I/O)	81	AD19	114	V_{SS} (Core)
16	V_{CC} (Core)	49	V_{CC} (I/O)	82	AD18	115	V_{CC} (Core)
17	V_{SS} (Core)	50	LOCK#/ONCE#	83	AD17	116	V_{SS} (Core)
18	NC	51	BSTAT	84	AD16	117	CLKIN
19	NC	52	BE0#	85	V_{SS} (I/O)	118	V_{SS} (CLK)
20	VCC5	53	BE1#	86	V_{CC} (I/O)	119	VCCPLL
21	NC	54	BE2#	87	AD15	120	$V_{CC\ (CLK)}$
22	NC	55	BE3#	88	AD14	121	NC
23	FAIL#	56	V_{SS} (I/O)	89	AD13	122	NC
24	ALE#	57	V_{CC} (I/O)	90	AD12	123	V_{CC} (Core)
25	TDO	58	V_{SS} (Core)	91	V_{SS} (Core)	124	V_{SS} (Core)
26	V_{CC} (I/O)	59	V_{CC} (Core)	92	V_{CC} (Core)	125	RESET#
27	V_{SS} (I/O)	60	AD31	93	V_{SS} (I/O)	126	NC
28	WIDTH/HLTD1	61	AD30	94	V_{CC} (I/O)	127	NC
29	V_{CC} (Core)	62	AD29	95	AD11	128	STEST
30	V_{SS} (Core)	63	AD28	96	AD10	129	V_{CC} (I/O)
31	WIDTH/HLTD0	64	V_{SS} (I/O)	97	V_{SS} (I/O)	130	TDI
32	A2	65	V_{CC} (I/O)	98	V_{CC} (I/O)	131	V_{SS} (I/O)
33	A3	66	AD27	99	AD9	132	RDYRCV#

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.2.4 80960Jx 196-Ball MPBGA Pinout

Figure 6. 196-Ball Mini Plastic Ball Grid Array Top View-Balls Facing Down

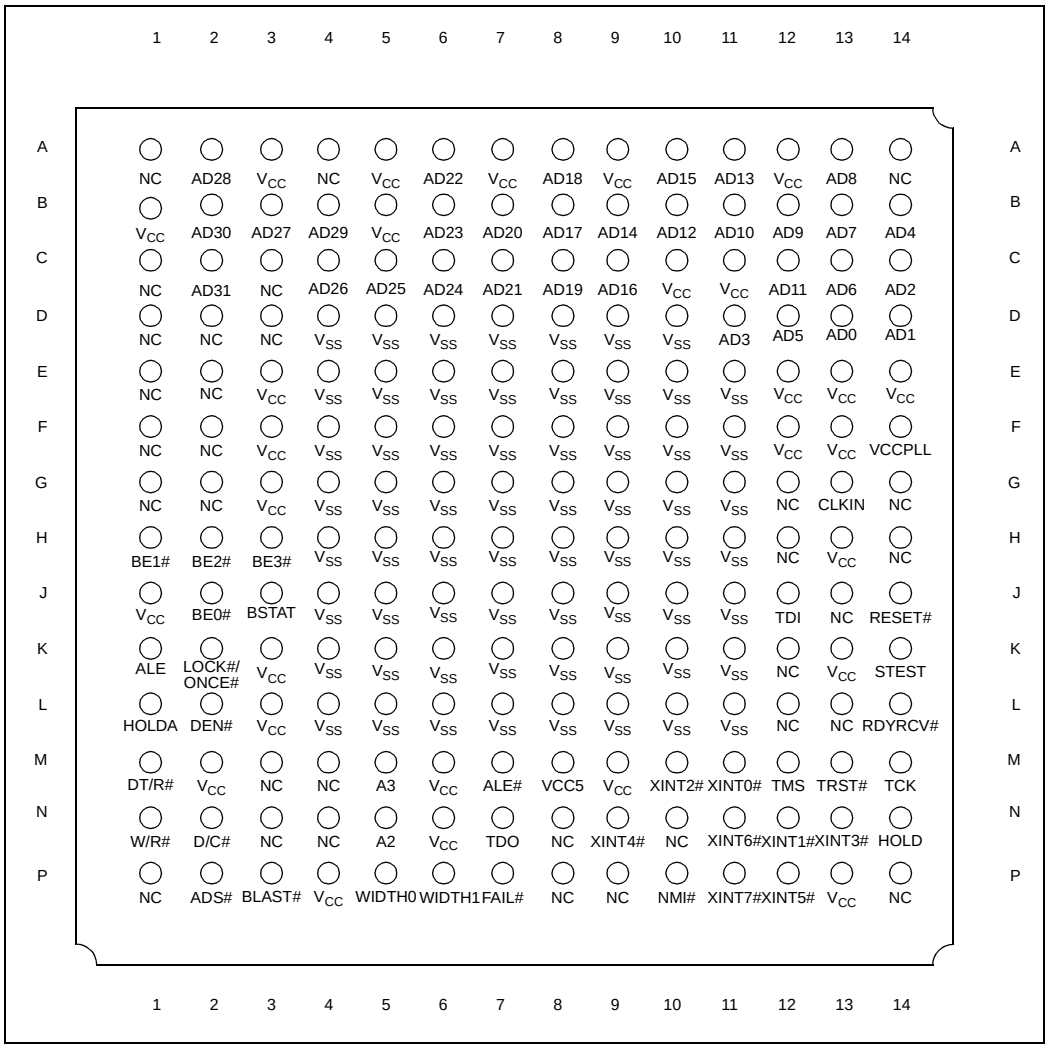


Figure 7. 196-Ball Mini Plastic Ball Grid Array Bottom View-Balls Facing Up

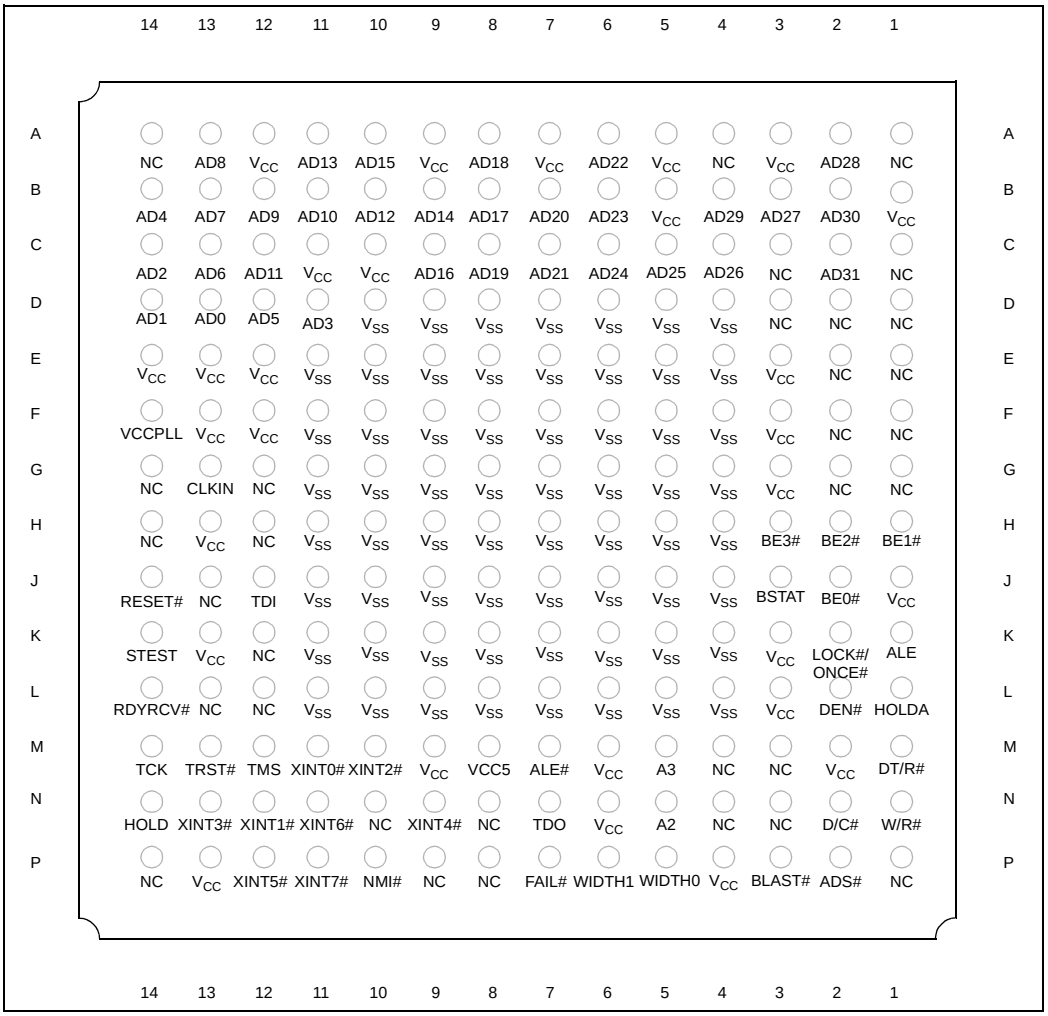


Table 15. 196-Ball MPBGA Pinout—In Signal Order (Sheet 1 of 2)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	N5	**BE0#**	J2	**NC**	M4	**V_{CC}**	J1
A3	M5	**BE1#**	H1	**NC**	N3	**V_{CC}**	K3
AD0	D13	**BE2#**	H2	**NC**	N4	**V_{CC}**	K13
AD1	D14	**BE3#**	H3	**NC**	N8	**V_{CC}**	L3
AD2	C14	**BLAST#**	P3	**NC**	N10	**V_{CC}**	M2
AD3	D11	**BSTAT**	J3	**NC**	P1	**V_{CC}**	M6
AD4	B14	**CLKIN**	G13	**NC**	P8	**V_{CC}**	M9
AD5	D12	**DEN#**	L2	**NC**	P9	**V_{CC}**	N6
AD6	C13	**D/C#**	N2	**NC**	P14	**V_{CC}**	P4
AD7	B13	**DT/R#**	M1	**NMI#**	P10	**V_{CC}**	P13
AD8	A13	**FAIL#**	P7	**RDYRCV#**	L14	**VCCPLL**	F14
AD9	B12	**HOLD**	N14	**RESET#**	J14	**V_{SS}**	D4
AD10	B11	**HOLDA**	L1	**STEST**	K14	**V_{SS}**	D5
AD11	C12	**LOCK#/ONCE#**	K2	**TCK**	M14	**V_{SS}**	D6
AD12	B10	**NC**	A1	**TDI**	J12	**V_{SS}**	D7
AD13	A11	**NC**	A4	**TDO**	N7	**V_{SS}**	D8
AD14	B9	**NC**	A14	**TMS**	M12	**V_{SS}**	D9
AD15	A10	**NC**	C1	**TRST#**	M13	**V_{SS}**	D10
AD16	C9	**NC**	C3	**VCC5**	M8	**V_{SS}**	E4
AD17	B8	**NC**	D1	**V_{CC}**	A3	**V_{SS}**	E5
AD18	A8	**NC**	D2	**V_{CC}**	A5	**V_{SS}**	E6
AD19	C8	**NC**	D3	**V_{CC}**	A7	**V_{SS}**	E7
AD20	B7	**NC**	E1	**V_{CC}**	A9	**V_{SS}**	E8
AD21	C7	**NC**	E2	**V_{CC}**	A12	**V_{SS}**	E9
AD22	A6	**NC**	F1	**V_{CC}**	B1	**V_{SS}**	E10
AD23	B6	**NC**	F2	**V_{CC}**	B5	**V_{SS}**	E11
AD24	C6	**NC**	G1	**V_{CC}**	C10	**V_{SS}**	F4
AD25	C5	**NC**	G2	**V_{CC}**	C11	**V_{SS}**	F5
AD26	C4	**NC**	G12	**V_{CC}**	E3	**V_{SS}**	F6
AD27	B3	**NC**	G14	**V_{CC}**	E12	**V_{SS}**	F7
AD28	A2	**NC**	H12	**V_{CC}**	E13	**V_{SS}**	F8
AD29	B4	**NC**	H14	**V_{CC}**	E14	**V_{SS}**	F9
AD30	B2	**NC**	J13	**V_{CC}**	F3	**V_{SS}**	F10
AD31	C2	**NC**	K12	**V_{CC}**	F12	**V_{SS}**	F11
ADS#	P2	**NC**	L12	**V_{CC}**	F13	**V_{SS}**	G4
ALE	K1	**NC**	L13	**V_{CC}**	G3	**V_{SS}**	G5
ALE#	M7	**NC**	M3	**V_{CC}**	H13	**V_{SS}**	G6

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 15. 196-Ball MPBGA Pinout—In Signal Order (Sheet 2 of 2)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VSS	G7	**V_{SS}**	H11	**V_{SS}**	K7	**V_{SS}**	L11
VSS	G8	**V_{SS}**	J4	**V_{SS}**	K8	**WIDTH0**	P5
VSS	G9	**V_{SS}**	J5	**V_{SS}**	K9	**WIDTH1**	P6
VSS	G10	**V_{SS}**	J6	**V_{SS}**	K10	**W/R#**	N1
VSS	G11	**V_{SS}**	J7	**V_{SS}**	K11	**XINT0#**	M11
VSS	H4	**V_{SS}**	J8	**V_{SS}**	L5	**XINT1#**	N12
VSS	H5	**V_{SS}**	J9	**V_{SS}**	L6	**XINT2#**	M10
VSS	H6	**V_{SS}**	J10	**V_{SS}**	L7	**XINT3#**	N13
VSS	H7	**V_{SS}**	J11	**V_{SS}**	L8	**XINT4#**	N9
VSS	H8	**V_{SS}**	K4	**V_{SS}**	L9	**XINT5#**	P12
VSS	H9	**V_{SS}**	K5	**V_{SS}**	L10	**XINT6#**	N11
VSS	H10	**V_{SS}**	K6	**V_{SS}**	L4	**XINT7#**	P11

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 16. 196-Ball MPBGA Pinout—In Pin Order (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	**NC**	C11	**V_{CC}**	F7	**V_{SS}**	J3	**BSTAT**
A2	**AD28**	C12	**AD11**	F8	**V_{SS}**	J4	**V_{SS}**
A3	**V_{CC}**	C13	**AD6**	F9	**V_{SS}**	J5	**V_{SS}**
A4	**NC**	C14	**AD2**	F10	**V_{SS}**	J6	**V_{SS}**
A5	**V_{CC}**	D1	**NC**	F11	**V_{SS}**	J7	**V_{SS}**
A6	**AD22**	D2	**NC**	F12	**V_{CC}**	J8	**V_{SS}**
A7	**V_{CC}**	D3	**NC**	F13	**V_{CC}**	J9	**V_{SS}**
A8	**AD18**	D4	**V_{SS}**	F14	**VCCPLL**	J10	**V_{SS}**
A9	**V_{CC}**	D5	**V_{SS}**	G1	**NC**	J11	**V_{SS}**
A10	**AD15**	D6	**V_{SS}**	G2	**NC**	J12	**TDI**
A11	**AD13**	D7	**V_{SS}**	G3	**V_{CC}**	J13	**NC**
A12	**V_{CC}**	D8	**V_{SS}**	G4	**V_{SS}**	J14	**RESET#**
A13	**AD8**	D9	**V_{SS}**	G5	**V_{SS}**	K1	**ALE**
A14	**NC**	D10	**V_{SS}**	G6	**V_{SS}**	K2	**LOCK#/ONCE#**
B1	**V_{CC}**	D11	**AD3**	G7	**V_{SS}**	K3	**V_{CC}**
B2	**AD30**	D12	**AD5**	G8	**V_{SS}**	K4	**V_{SS}**
B3	**AD27**	D13	**AD0**	G9	**V_{SS}**	K5	**V_{SS}**
B4	**AD29**	D14	**AD1**	G10	**V_{SS}**	K6	**V_{SS}**
B5	**V_{CC}**	E1	**NC**	G11	**V_{SS}**	K7	**V_{SS}**
B6	**AD23**	E2	**NC**	G12	**NC**	K8	V_{SS}

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 16. 196-Ball MPBGA Pinout—In Pin Order (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B7	**AD20**	E3	**V_{CC}**	G13	**CLKIN**	K9	**V_{SS}**
B8	**AD17**	E4	**V_{SS}**	G14	**NC**	K10	**V_{SS}**
B9	**AD14**	E5	**V_{SS}**	H1	**BE1#**	K11	**V_{SS}**
B10	**AD12**	E6	**V_{SS}**	H2	**BE2#**	K12	**NC**
B11	**AD10**	E7	**V_{SS}**	H3	**BE3#**	K13	**V_{CC}**
B12	**AD9**	E8	**V_{SS}**	H4	**V_{SS}**	K14	**STEST**
B13	**AD7**	E9	**V_{SS}**	H5	**V_{SS}**	L1	**HOLDA**
B14	**AD4**	E10	**V_{SS}**	H6	**V_{SS}**	L2	**DEN#**
C1	**NC**	E11	**V_{SS}**	H7	**V_{SS}**	L3	**V_{CC}**
C2	**AD31**	E12	**V_{CC}**	H8	**V_{SS}**	L4	**V_{SS}**
C3	**NC**	E13	**V_{CC}**	H9	**V_{SS}**	L5	**V_{SS}**
C4	**AD26**	E14	**V_{CC}**	H10	**V_{SS}**	L6	**V_{SS}**
C5	**AD25**	F1	**NC**	H11	**V_{SS}**	L7	**V_{SS}**
C6	**AD24**	F2	**NC**	H12	**NC**	L8	**V_{SS}**
C7	**AD21**	F3	**V_{CC}**	H13	**V_{CC}**	L9	**V_{SS}**
C8	**AD19**	F4	**V_{SS}**	H14	**NC**	L10	**V_{SS}**
C9	**AD16**	F5	**V_{SS}**	J1	**V_{CC}**	L11	**V_{SS}**
C10	**V_{CC}**	F6	**V_{SS}**	J2	**BE0#**	L12	**NC**
L13	**NC**	M10	**XINT2#**	N7	**TDO**	P4	**V_{CC}**
L14	**RDYRCV#**	M11	**XINT0#**	N8	**NC**	P5	**WIDTH0**
M1	**DT/R#**	M12	**TMS**	N9	**XINT4#**	P6	**WIDTH1**
M2	**V_{CC}**	M13	**TRST#**	N10	**NC#**	P7	**FAIL#**
M3	**NC**	M14	**TCK**	N11	**XINT6#**	P8	**NC**
M4	**NC**	N1	**W/R#**	N12	**XINT1#**	P9	**NC**
M5	**A3**	N2	**D/C#**	N13	**XINT3#**	P10	**NMI#**
M6	**V_{CC}**	N3	**NC**	N14	**HOLD**	P11	**XINT7#**
M7	**ALE#**	N4	**NC**	P1	**NC**	P12	**XINT5#**
M8	**VCC5**	N5	**A2**	P2	**ADS#**	P13	**V_{CC}**
M9	**V_{CC}**	N6	**V_{CC}**	P3	**BLAST#**	P14	**NC**

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

This document contains information on products in the production phase of development. The specifications within this datasheet are subject to change without prior notice. Verify with your local Intel sales office or the world wide web to ensure that you have the latest datasheet and device specification update before finalizing a design.

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Table 17 presents the absolute maximum ratings.

Table 17. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65° C to +150° C
Case Temperature Under Bias	–65° C to +110° C
Supply Voltage wrt. V_{SS}	–0.5 V to + 4.6 V
Voltage on VCC5 wrt. V_{SS}	–0.5 V to + 6.5 V
Voltage on Other Pins wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

4.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 18 presents the operating conditions for the 80960Jx 3.3 V processors.

Table 18. 80960Jx Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.15	3.45	V	
VCC5	Input Protection Bias	3.15	5.5	V	(†)
f_{CLKIN}	Input Clock Frequency			MHz	
	80960JT-100	15	33.3		
	80960JC-66	15	33.3		
	80960JC-50	15	25		
	80960JS-33	15	33		
	80960JS-25	15	25		
	80960JD-66	12	33.3		
	80960JD-50	12	25		
	80960JD-40	12	20		
	80960JD-33	12	16.67		
	80960JA/JF-33	12	33.3		
	80960JA/JF-25	12	25		
	80960JA-16	12	16		
T_C	Operating Case Temperature			°C	
	PGA, MPBGA, and PQFP	0	100		
	Extended temp PQFP and MPBGA	-40	100		

† See Section 4.4, “VCC5 Pin Requirements (VDIFF)” on page 36.

4.3 Connection Recommendations

For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960Jx power and ground pins. On the circuit board, every V_{CC} pin should connect to a power plane and every V_{SS} pin should connect to a ground plane. Place liberal decoupling capacitance near the 80960Jx, since the processor may cause transient power surges.

The 80960JS/JC/JT processors are produced on Intel's advanced CMOS process. Proper bulk decoupling must be used to prevent device damage during initial power up and during transitions from low power mode to normal processor operation. Power supply behavior during these transitions may cause the power supply to exceed the maximum V_{CC} specification and may cause device damage.

Pay special attention to the Test Reset (TRST#) pin. It is essential that the JTAG Boundary Scan Test Access Port (TAP) controller initializes to a known state whether it may be used or not. When the JTAG Boundary Scan function may be used, connect a pull-down resistor between the TRST# pin and V_{SS}. When the JTAG Boundary Scan function may not be used (even for board-level testing), connect the TRST# pin to V_{SS}.

Do not connect the TDI, TDO, and TCK pins when the TAP Controller may not be used.

Note: Pins identified as NC must not be connected in the system.

4.4 VCC5 Pin Requirements (VDIFF)

In 3.3 V only systems where the 80960Jx input pins are driven from 3.3 V logic, connect the VCC5 pin directly to the 3.3 V V_{CC} plane.

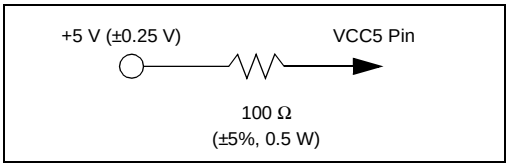
In mixed voltage systems where the processor is powered by 3.3 V and interfaces with 5 V components, VCC5 must be connected to 5 V. This allows proper 5 V tolerant buffer operation, and prevents damage to the input pins. The voltage differential between the 80960Jx VCC5 pin and its 3.3 V V_{CC} pins must not exceed 2.25 V. When this requirement is not met, current flow through the pin may exceed the value at which the processor is damaged. Instances when the voltage may exceed 2.25 V is during power up or power down, where one source reaches its level faster than the other, briefly causing an excess voltage differential. Another instance is during steady-state operation, where the differential voltage of the regulator (provided a regulator is used) cannot be maintained within 2.25 V. Two methods are possible to prevent this from happening:

- Use a regulator that is designed to prevent the voltage differential from exceeding 2.25 V.

  or:

- As shown in Figure 8, place a 100 Ω resistor in series with the VCC5 pin to limit the current through VCC5.

Figure 8. VCC5 Current-Limiting Resistor



When the regulator cannot prevent the 2.25 V differential, the addition of the resistor is a simple and reliable method for limiting current. The resistor may also prevent damage in the case of a power failure, where the 5 V supply remains on and the 3.3 V supply goes to zero.

Table 19. VDIFF Parameters

Symbol	Parameter	Min	Max	Units	Notes
VDIFF	VCC5-V_{CC} Difference		2.25	V	VCC5 input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation.

4.5 VCCPLL Pin Requirements

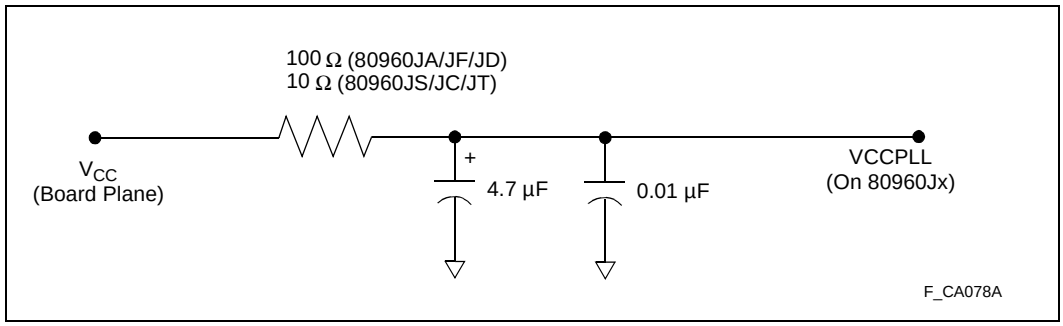
To reduce clock skew on the 80960Jx processor, the VCCPLL pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, as shown in Figure 9, reduces noise induced clock jitter and its effects on timing relationships in system designs. The 4.7 µF capacitor must be low ESR solid tantalum; the 0.01 µF capacitor must be of the type X7R and the node connecting VCCPLL must be as short as possible.

When the voltage on the VCCPLL power supply pin exceeds the V_{CC} pin voltage by 0.5 V at any time, including the power up and power down sequences, excessive currents may permanently damage on-chip electrostatic discharge (ESD) protection diodes. The damage may accumulate over multiple episodes.

In actual applications, this problem occurs only when the VCCPLL and V_{CC} pins are driven by separate power supplies or voltage regulators. Applications that use one power supply for VCCPLL and V_{CC} are not typically at risk. Verify that your application does not allow the VCCPLL voltage to exceed V_{CC} by 0.5 V.

The VCCPLL low-pass filter recommendation does not promote this problem.

Figure 9. VCCPLL Lowpass Filter



4.6 D.C. Specifications

Table 20. 80960Jx D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC5} + 0.3	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -1 mA
V_{OLP}	Output Ground Bounce		<0.8		V	(1,2)
C_{IN}	Input Capacitance PGA PQFP MPBGA			 15 15 15	pF	$f_{CLKIN} = f_{MIN}$ (2)
C_{OUT}	I/O or Output Capacitance PGA PQFP MPBGA			 15 15 15	pF	$f_{CLKIN} = f_{MIN}$ (2)
C_{CLK}	CLKIN Capacitance PGA PQFP MPBGA			 15 15 15	pF	$f_{CLKIN} = f_{MIN}$ (2)

NOTES:
1. Typical is measured with V_{CC} = 3.3 V and temperature = 25°C.
2. Not tested.

Table 21. 80960Jx I_{CC} Characteristics (Sheet 1 of 3)

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each pin except TCK, TDI, TRST# and TMS		± 1	µA	$0 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current for TCK, TDI, TRST# and TMS 80960 JA/JF/JD 80960 JS/JC/JT	 -140 -250	 -250 -300	µA	V_{IN} = 0.45V (1)
I_{LO}	Output Leakage Current		± 1	µA	$0.4 \le V_{OUT} \le V_{CC}$
R_{pu}	Internal Pull-UP Resistance for ONCE#, TMS, TDI and TRST#	20	30	kΩ	
I_{CC} Active (Power Supply)	80960JT-100 80960JC-66 80960JC-50 80960JS-33 80960JS-25 80960JD-66 80960JD-50 80960JD-40 80960JD-33 80960JA/JF-33 80960JA/JF-25 80960JA-16		505 360 280 240 185 580 447 367 310 320 241 154	mA	(2,3)
I_{CC} Active (Thermal)	80960JT-100 80960JC-66 80960JC-50 80960JS-33 80960JS-25 80960JD-66 80960JD-50 80960JD-40 80960JD-33 80960JA/JF-33 80960JA/JF-25 80960JA-16	480 345 270 221 170 510 390 320 260 271 215 152		mA	(2,4)

Table 21. 80960Jx I_{CC} Characteristics (Sheet 2 of 3)

Symbol	Parameter	Typ	Max	Units	Notes
I_{CC} Test (Power modes)	Reset mode			mA	(5)
	80960JT-100		380		
	80960JC-66		275		
	80960JC-50		210		
	80960JS-33		240		
	80960JS-25		182		
	80960JD-66		475		
	80960JD-50		425		
	80960JD-40		345		
	80960JD-33		300		
	80960JA/JF-33		250		
	80960JA/JF-25		200		
	80960JA-16		150		
	Halt mode				
	80960JT-100		52		
	80960JC-66		45		
	80960JC-50		34		
	80960JS-33		35		
	80960JS-25		30		
	80960JD-66		50		
	80960JD-50		40		
	80960JD-40		34		
	80960JD-33		29		
	80960JA/JF-33		31		
	80960JA/JF-25		26		
	80960JA-16		21		
	ONCE mode		10		

Table 21. 80960Jx I_{CC} Characteristics (Sheet 3 of 3)

Symbol	Parameter	Typ	Max	Units	Notes
ICC5 Current on the **VCC5** Pin	80960JT-100 80960JC-66 80960JC-50 80960JS-33 80960JS-25 80960JD-66 80960JD-50 80960JD-40 80960JD-33 80960JA/JF-33 80960JA/JF-25 80960JA-16		200	µA	(6)

NOTES:
1. These pins have internal pullup devices. Typical leakage current is not tested.
2. Measured with device operating and outputs loaded to the test condition in Figure 10, “A.C. Test Load” on page 45.
3. I_{CC} Active (Power Supply) value is provided for selecting your system’s power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.45 V. This parameter is characterized but not tested.
4. I_{CC} Active (Thermal) value is provided for your system’s thermal management. Typical I_{CC} is measured with V_{CC} =3.3 V and temperature = 25° C. This parameter is characterized but not tested.
5. I_{CC} Test (Power modes) refers to the I_{CC} values that are tested when the 80960JD is in Reset mode, Halt mode or ONCE mode with V_{CC} = 3.45 V.
6. I_{CC5} is tested at V_{CC} = 3.3 V, VCC5 = 5.25 V.

4.7 A.C. Specifications

The 80960Jx A.C. timings are based upon device characterization.

Table 22. 80960Jx A.C. Characteristics (Sheet 1 of 3)

Symbol	Parameter	Min	Max	Unit	Notes
	Input Clock Timings				
T_F	CLKIN Frequency			MHz	
	80960JT-100	15	33.3		
	80960JC-66	15	33.3		
	80960JC-50	15	25		
	80960JS-33	15	33.3		
	80960JS-25	15	25		
	80960JD-66	12	33.3		
	80960JD-50	12	25		
	80960JD-40	12	20		
	80960JD-33	12	16.67		
	80960JA/JF-33	12	33.3		
	80960JA/JF-25	12	25		
	80960JA-16	12	16		
T_C	CLKIN Period			ns	
	80960JT-100	30	66.7		
	80960JC-66	30	66.7		
	80960JC-50	40	66.7		
	80960JS-33	30	66.7		
	80960JS-25	40	66.7		
	80960JD-66	30	83.3		
	80960JD-50	40	83.3		
	80960JD-40	50	83.3		
	80960JD-33	60	83.3		
	80960JA/JF-33	30	83.3		
	80960JA/JF-25	40	83.3		
	80960JA-16	62.5	83.3		
T_{CS}	CLKIN Period Stability		± 250	ps	(1, 2)
T_{CH}	CLKIN High Time	8		ns	Measured at 1.5 V (1)
T_{CL}	CLKIN Low Time	8		ns	Measured at 1.5 V (1)
T_{CR}	CLKIN Rise Time		4	ns	0.8 V to 2.0 V (1)
T_{CF}	CLKIN Fall Time		4	ns	2.0 V to 0.8 V (1)

NOTE: See Table 23 on page 45 for note definitions for this table.

Table 22. 80960Jx A.C. Characteristics (Sheet 2 of 3)

Symbol	Parameter	Min	Max	Unit	Notes
	Synchronous Output Timings				
T_{OV1}	Output Valid Delay, Except ALE/ALE# Inactive and DT/R# for 3.3 V input signals Same as above, but for 5.5 V input signals **Extended Temp MPBGA and PQFP (JS/JC/JT only):** Output Valid Delay, Except ALE/ALE# Inactive and DT/R# for 3.3 V input signals Same as above, but for 5.5 V input signals	2.5 2.5 1.75 1.75	13.5 16.5 13.5 16.5	ns	(2, 11)
T_{OV2}	Output Valid Delay, DT/R# 80960JS/JC/JT 80960JD 80960JA/JF	 $0.5T_C + 7$ $0.5T_C + 7$ $0.5T_C + 4$	 $0.5T_C + 9$ $0.5T_C + 9$ $0.5T_C + 18$	ns	
T_{OF}	Output Float Delay	2.5	13.5	ns	(4)
	Synchronous Input Timings				
T_{IS1}	Input Setup to CLKIN — AD[31:0], NMI#, XINT[7:0]# 80960JS/JC/JT 80960JD 80960JA/JF	 6 6 9		ns	(5)
T_{IH1}	Input Hold from CLKIN — AD[31:0], NMI#, XINT[7:0]# 80960JS/JC/JT 80960JD 80960JA/JF	 2.0 1.5 1.0		ns	(5)
T_{IS2}	Input Setup to CLKIN — RDYRCV# and HOLD 80960JS/JC/JT 80960JD 80960JA/JF	 6.5 6.5 10.0		ns	(6)
T_{IH2}	Input Hold from CLKIN — RDYRCV# and HOLD	1		ns	(6)
T_{IS3}	Input Setup to CLKIN — RESET# 80960JS/JC/JT 80960JD 80960JA/JF	 7 7 8		ns	(7)
T_{IH3}	Input Hold from CLKIN — RESET# 80960JS/JC/JT 80960JD 80960JA/JF	 2 2 1		ns	(7)
T_{IS4}	Input Setup to RESET# — ONCE#, STEST 80960JS/JC/JT 80960JD 80960JA/JF	 7 7 8		ns	(8)

NOTE: See Table 23 on page 45 for note definitions for this table.

Table 22. 80960Jx A.C. Characteristics (Sheet 3 of 3)

Symbol	Parameter	Min	Max	Unit	Notes
T_{IH4}	Input Hold from RESET# — ONCE#, STEST 80960JS/JC/JT 80960JD 80960JA/JF	 2 2 1		ns	(8)
Relative Output Timings					
T_{LX}	Address Valid to ALE/ALE# Inactive For 3.3 V Data Input Signals For 5.0 V Data Input Signals	 $0.5T_C$ - 5 $0.5T_C$ - 8		ns	(9)
T_{LXL}	ALE/ALE# Width	$0.5T_C$ - 7		ns	Equal Loading (9)
T_{LXA}	Address Hold from ALE/ALE# Inactive				
T_{DXD}	DT/R# Valid to DEN# Active				
Boundary Scan Test Signal Timings					
T_{BSF}	TCK Frequency		$0.5T_F$	MHz	
T_{BSCH}	TCK High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	4		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	6		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	(1, 10)
T_{BSOF1}	TDO Float Delay	3	30	ns	(1, 10)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	(1, 10)
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	30	ns	(1, 10)
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	4		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	6		ns	

NOTE: See Table 23 on page 45 for note definitions for this table.

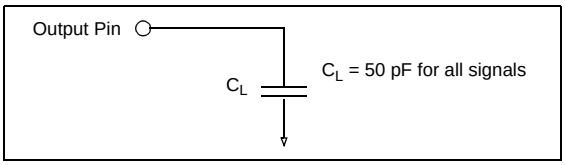
Table 23. Note Definitions for Table 22, 80960Jx AC Characteristics

NOTES:
1. Not tested.
2. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal clock, the jitter frequency spectrum should not have any power peaking between 500 KHz and 1/3 of the CLKIN frequency.
3. Inactive ALE/ALE# refers to the falling edge of ALE and the rising edge of ALE#. For inactive ALE/ALE# timings, refer to Relative Output Timings in this table.
4. A float condition occurs when the output current becomes less than I_{OL}. Float delay is not tested, but is designed to be no longer than the valid delay.
5. AD[31:0] are synchronous inputs. Setup and hold times must be met for proper processor operation. NMI# and XINT[7:0]# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, NMI# and XINT[7:0]# must be asserted for a minimum of two CLKIN periods to ensure recognition.
6. RDYRCV# and HOLD are synchronous inputs. Setup and hold times must be met for proper processor operation.
7. RESET# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
8. ONCE# and STEST# must be stable at the rising edge of RESET# for proper operation.
9. Guaranteed by design. May not be 100% tested.
10. Relative to falling edge of TCK.
11. Worst-case T_{OV} condition occurs on I/O pins when pins transition from a floating high input to driving a low output state. The Address/Data Bus pins encounter this condition between the last access of a read, and the address cycle of a following write. 5 V signals take 3 ns longer to discharge than 3.3 V signals at 50 pF loads.

4.7.1 A.C. Test Conditions and Derating Curves

The A.C. Specifications in Section 4.7, “A.C. Specifications” are tested with the 50 pF load indicated in Figure 10.

Figure 10. A.C. Test Load



Refer to the following sections for the specified derating curves:

- Section 4.7.1.1, “Output Delay or Hold vs. Load Capacitance” on page 46
- Section 4.7.1.2, “TLX vs. AD Bus Load Capacitance” on page 47

4.7.1.1 Output Delay or Hold vs. Load Capacitance

Figure 11. Output Delay or Hold vs. Load Capacitance–80960JS/JC/JT (3.3 V Signals)

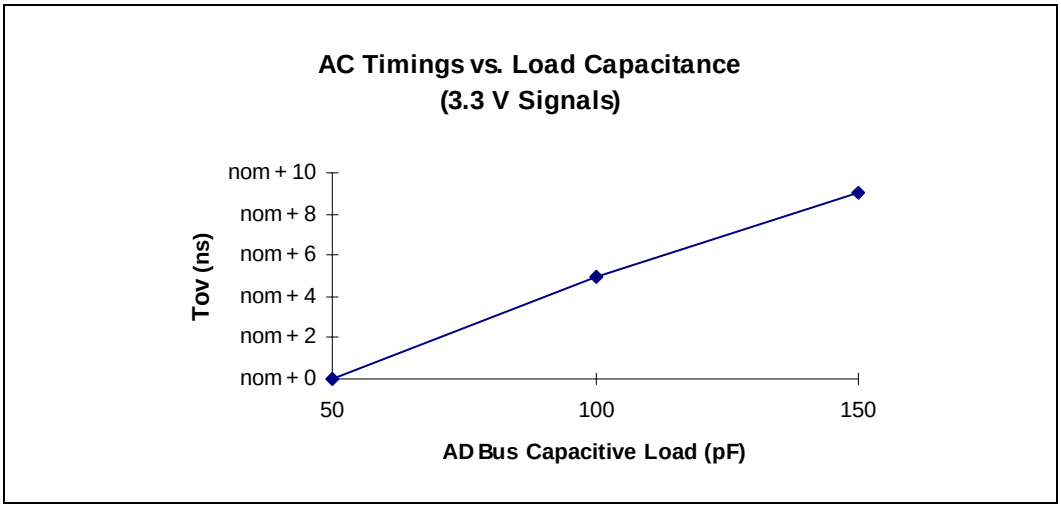


Figure 12. Output Delay or Hold vs. Load Capacitance–80960JS/JC/JT (5 V Signals)

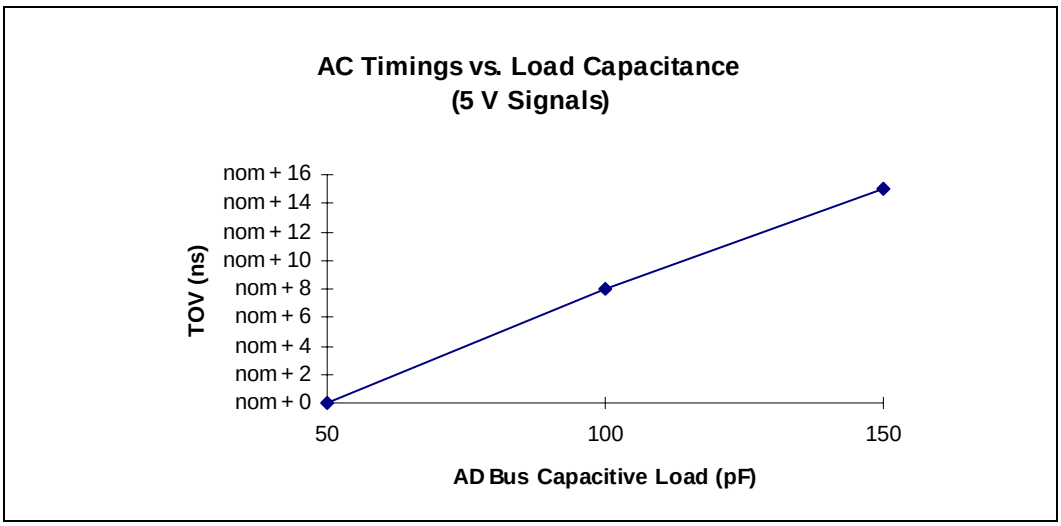
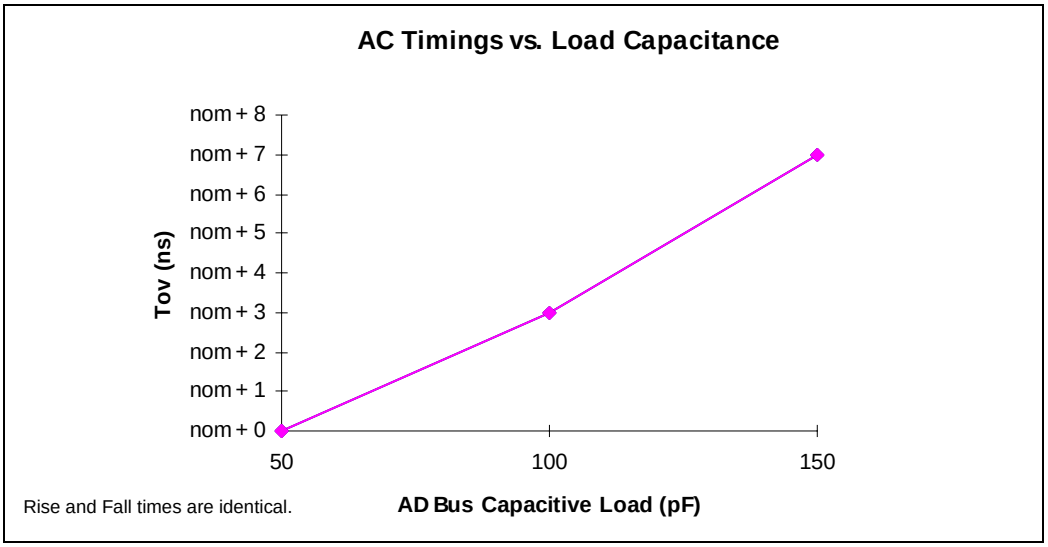
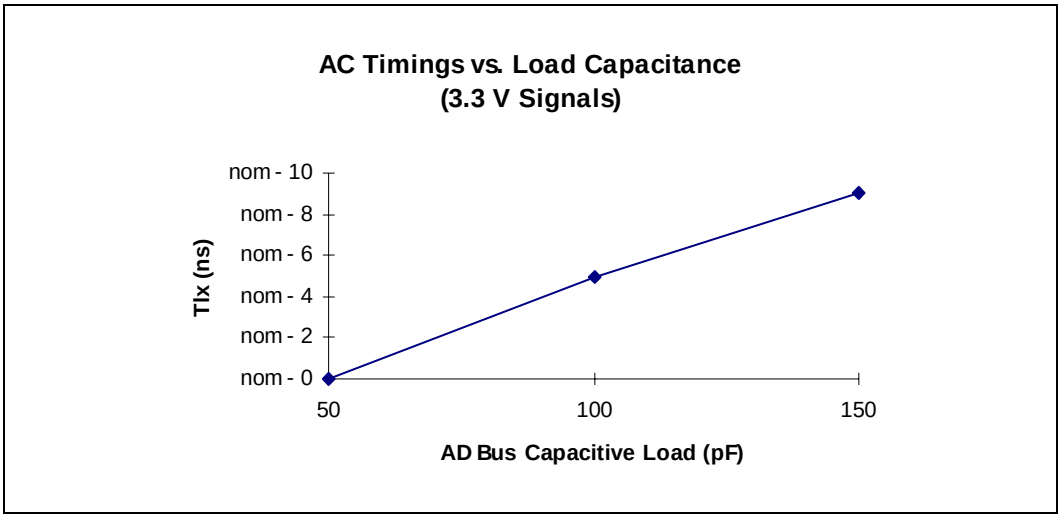


Figure 13. Output Delay or Hold vs. Load Capacitance–80960JA/JF/JD



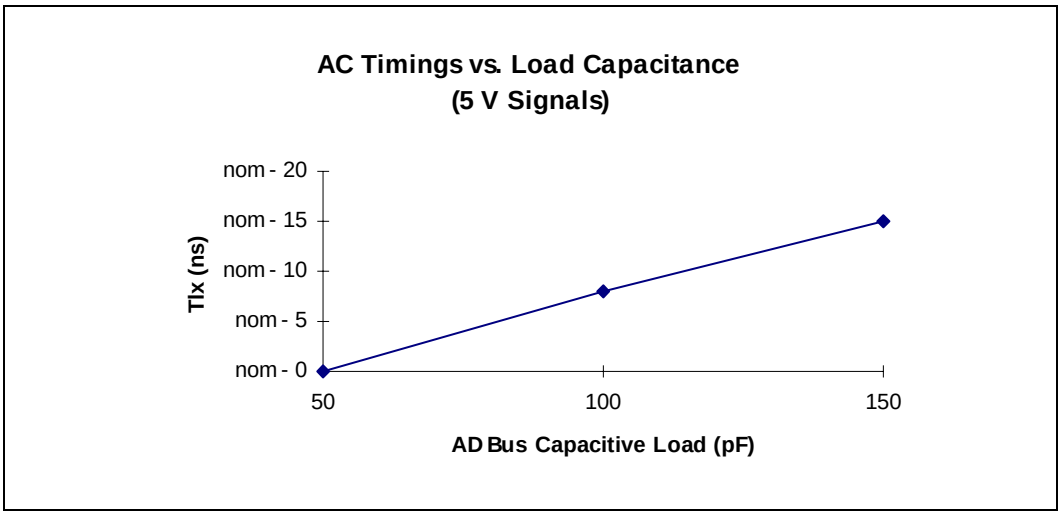
4.7.1.2 T_{LX} vs. AD Bus Load Capacitance

Figure 14. T_{LX} vs. AD Bus Load Capacitance–80960JS/JC/JT (3.3 V Signals)



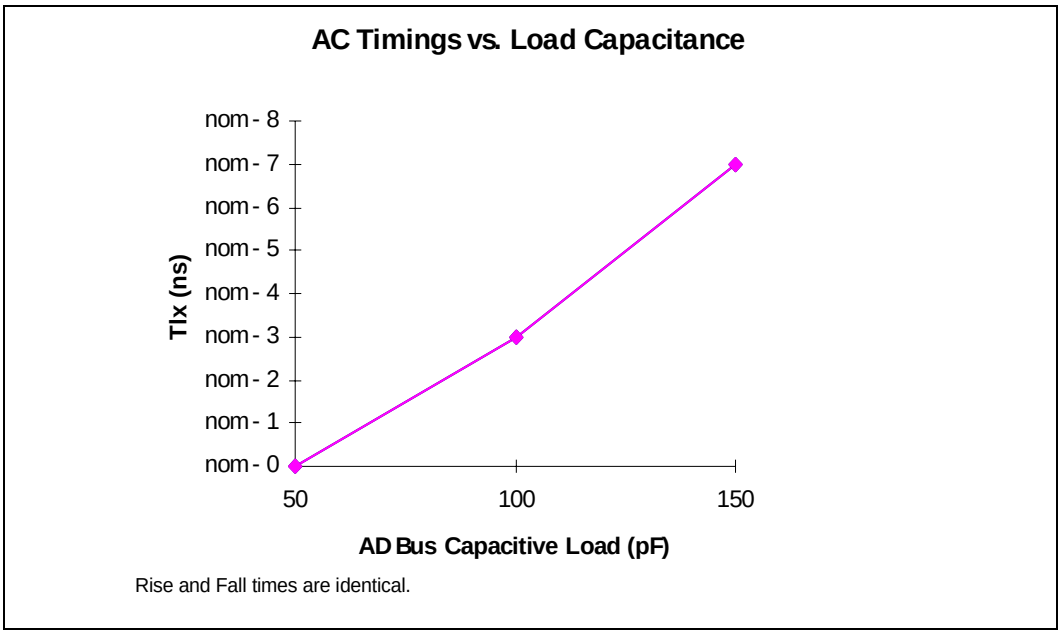
Note: The T_{LX} Derating curve applies only when an imbalance in the capacitive load occurs between the AD bus and ALE. The T_{LX} derating is based on a 50 pF load on ALE. The derating applies to ALE and ALE#.

Figure 15. T_{LX} vs. AD Bus Load Capacitance–80960JS/JC/JT (5 V Signals)



Note: The T_{LX} Derating curve applies only when an imbalance in the capacitive load occurs between the AD bus and ALE. The T_{LX} derating is based on a 50 pF load on ALE. The derating applies to ALE and ALE#.

Figure 16. T_{LX} vs. AD Bus Load Capacitance–80960JA/JF/JD



Note: The T_{LX} Derating curve applies only when an imbalance in the capacitive load occurs between the AD bus and ALE. The T_{LX} derating is based on a 50 pF load on ALE. The derating applies to ALE and ALE#.

4.7.1.3 ICC Active vs. Frequency

Figure 17. I_{CC} Active (Power Supply) vs. Frequency–80960JA/JF

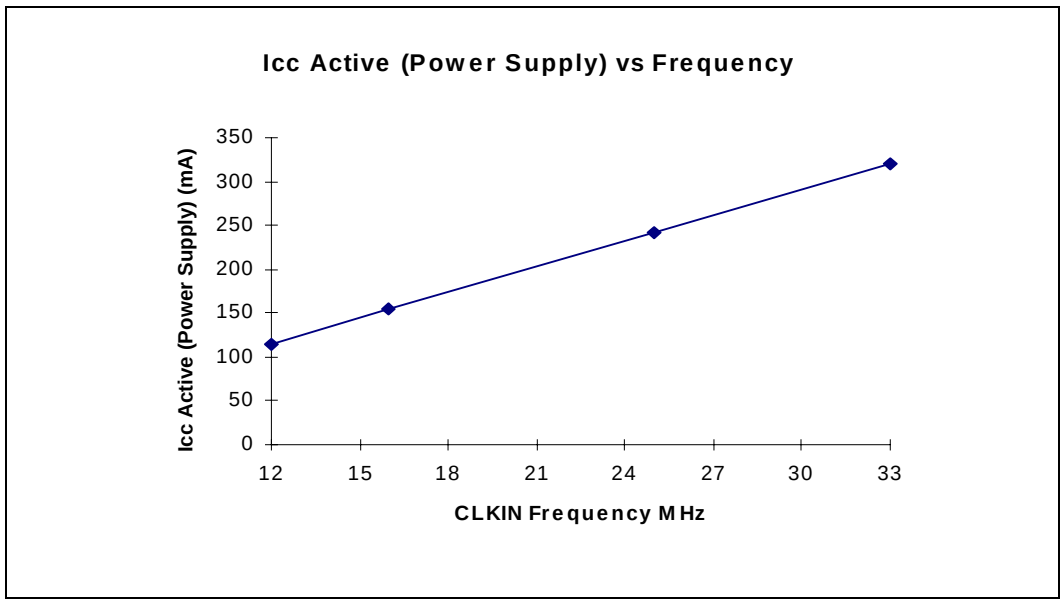


Figure 18. 80960JA/JF I_{CC} Active (Thermal) vs. Frequency

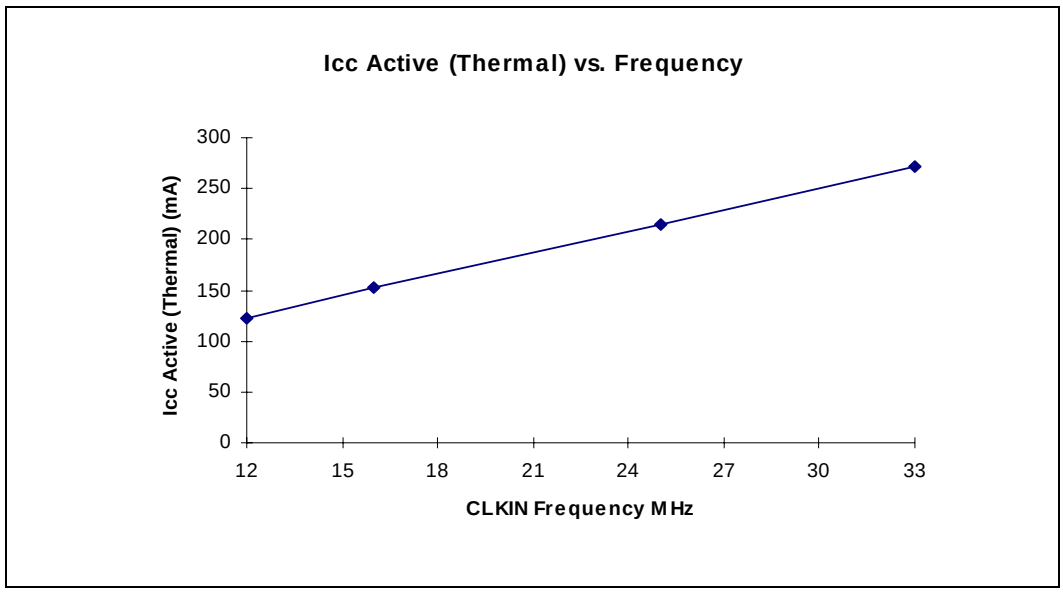


Figure 19. 80960JD I_{CC} Active (Power Supply) vs. Frequency

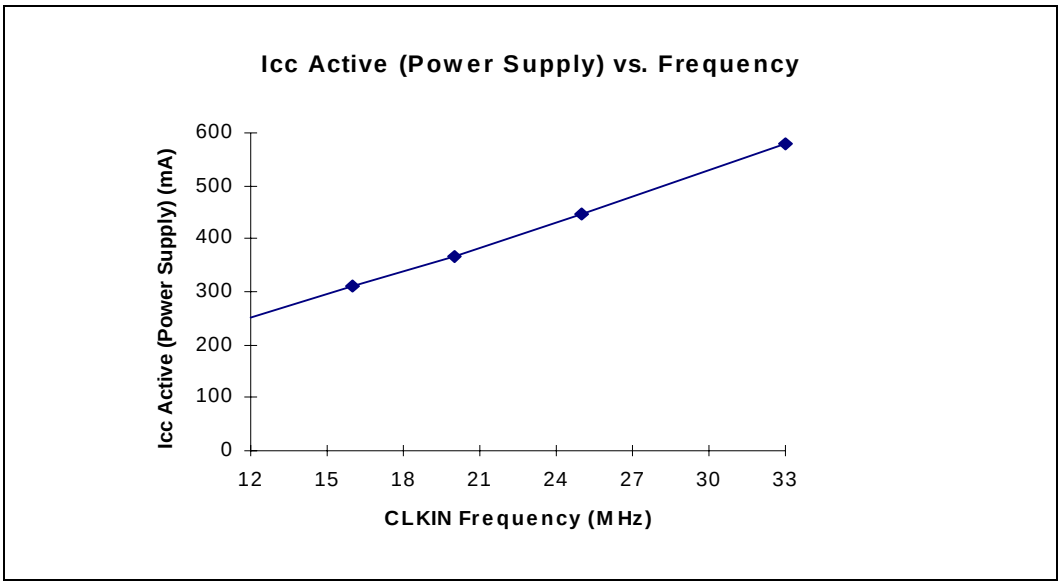


Figure 20. 80960JD I_{CC} Active (Thermal) vs. Frequency

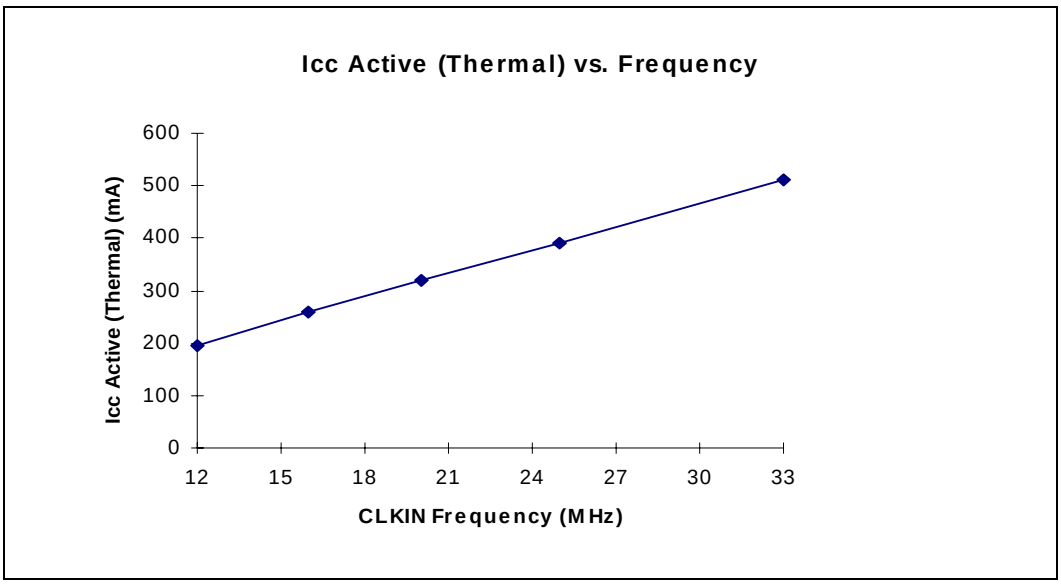


Figure 21. 80960JC I_{CC} Active (Power Supply) vs. Frequency

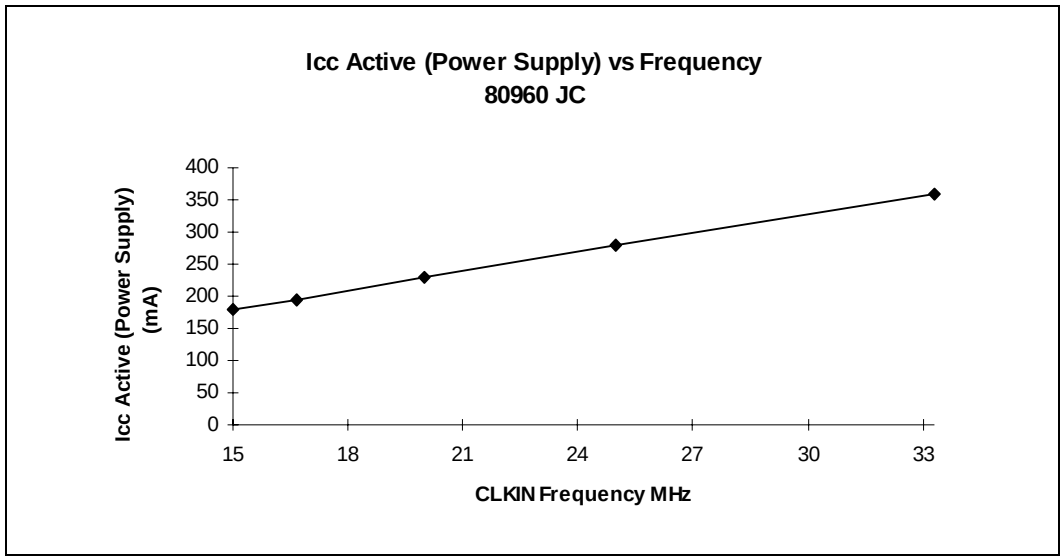


Figure 22. 80960JC I_{CC} Active (Thermal) vs. Frequency

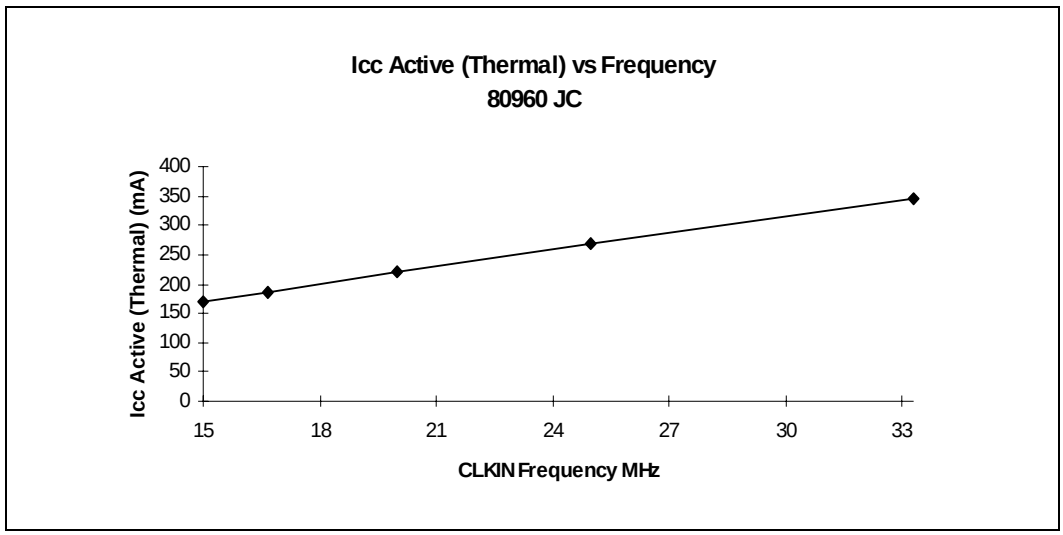


Figure 23. 80960JS I_{CC} Active (Power Supply) vs. Frequency

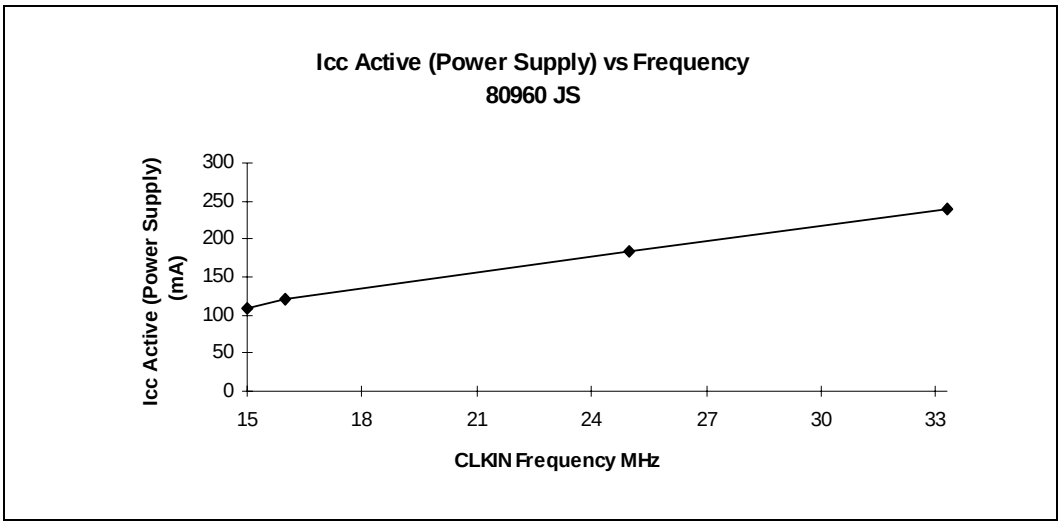
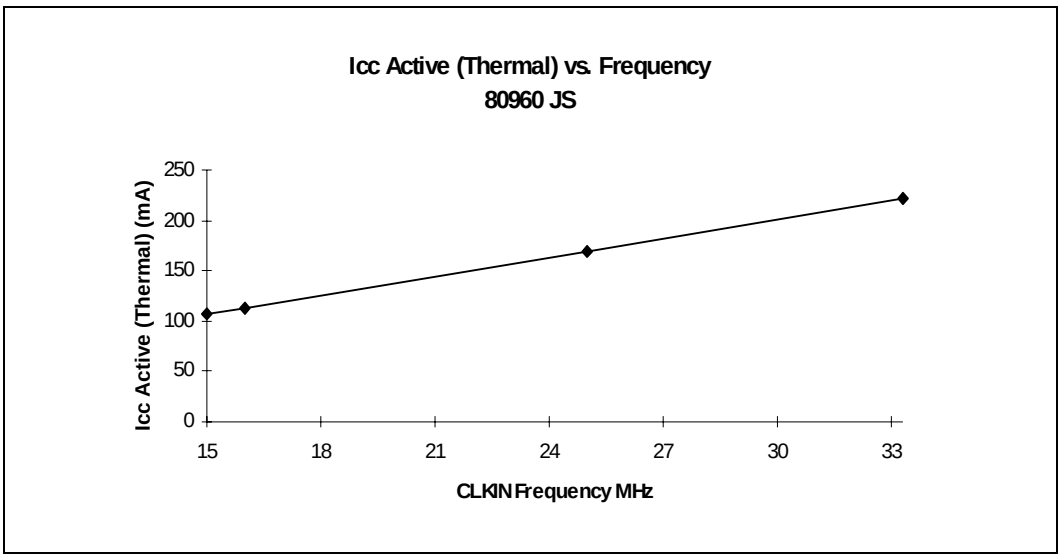


Figure 24. 80960JS I_{CC} Active (Thermal) vs. Frequency



4.7.2 A.C. Timing Waveforms

Figure 25. CLKIN Waveform

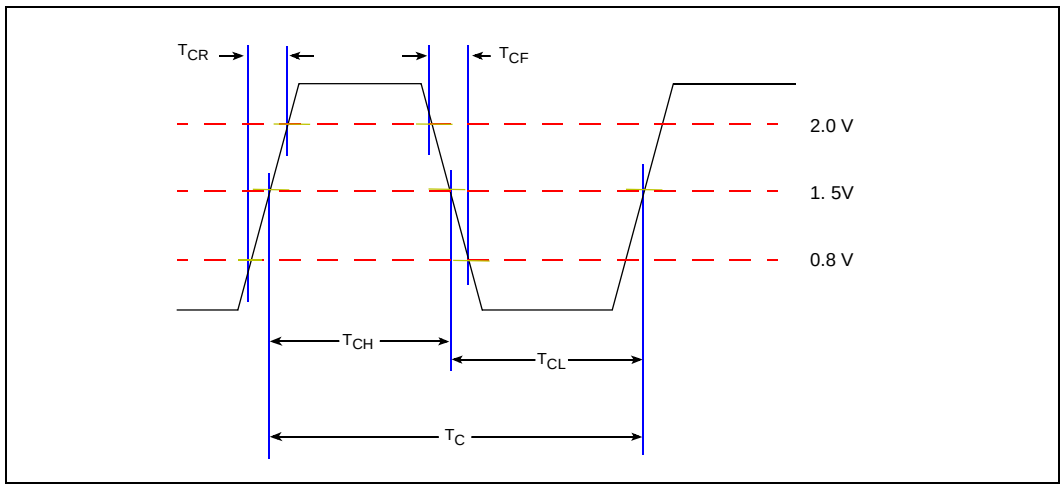


Figure 26. T_{OV1} Output Delay Waveform

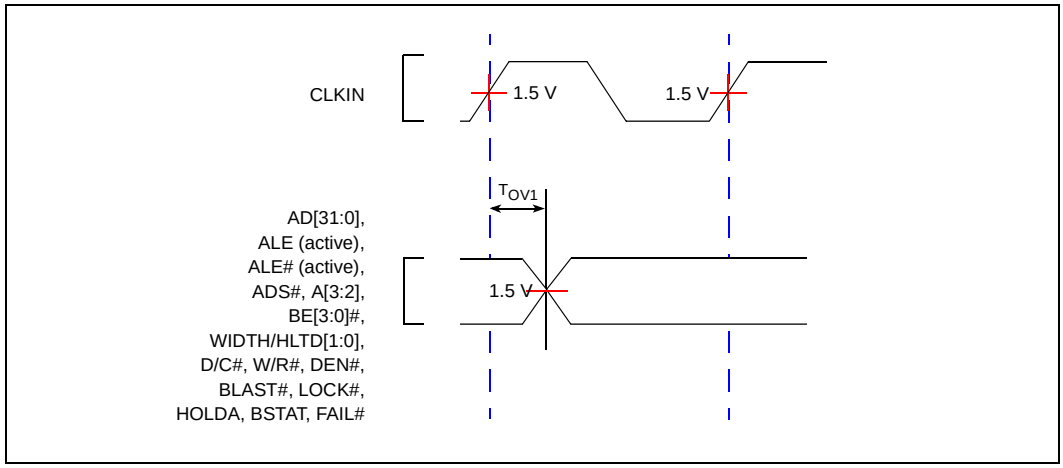


Figure 27. T_{OF} Output Float Waveform

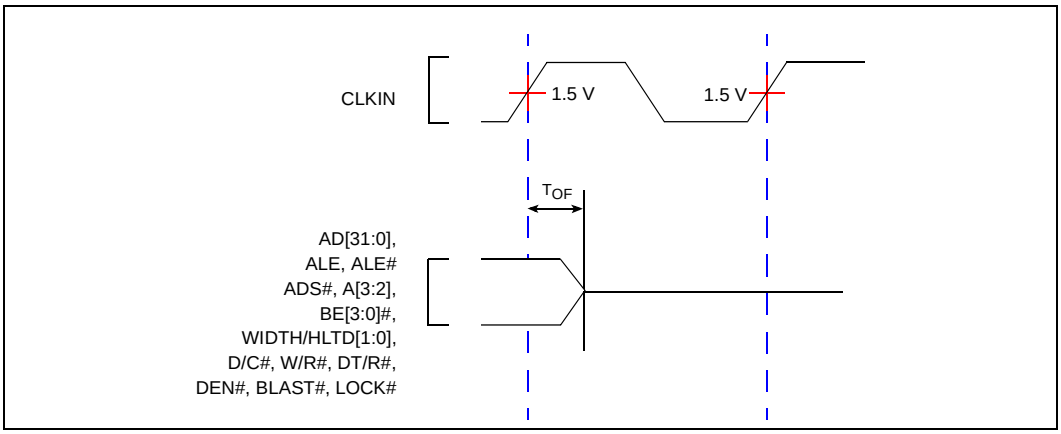


Figure 28. T_{IS1} and T_{IH1} Input Setup and Hold Waveform

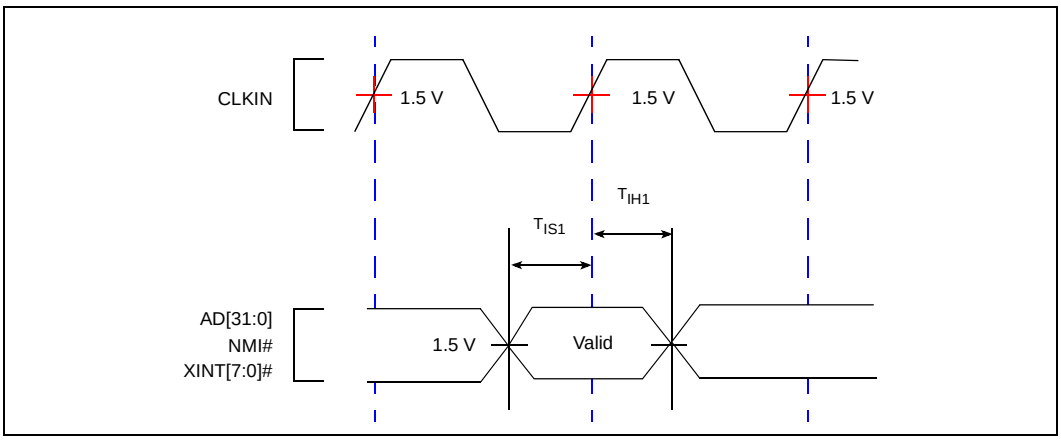


Figure 29. T_{IS2} and T_{IH2} Input Setup and Hold Waveform

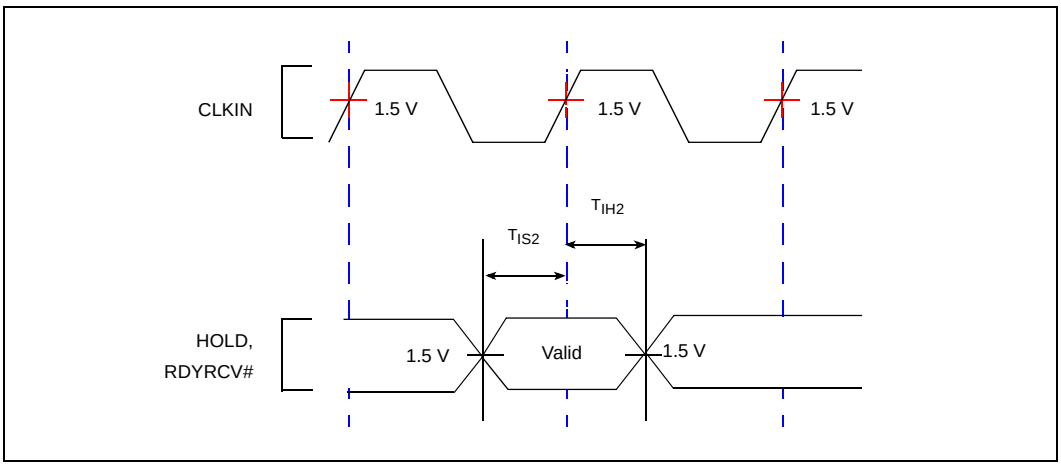


Figure 30. T_{IS3} and T_{IH3} Input Setup and Hold Waveform

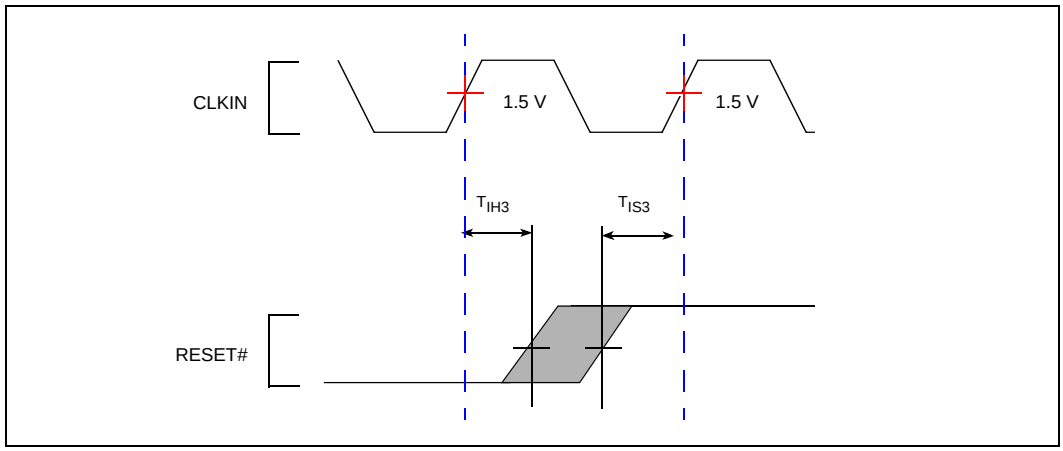


Figure 31. T_{IS4} and T_{IH4} Input Setup and Hold Waveform

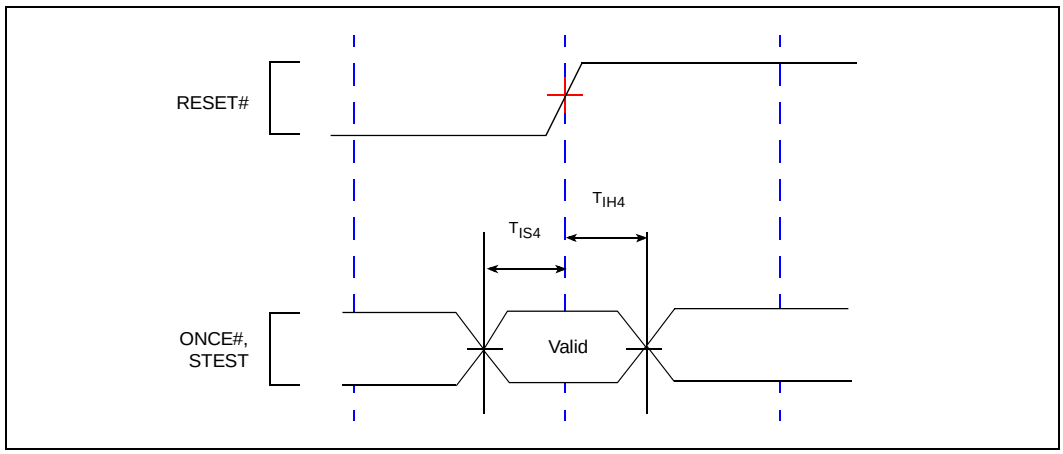


Figure 32. T_{LX}, T_{LXL} and T_{LXA} Relative Timings Waveform

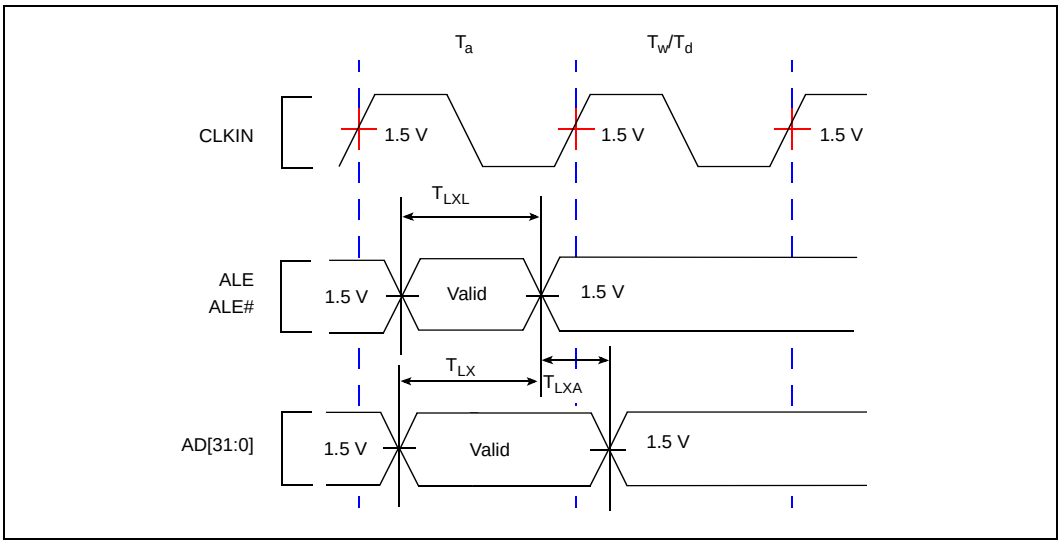


Figure 33. DT/R# and DEN# Timings Waveform

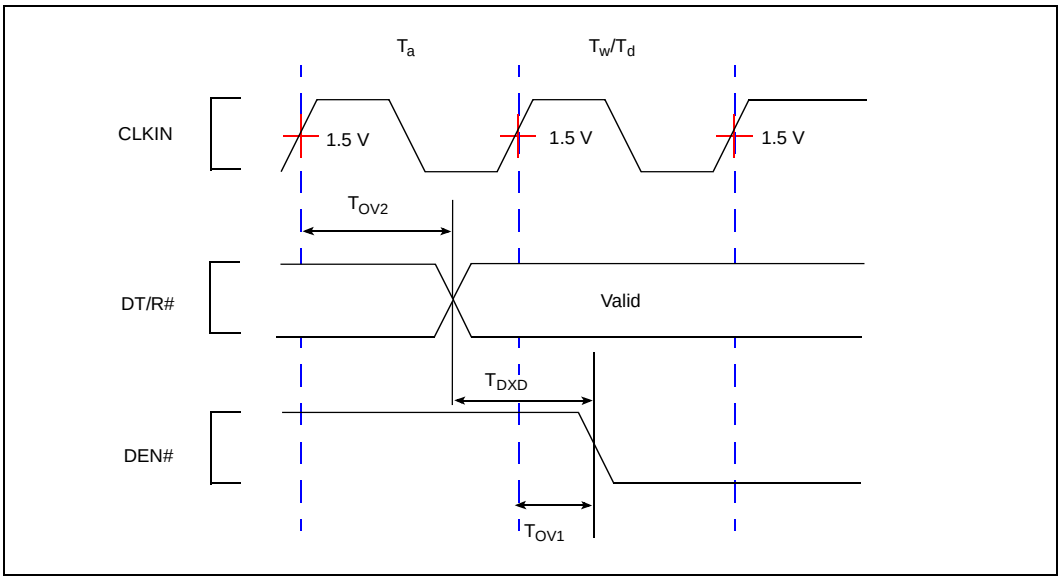


Figure 34. TCK Waveform

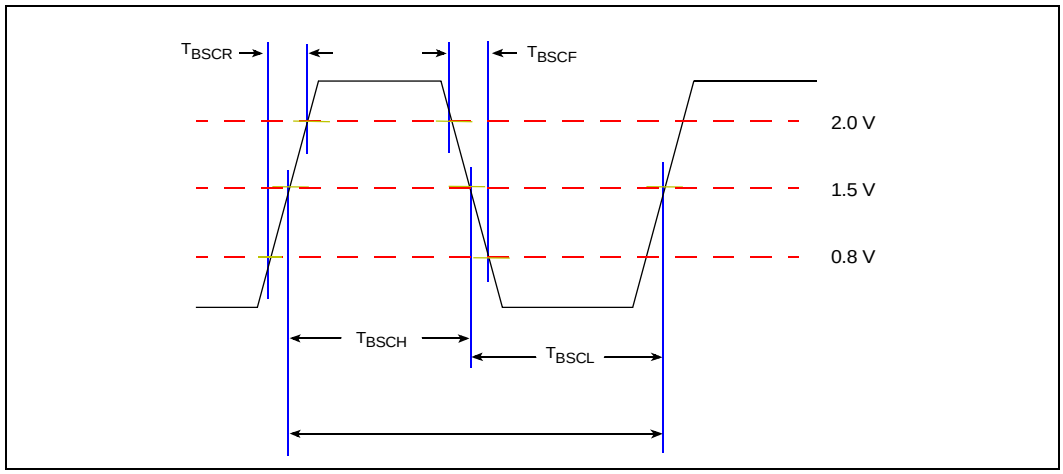


Figure 35. T_{BSIS1} and T_{BSIH1} Input Setup and Hold Waveforms

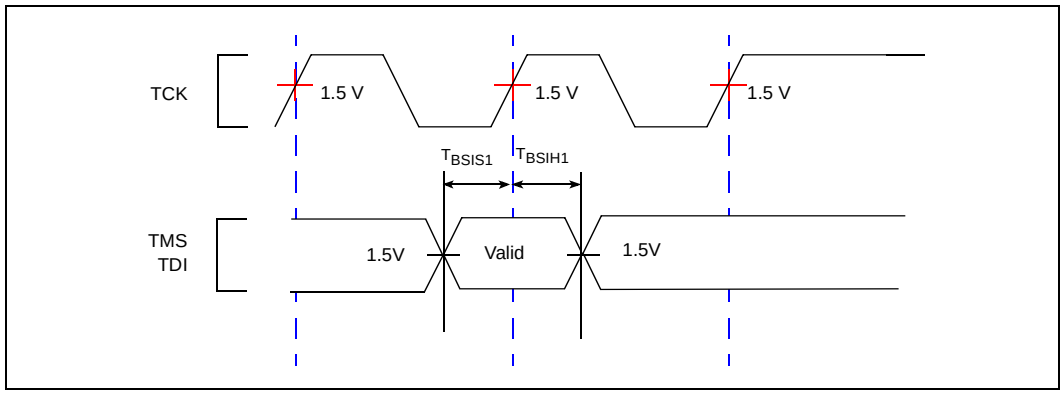


Figure 36. T_{BSOV1} and T_{BSOF1} Output Delay and Output Float Waveform

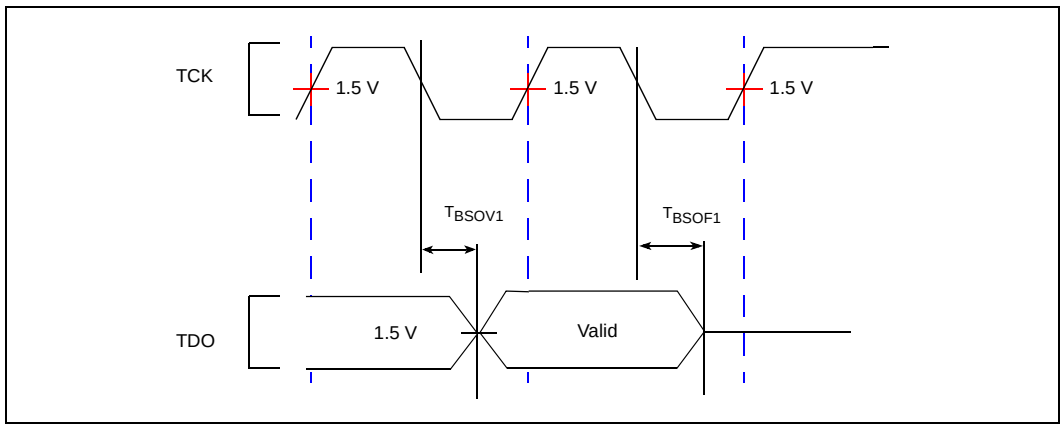


Figure 37. T_{BSOV2} and T_{BSOF2} Output Delay and Output Float Waveform

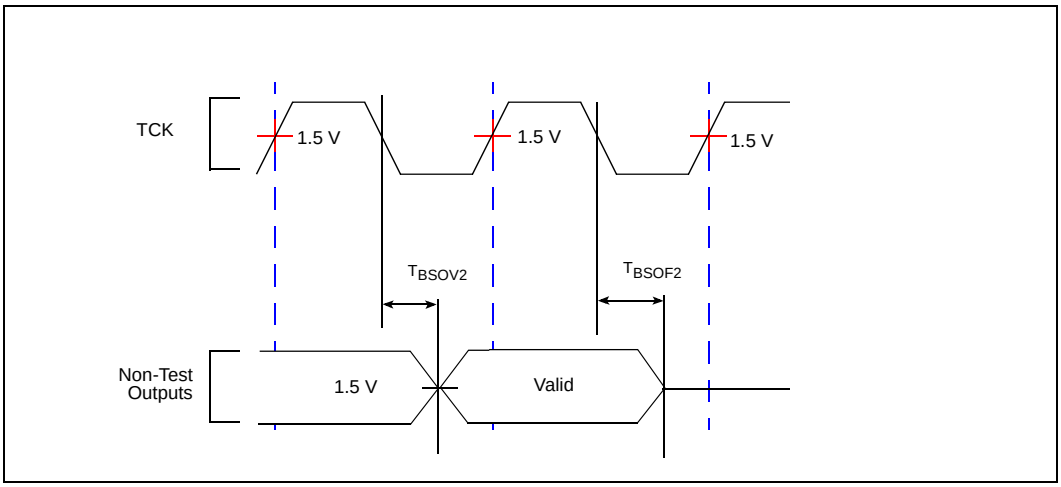
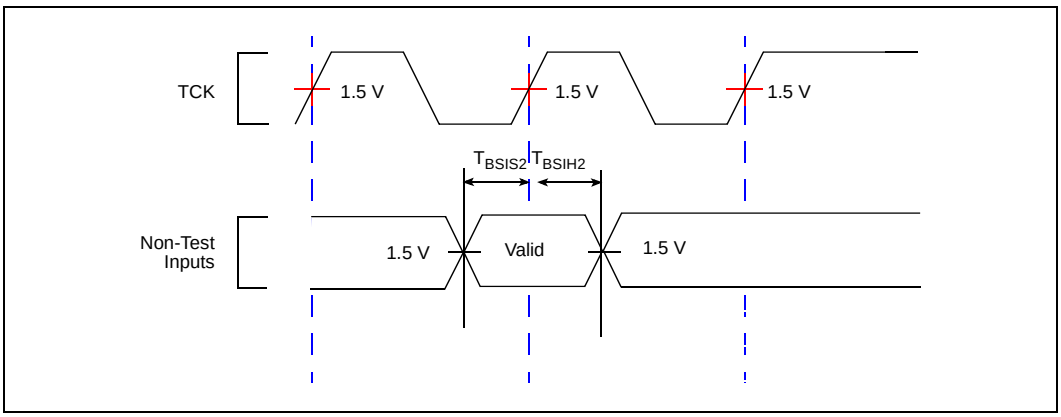


Figure 38. T_{BSIS2} and T_{BSIH2} Input Setup and Hold Waveform



5.0 Device Identification

80960Jx processors may be identified electrically, according to device type and stepping (see Figure 39, and Table 25 through Table 30). Table 24 identifies the device type and stepping for all 5 V, 80960Jx processors. Figure 39, and Table 25 through Table 30 identify all 3.3 V to 5 V-tolerant 80960Jx processors. The device ID was enhanced to differentiate between 3.3 V and 5 V supply voltages, and between non-clock-doubled and clock-doubled cores when stepping from the A2 stepping to the C0 stepping. The 32-bit identifier is accessible in several ways:

- Upon reset, the identifier is placed into the g0 register.
- The identifier may be accessed from supervisor mode at any time by reading the DEVICEID register at address FF008710H.
- The IEEE Standard 1149.1 Test Access Port may select the DEVICE ID register through the IDCODE instruction.
- The device and stepping letter is also printed on the top side of the product package.

Table 24. 80960Jx Device Type and Stepping Reference

Device and Stepping	Version Number	Part Number	Manufacturer	X	Complete ID (Hex)
80960JT A0, A1	0000	0000 1000 0010 1011	0000 0001 001	1	0082B013
80960JC A1	0011	0000 1000 0011 0011	0000 0001 001	1	30833013
80960JS A1	0011	0000 1000 0010 0011	0000 0001 001	1	30823013
80960JD C0	0011	0000 1000 0011 0000	0000 0001 001	1	30830013
80960JF C0	0011	0000 1000 0010 0000	0000 0001 001	1	30820013
80960JA C0	0011	0000 1000 0010 0001	0000 0001 001	1	30821013

5.1 80960JS/JC/JT Device Identification Register

Figure 39. 80960JS/JC/JT Device Identification Register Fields

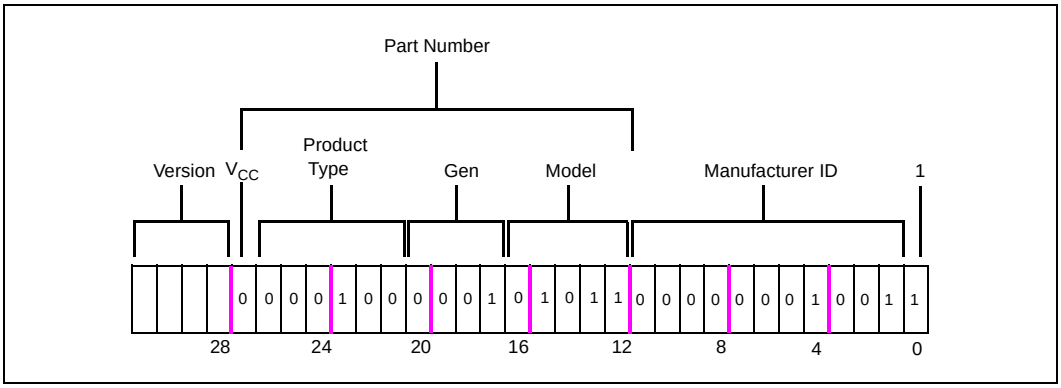


Table 25. 80960JS/JC/JT Device ID Register Field Definitions

Field	Value	Definition
Version	See Table 26	Indicates major stepping changes.
V_{CC}	0 = 3.3 V device	Indicates that a device is 3.3 V.
Product Type	000 100 (Indicates i960 CPU)	Designates type of product.
Generation Type	0001 = J-series	Indicates the generation (or series) to which the product belongs.
Model	D DPCC D = Clock Multiplier (01) Clock-Tripled (P) Product Derivative (0) Jx C = Cache Size (11) 16K I-cache, 4K D-cache	Indicates member within a series and specific model information.
Manufacturer ID	000 0000 1001 (Indicates Intel)	Manufacturer ID assigned by IEEE.

Table 26. 80960JS/JC/JT Device ID Model Types

Device	Version	V_{CC}	Product	Gen.	Model	Manufacturer ID	'1'
80960JT A0, A1	0000	0	000100	0001	01011	00000001001	1
80960JC A1	0000	0	000100	0001	10011	00000001001	1
80960JS A1	0000	0	000100	0001	00011	00000001001	1

5.2 80960JD Device Identification Register

Figure 40. 80960JD Device Identification Register Fields

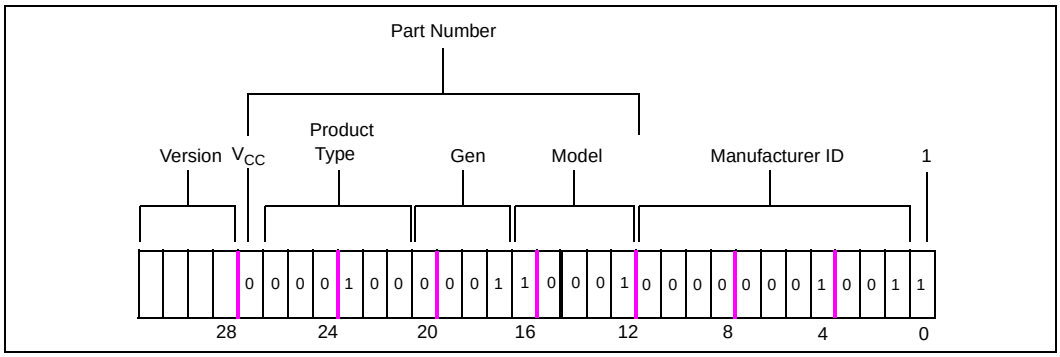


Table 27. 80960JD Device ID Field Definitions

Field	Value	Definition
Version	See Table 24.	Indicates major stepping changes.
V_{CC}	0 = 3.3 V device 1 = 5 V device	Indicates that a device is 3.3 V.
Product Type	00 0100 (Indicates i960 CPU)	Designates type of product.
Generation Type	0001 = J-series	Indicates the generation (or series) to which the product belongs.
Model	D000C D = Clock Doubled (0) Not Clock-Doubled (1) Clock Doubled C = Cache Size (0) 4K I-cache, 2K D-cache (1) 2K I-cache, 1K D-cache	Indicates member within a series and specific model information.
Manufacturer ID	000 0000 1001 (Indicates Intel)	Manufacturer ID assigned by IEEE.

Table 28. 80960JD Device ID Model Types

Device	Version	V_{CC}	Product	Gen.	Model	Manufacturer ID	'1'
80960JD C0	0011	0	000100	0001	10000	00000001001	1

5.3 80960JA/JF Device Identification Register

Figure 41. 80960JA/JF Device Identification Register Fields

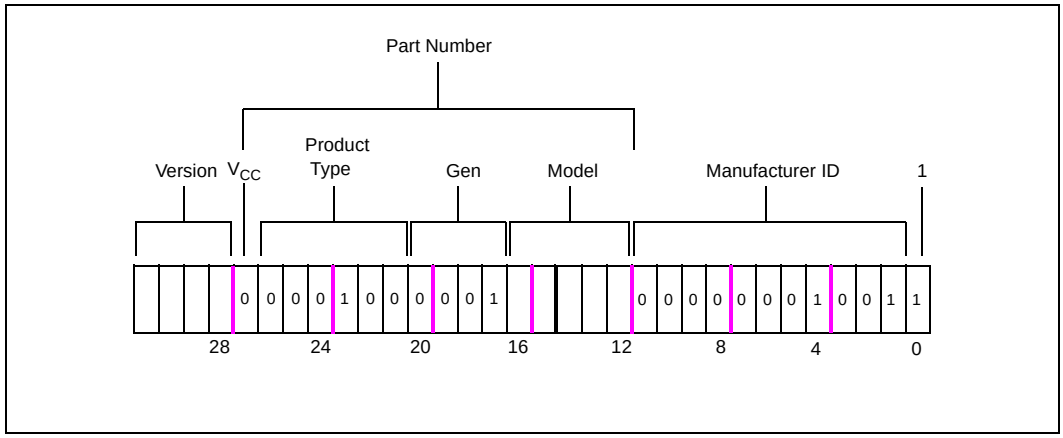


Table 29. 80960JA/JF Device ID Field Definitions

Field	Value	Definition
Version	See Table 30.	Indicates major stepping changes.
V_{CC}	0 = 3.3 V device 1 = 5 V device	Indicates that a device is 3.3 V.
Product Type	00 0100 (Indicates i960 CPU)	Designates type of product.
Generation Type	0001 = J-series	Indicates the generation (or series) to which the product belongs.
Model	0000C C = Cache Size 0 = 4K I-cache, 2K D-cache 1 = 2K I-cache, 1K D-cache	Indicates member within a series and specific model information.
Manufacturer ID	000 0000 1001 (Indicates Intel)	Manufacturer ID assigned by IEEE.

Table 30. 80960JA/JF Device ID Model Types

Device	Version	V_{CC}	Product	Gen.	Model	Manufacturer ID	'1'
80960JA C0	0011	0	000100	0001	00001	00000001001	1
80960JF C0	0011	0	000100	0001	00000	00000001001	1

6.0 Thermal Specifications

The 80960Jx is specified for operation when T_C (case temperature) is within the range of 0° C to 100° C for PGA, MPBGA and PQFP packages. Extended temperature devices are also available in a PQFP package and an MPBGA package with T_C = -40° C to 100° C. Case temperature may be measured in any environment to determine whether the 80960Jx is within its specified operating range. The case temperature should be measured at the center of the top surface, opposite the pins.

θ_{CA} is the thermal resistance from case to ambient. Use the following equation to calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P\ (\theta_{CA})$$

Junction temperature (T_J) is commonly used in reliability calculations. T_J may be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P\ (\theta_{JC})$$

Similarly, when T_A is known, the corresponding case temperature (T_C) may be calculated as follows:

$$T_C = T_A + P\ (\theta_{CA})$$

Compute P by multiplying I_{CC} from Table 21, “80960Jx ICC Characteristics” on page 39 and V_{CC}. See the following tables for θ_{JC} and θ_{CA} values:

Table 31. Thermal Resistance for θ_{CA} and θ_{JC} Reference Table

Package	Table
PGA package	Table 33 on page 64
MPBGA package	Table 34 on page 64 and Table 35 on page 65
PQFP package	Table 36 on page 65

For high speed operation, the processor’s θ_{JA} may be significantly reduced by adding a heatsink and/or by increasing airflow.

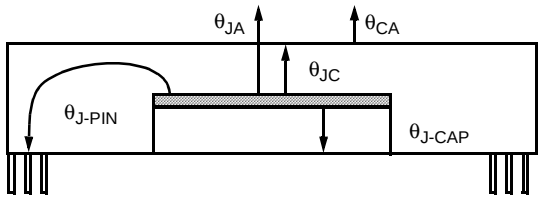
Refer to the following tables for the maximum ambient temperature (T_A) permitted without exceeding T_C for the PGA, MPBGA, and PQFP packages. The values are based on typical I_{CC} and V_{CC} of +3.3 V, with a T_C of +100° C.

Table 32. Maximum Ambient Temperature Reference Table

Processor	Table
80960JT processor	Table 37 on page 66
80960JC processor	Table 38 on page 66
80960JD processor	Table 39 on page 67
80960JS processor	Table 40 on page 67
80960JA/JF processor	Table 41 on page 68

Table 33. 132-Lead PGA Package Thermal Characteristics

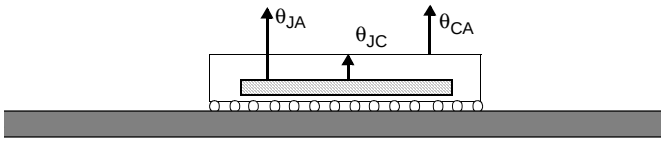
Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.08)
θ_{JC} (Junction-to-Case)	0.7	0.7	0.7	0.7	0.7	0.7
θ_{CA} (Case-to-Ambient) (No Heatsink)	25	19	14	12	11	10
θ_{CA} (Case-to-Ambient) (Omnidirectional Heatsink)	15	9	6	5	4	4
θ_{CA} (Case-to-Ambient) (Unidirectional Heatsink)	16	8	6	5	4	4



NOTES:
1. This table applies to a PGA device plugged into a socket or soldered directly into a board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{J\text{-}CAP}$ = 5.6° C/W (approximate) (no heatsink)
4. $\theta_{J\text{-}PIN}$ = 6.4° C/W (inner pins) (approximate) (no heatsink)
5. $\theta_{J\text{-}PIN}$ = 6.2° C/W (outer pins) (approximate) (no heatsink)
6. $\theta_{J\text{-}CAP}$ = 3° C/W (approximate) (with heatsink)
7. $\theta_{J\text{-}PIN}$ = 3.3° C/W (inner pins) (approximate) (with heatsink)
8. $\theta_{J\text{-}PIN}$ = 3.3° C/W (outer pins) (approximate) (with heatsink)

Table 34. 80960JA/JF/JD 196-Ball MPBGA Package Thermal Characteristics

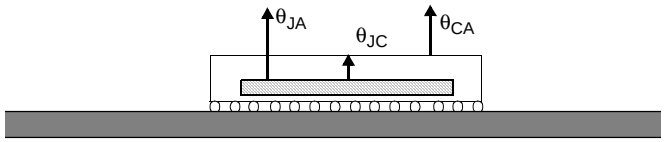
Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.08)
θ_{JC} (Junction-to-Case)	2	2	2	2	2	2
θ_{CA} (Case-to-Ambient) (No Heatsink)	30	22	20	19	18	18



NOTES:
1. This table applies to an MPBGA device soldered directly into a board with all V_{SS} connections.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

Table 35. 80960JS/JC/JT 196-Ball MPBGA Package Thermal Characteristics

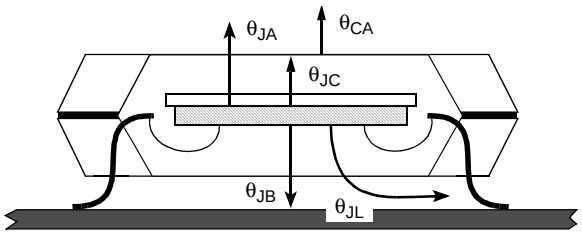
Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.08)
θ_{JC} (Junction-to-Case)	2	2	2	2	2	2
θ_{CA} (Case-to-Ambient) (No Heatsink)	34	25	23	22	21	20



NOTES:
1. This table applies to an MPBGA device soldered directly into a board with all V_{SS} connections.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

Table 36. 132-Lead PQFP Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	Airflow — ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ_{JC} (Junction-to-Case)	4.1	4.3	4.3	4.3	4.3	4.7	4.9
θ_{CA} (Case-to-Ambient -No Heatsink)	23	19	18	16	14	11	9



NOTES:
1. This table applies to a PQFP device soldered directly into board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. θ_{JL} = 13° C/W (approx.)
4. θ_{JB} = 13.5° C/W (approx.)

Table 37. Maximum T_A at Various Airflows in °C (80960JT)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
PQFP Package	T_A without Heatsink	33	63	74	78	82	86	87
PGA Package	T_A without Heatsink	33	60	70	78	81	82	84
	T_A with Omnidirectional Heatsink[1]	33	76	86	90	92	94	94
	T_A with Unidirectional Heatsink[2]	33	74	87	90	92	94	94
MPBGA Package	T_A without Heatsink	33	46	60	63	65	66	68

NOTES:
1. 0.248 inch high omnidirectional heatsink (AI alloy 6061, 41 mil fin width, 124 mil center-to-center fin spacing).
2. 0.250 inch high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 146 mil center-to-center fin spacing).

Table 38. Maximum T_A at Various Airflows in °C (80960JC)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
PQFP Package	T_A without Heatsink	33 25 20 16.67	75 79 84 86	82 86 89 90	85 87 90 92	88 90 92 93	90 92 94 95	91 93 94 95
PGA Package	T_A without Heatsink	33 25 20 16.67	73 78 83 85	79 83 87 89	85 87 90 92	87 89 92 93	88 90 92 93	89 91 93 94
	T_A with Omnidirectional Heatsink[1]	33 25 20 16.67	84 87 90 91	90 92 94 95	93 95 96 96	95 96 97 97	96 96 97 98	96 96 97 98
	T_A with Unidirectional Heatsink[2]	33 25 20 16.67	82 86 89 90	91 93 94 95	93 95 96 96	95 96 97 97	96 96 97 98	96 96 97 98
MPBGA Package	T_A without Heatsink	33 25 20 16.67	63 69 76 80	73 78 83 85	75 79 84 86	76 80 85 87	77 81 85 87	78 82 86 88

NOTES:
1. 0.248 inch high omnidirectional heatsink (AI alloy 6061, 41 mil fin width, 124 mil center-to-center fin spacing).
2. 0.250 inch high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 146 mil center-to-center fin spacing).

Table 39. Maximum T_A at Various Airflows in °C (80960JD)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
PQFP Package	T_A without Heatsink	33 25 20 16.67	61 70 75 79	73 79 82 86	76 82 85 87	81 86 88 90	85 88 90 92	86 90 91 93
PGA Package	T_A without Heatsink	33 25 20 16.67	58 68 73 78	68 75 79 83	76 82 85 87	80 84 87 89	81 86 88 90	83 87 89 91
	T_A with Omnidirectional Heatsink[1]	33 25 20 16.67	75 81 84 87	85 88 90 92	90 92 93 95	92 94 95 96	93 95 96 96	93 95 96 96
	T_A with Unidirectional Heatsink[2]	33 25 20 16.67	73 79 82 86	86 90 91 93	90 92 93 95	92 94 95 96	93 95 96 96	93 96 96 96
MPBGA Package	T_A without Heatsink	25	61	72	74	76	77	77

NOTES:
1. 0.248 inch high omnidirectional heatsink (AI alloy 6061, 41 mil fin width, 124 mil center-to-center fin spacing).
2. 0.250 inch high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 146 mil center-to-center fin spacing).

Table 40. Maximum T_A at Various Airflows in °C (80960JS)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
PQFP Package	T_A without Heatsink	33 25 16.67	84 86 91	89 90 94	90 92 94	92 93 96	94 95 96	94 95 97
PGA Package	T_A without Heatsink	33 25 16.67	83 85 90	87 89 92	90 92 94	92 93 95	92 93 96	93 94 96
	T_A with Omnidirectional Heatsink[1]	33 25 16.67	90 91 94	94 95 96	96 96 98	97 97 98	97 98 98	97 98 98
	T_A with Unidirectional Heatsink[2]	33 25 16.67	89 90 94	94 95 97	96 96 98	97 97 98	97 98 98	97 98 98
MPBGA Package	T_A without Heatsink	33 25 16.67	76 80 86	83 85 90	84 86 91	85 87 91	85 87 92	86 88 92

NOTES:
1. 0.248 inch high omnidirectional heatsink (AI alloy 6061, 41 mil fin width, 124 mil center-to-center fin spacing).
2. 0.250 inch high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 146 mil center-to-center fin spacing).

Table 41. Maximum T_A at Various Airflows in °C (80960JA/JF)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
PQFP Package	For NG80960JA/JF T_A without Heatsink	33 25 16	79 84 89	86 89 92	87 90 93	90 92 95	92 94 96	93 94 96
	For TG80960JA-25 T_A without Heatsink	25	84	89	90	92	94	94
PGA Package	T_A without Heatsink	33 25 16	78 83 88	83 87 91	87 90 93	89 92 94	90 92 95	91 93 95
	T_A with Omnidirectional Heatsink[1]	33 25 16	87 90 93	92 94 96	95 96 97	96 97 98	96 97 98	96 97 98
	T_A with Unidirectional Heatsink[2]	33 25 16	86 89 92	93 94 96	95 96 97	96 97 98	96 97 98	96 97 98
MPBGA Package	T_A without Heatsink	33 25	73 79	80 84	82 86	83 87	84 87	84 87

NOTES:
1. 0.248 inch high omnidirectional heatsink (Al alloy 6061, 41 mil fin width, 124 mil center-to-center fin spacing).
2. 0.250 inch high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 146 mil center-to-center fin spacing).

6.1 Thermal Management Accessories

The following is a list of suggested sources for 80960Jx thermal solutions. This is neither an endorsement or a warranty of the performance of any of the listed products and/or companies.

6.1.1 Heatsinks

1. Thermalloy, Inc.
   2021 West Valley View Lane
   Dallas, TX 75234-8993
   (972) 243-4321
2. Wakefield Engineering
   60 Audubon Road
   Wakefield, MA 01880
   (617) 245-5900
3. Aavid Thermal Technologies, Inc.
   One Kool Path
   Laconia, NH 03247-0400
   (603) 528-3400

7.0 Bus Functional Waveforms

Figure 42 through Figure 47 illustrate typical 80960Jx bus transactions. Figure 48 depicts the bus arbitration sequence. Figure 49 illustrates the processor reset sequence from the time power is applied to the device. Figure 50 illustrates the processor reset sequence when the processor is in operation. Figure 51 illustrates the processor ONCE# sequence from the time power is applied to the device. Figure 53 and Figure 54 also show accesses on 32-bit buses. Table 44 through Table 46 summarize all possible combinations of bus accesses across 8-, 16-, and 32-bit buses according to data alignment.

Figure 42. Non-Burst Read and Write Transactions Without Wait States, 32-Bit Bus

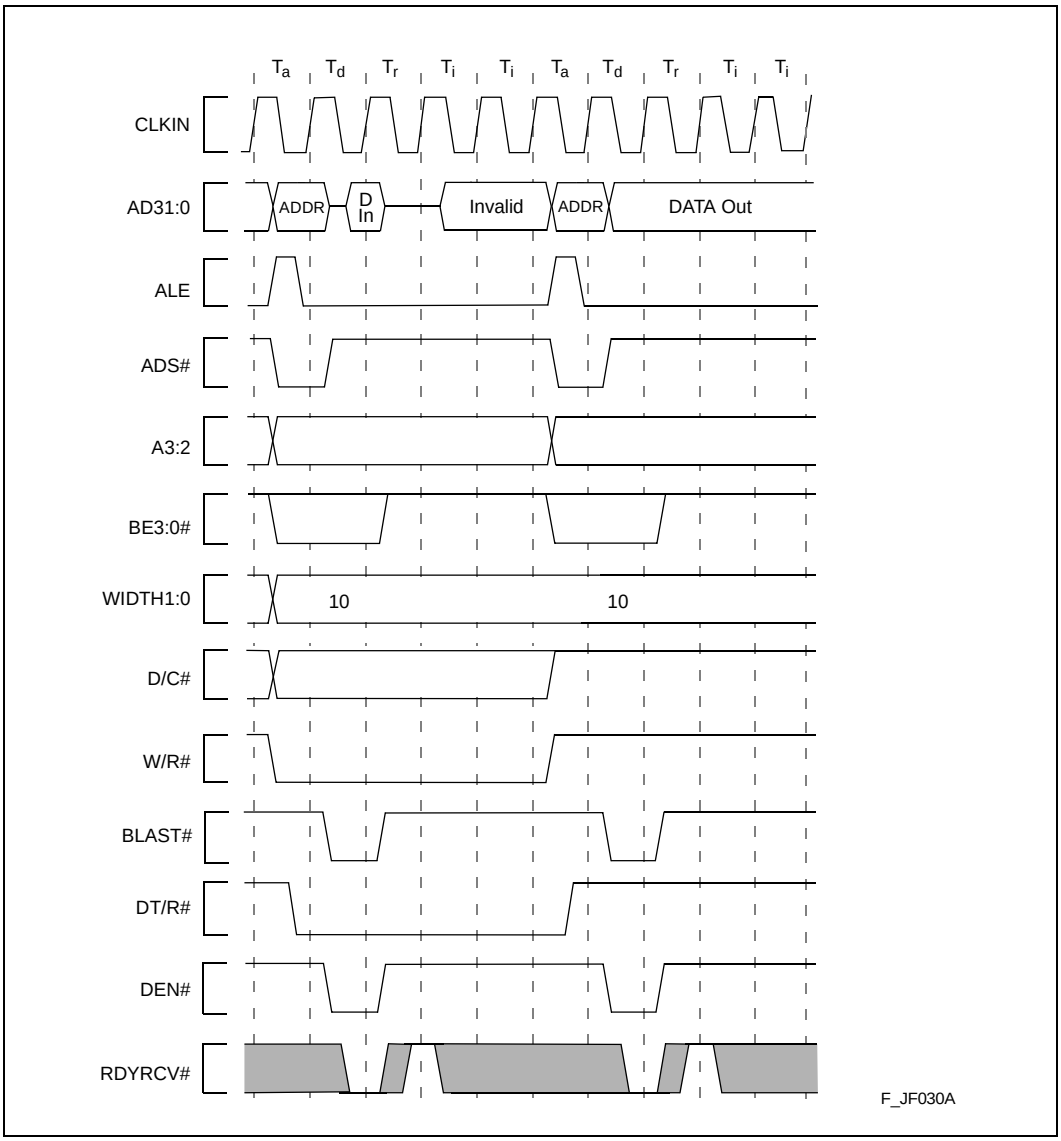


Figure 43. Burst Read and Write Transactions Without Wait States, 32-Bit Bus

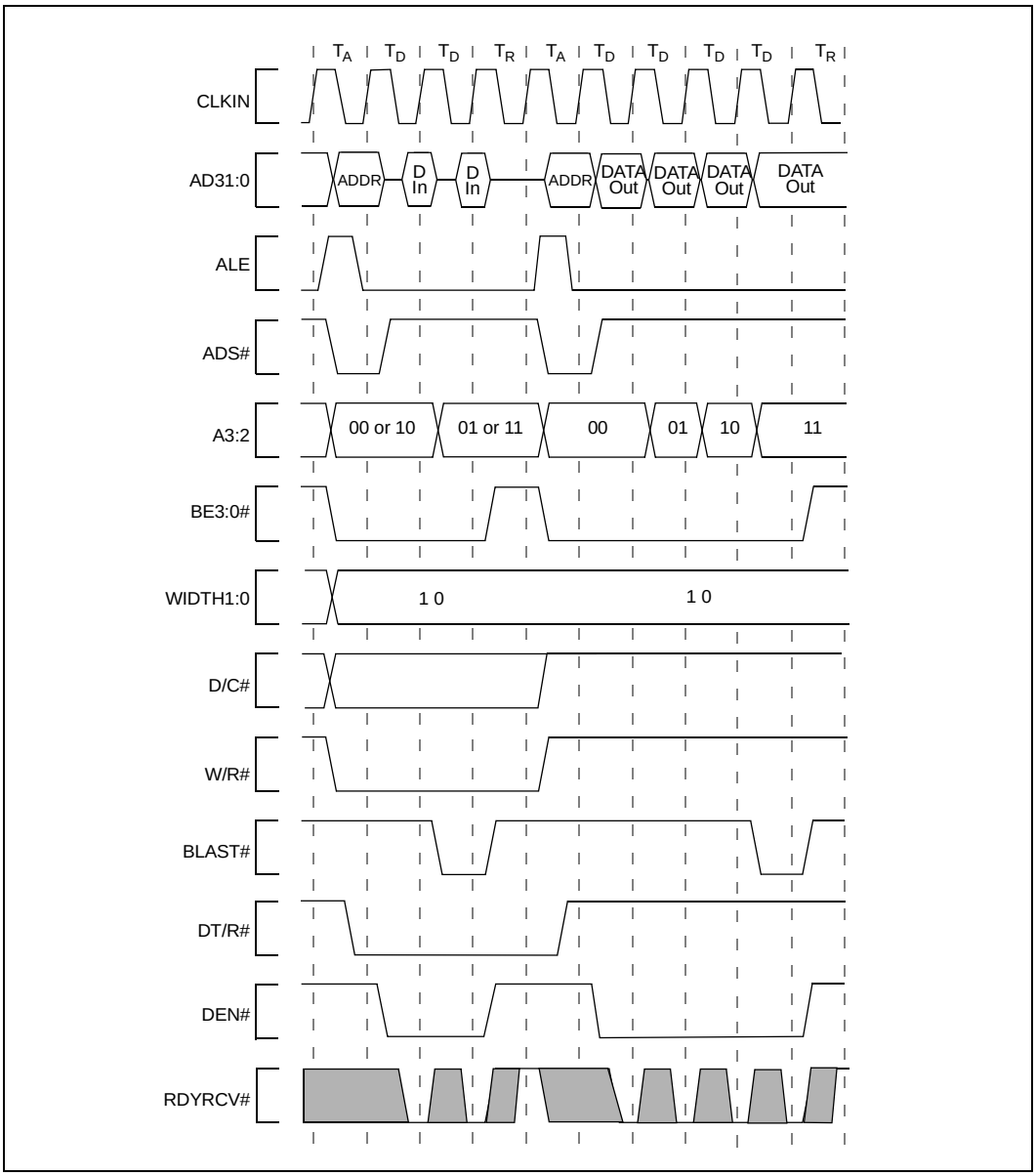


Figure 44. Burst Write Transactions With 2,1,1,1 Wait States, 32-Bit Bus

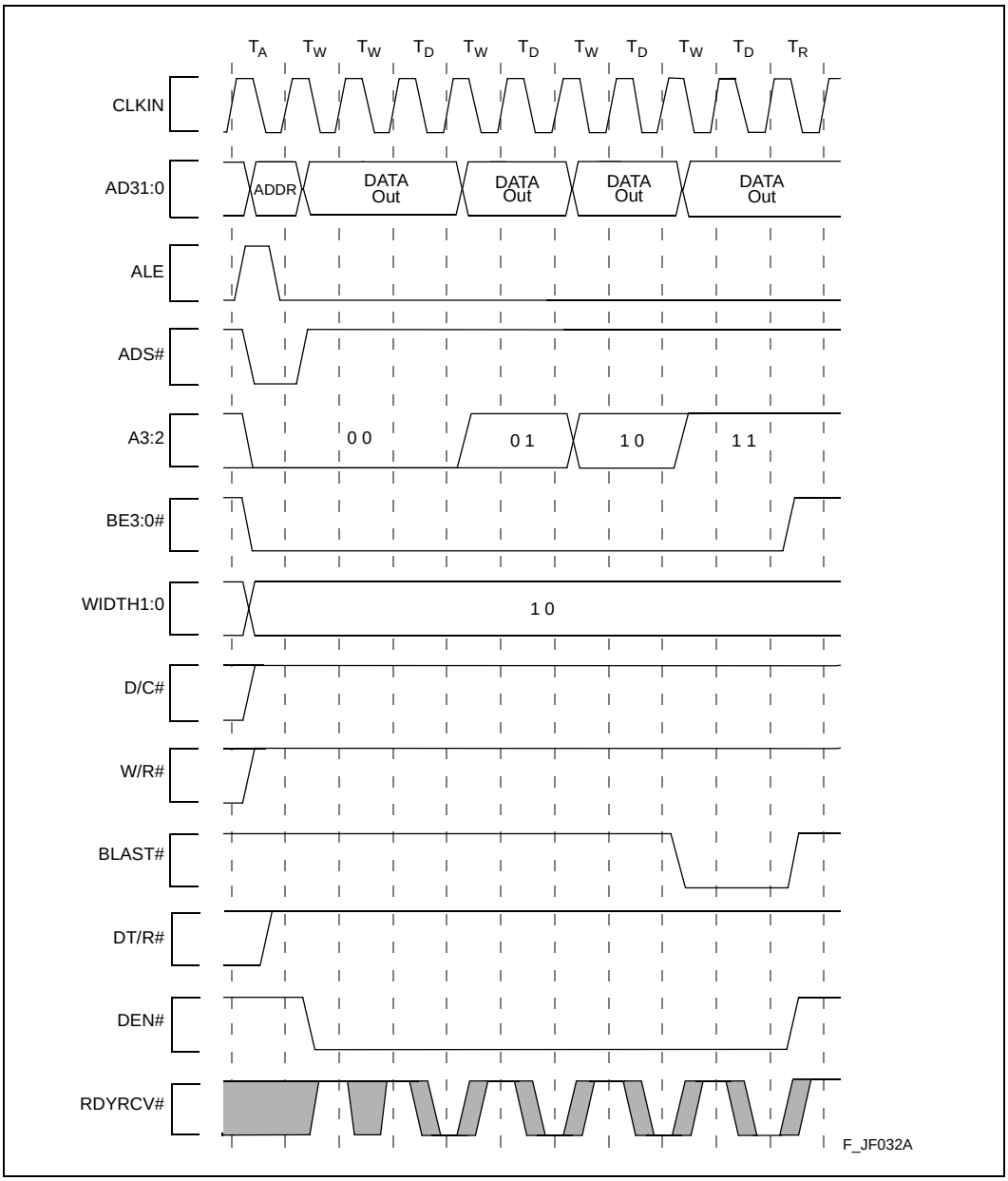


Figure 45. Burst Read and Write Transactions Without Wait States, 8-Bit Bus

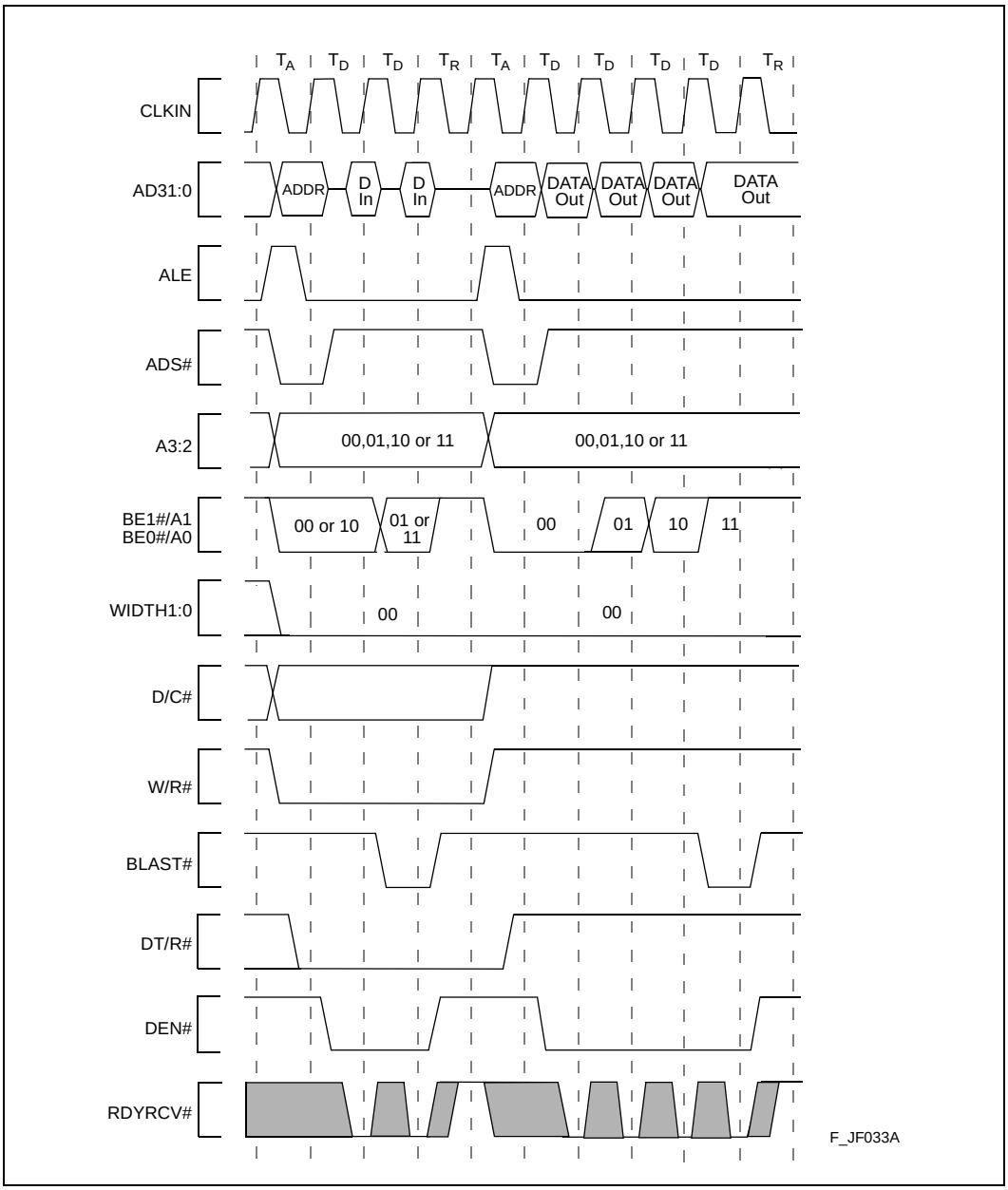


Figure 46. Burst Read and Write Transactions With 1, 0 Wait States and Extra Tr State on Read, 16-Bit Bus

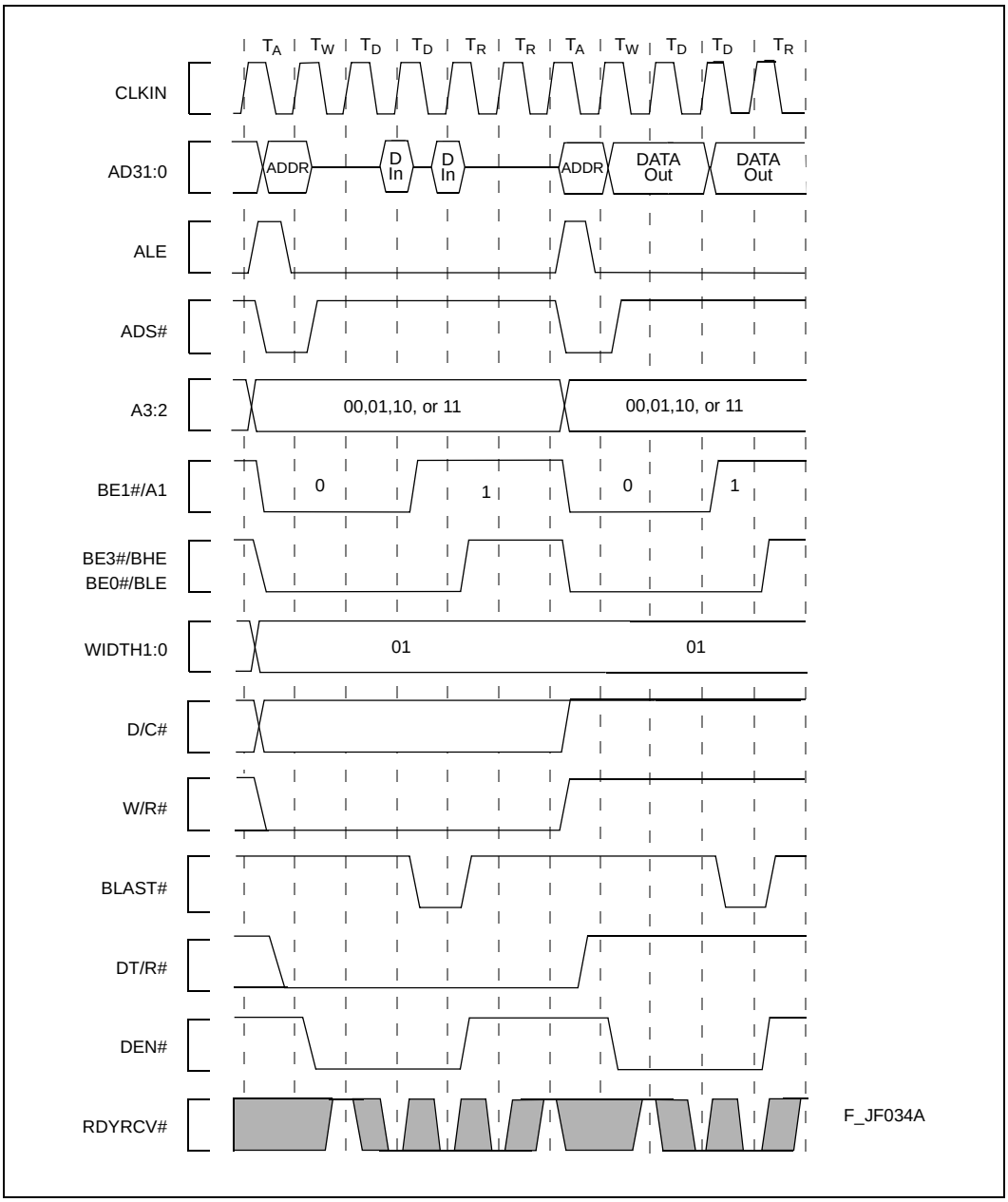


Figure 47. Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit Bus, Little Endian

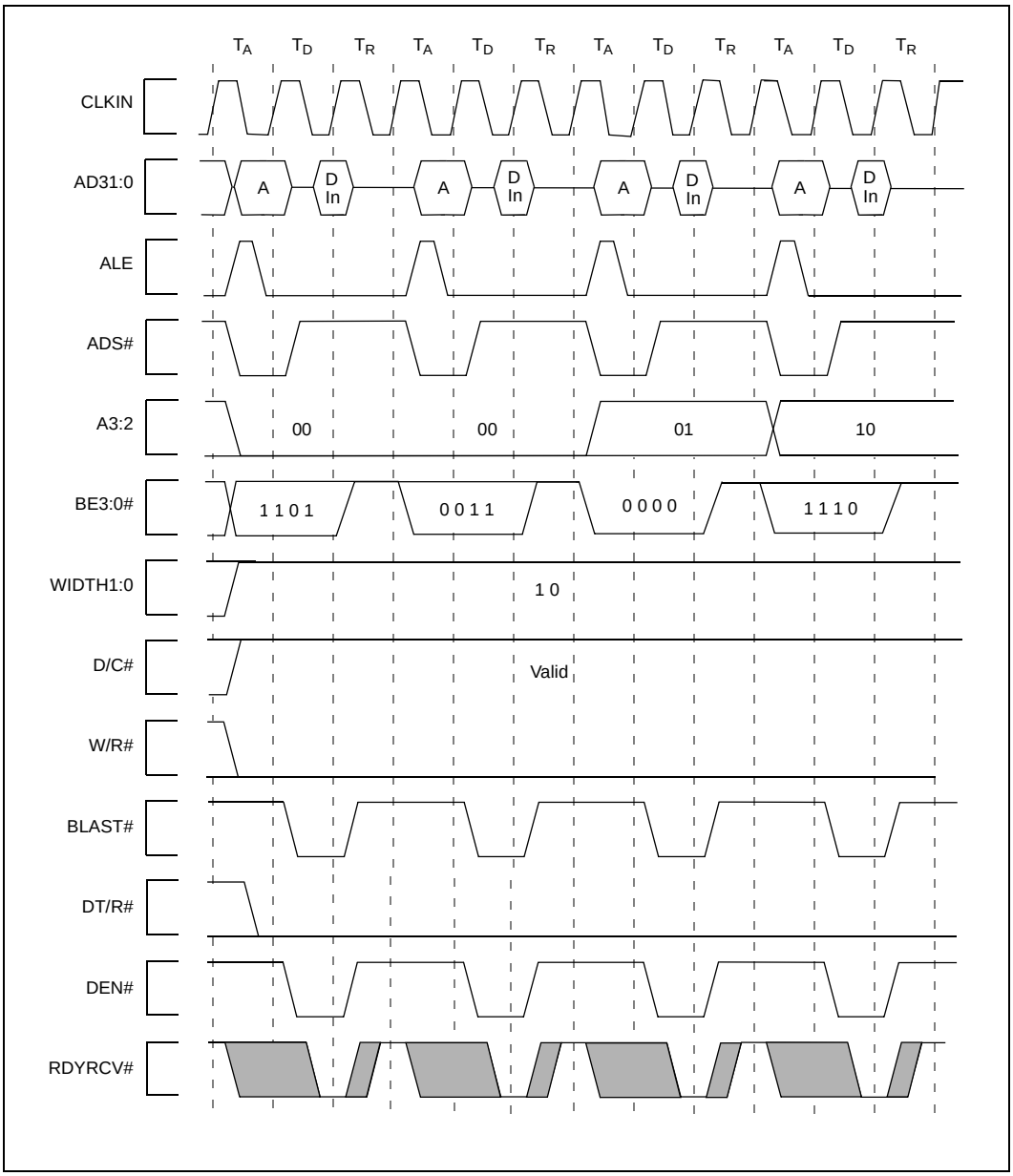
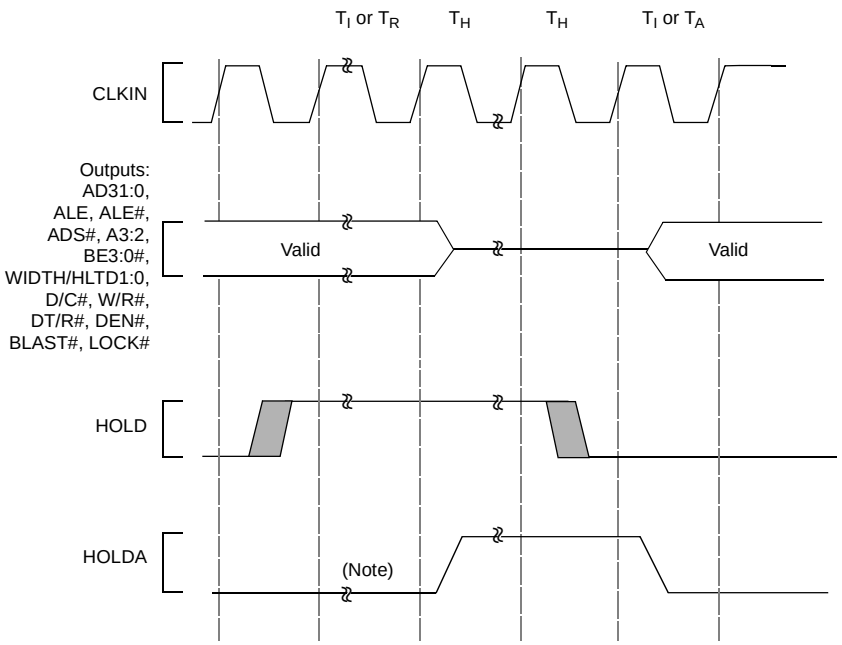
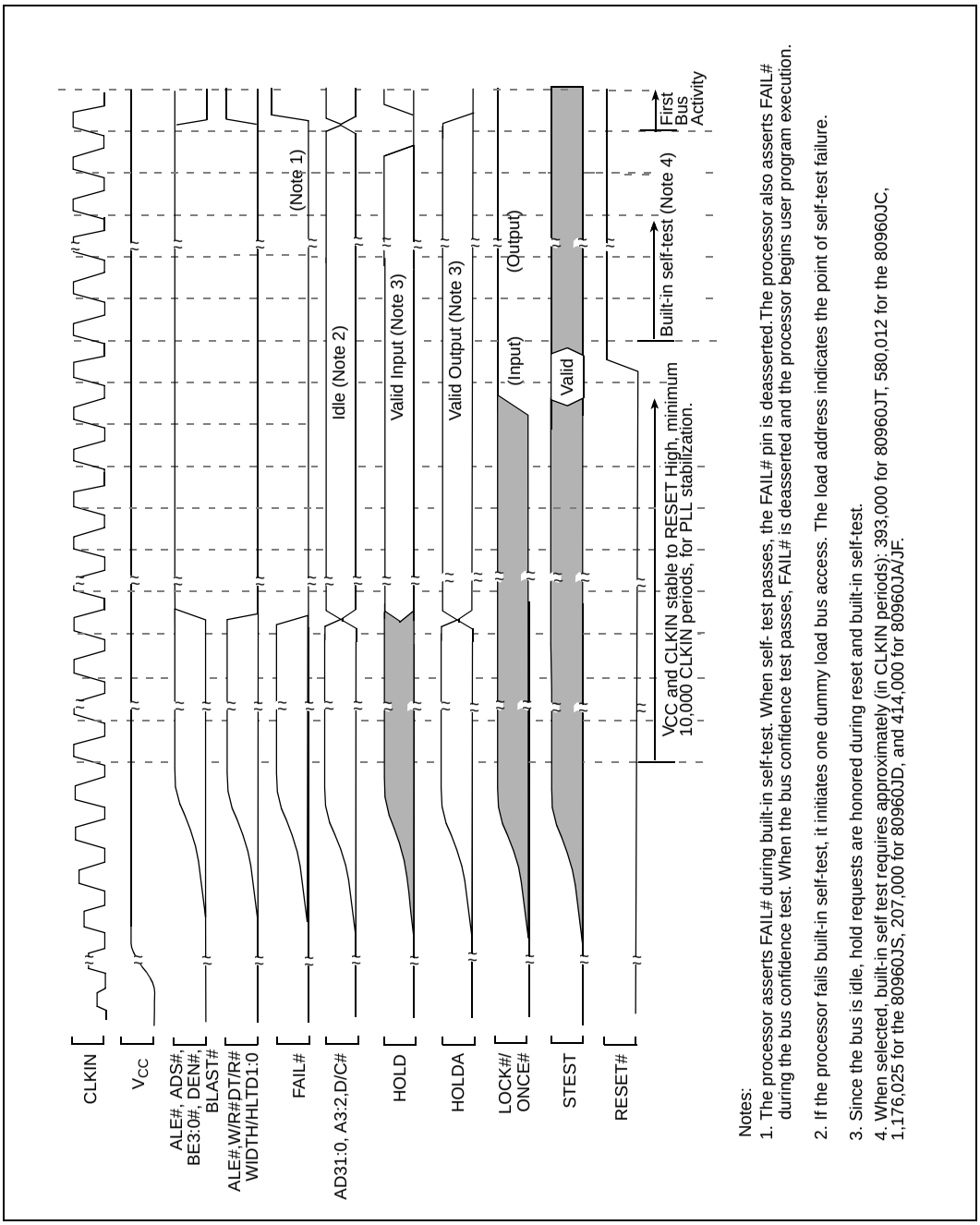


Figure 48. HOLD/HOLDA Waveform For Bus Arbitration



NOTE: HOLD is sampled on the rising edge of CLKIN. The processor asserts HOLDA to grant the bus on the same edge in which it recognizes HOLD when the last state was T_i or the last T_r of a bus transaction. Similarly, the processor deasserts HOLDA on the same edge in which it recognizes the deassertion of HOLD.

Figure 49. Cold Reset Waveform



Notes:
1. The processor asserts FAIL# during built-in self-test. When self- test passes, the FAIL# pin is deasserted.The processor also asserts FAIL# during the bus confidence test. When the bus confidence test passes, FAIL# is deasserted and the processor begins user program execution.
2. If the processor fails built-in self-test, it initiates one dummy load bus access. The load address indicates the point of self-test failure.
3. Since the bus is idle, hold requests are honored during reset and built-in self-test.
4. When selected, built-in self test requires approximately (in CLKIN periods): 393,000 for 80960JT, 580,012 for the 80960JC, 1,176,025 for the 80960JS, 207,000 for 80960JD, and 414,000 for 80960JA/JF.

Figure 50. Warm Reset Waveform

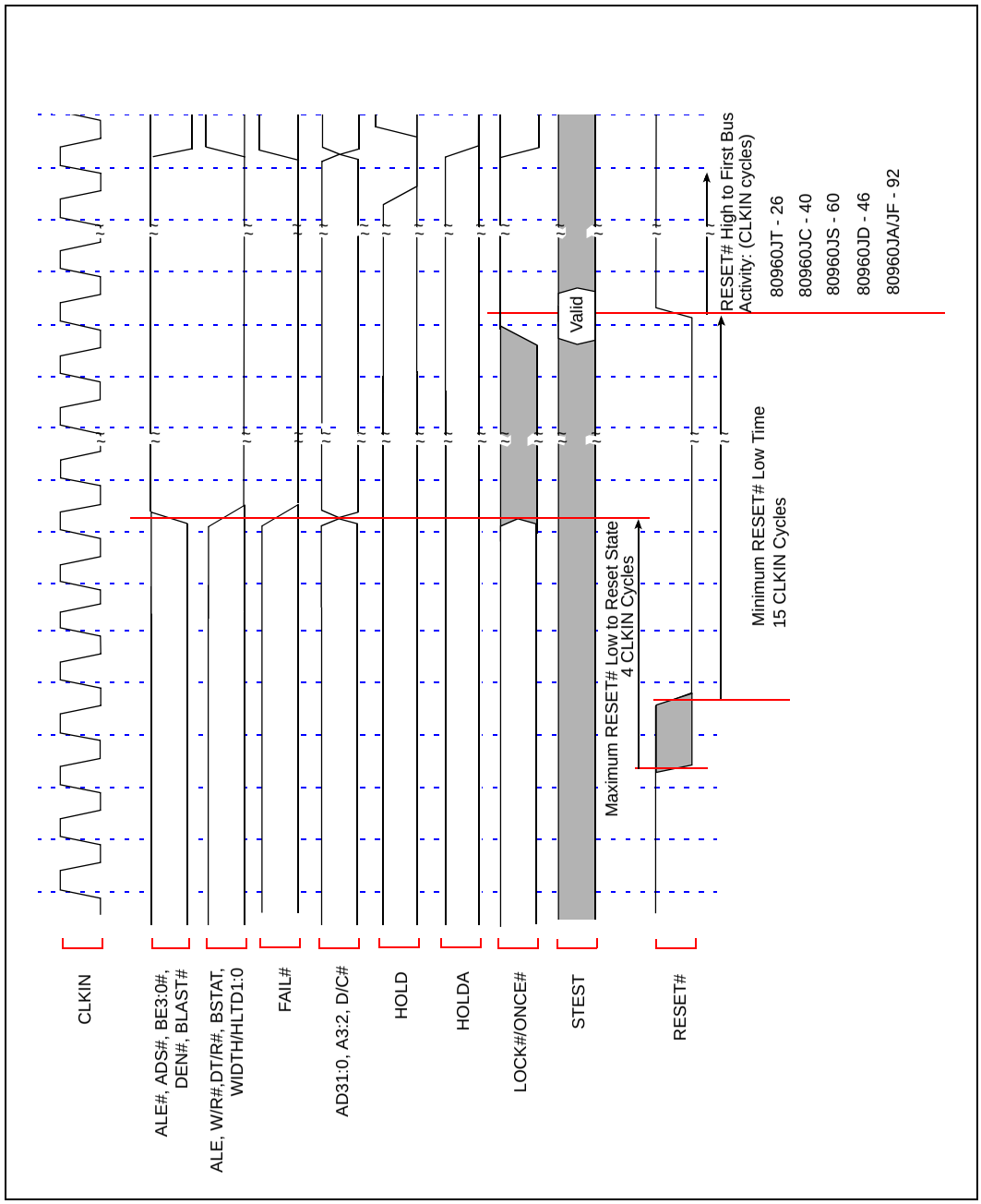
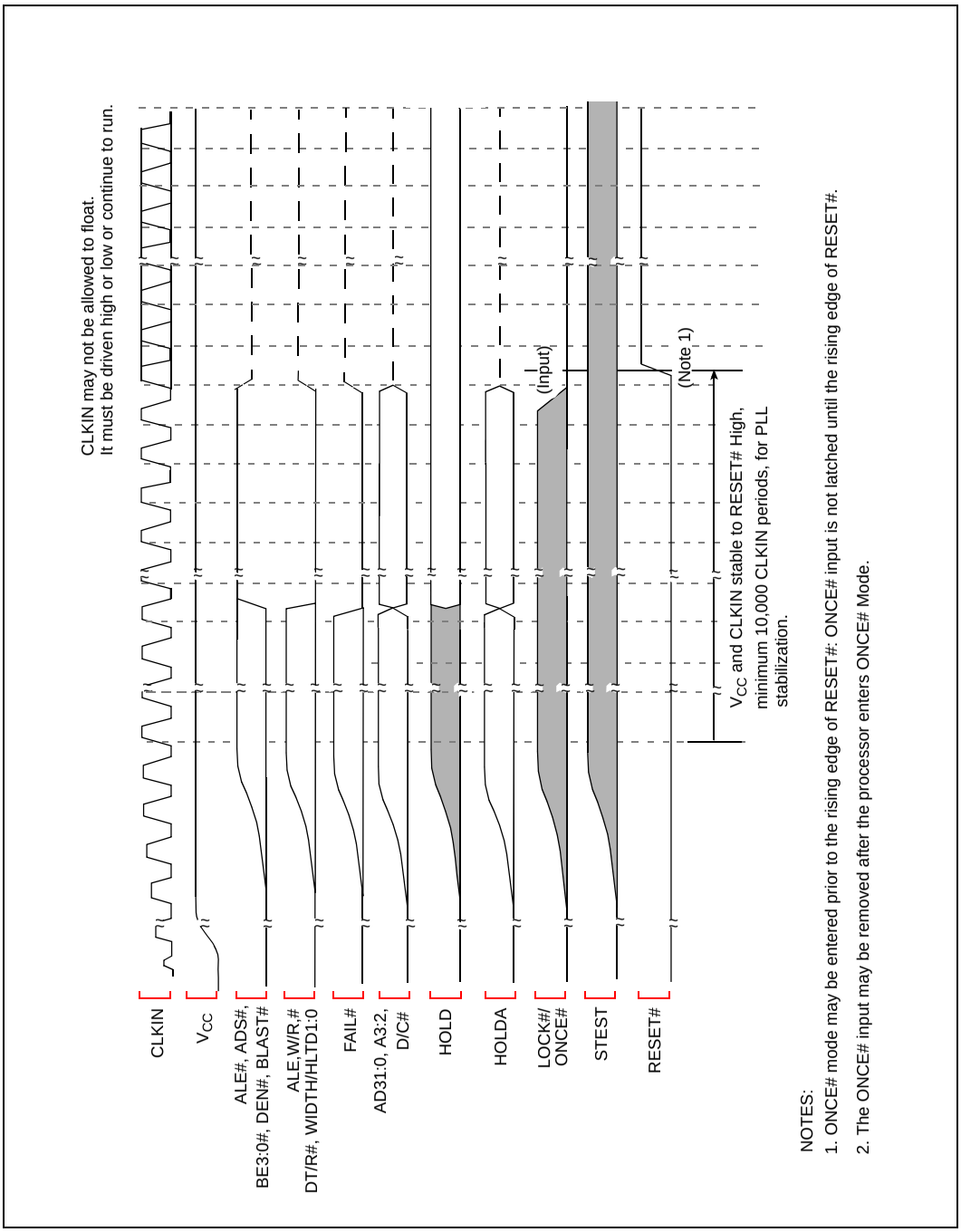


Figure 51. Entering the ONCE State



7.1 Basic Bus States

The bus has five basic bus states: idle (Ti), address (Ta), wait/data (Tw/Td), recovery (Tr), and hold (Th). During system operation, the processor continuously enters and exits different bus states. Figure 52 shows the five bus states.

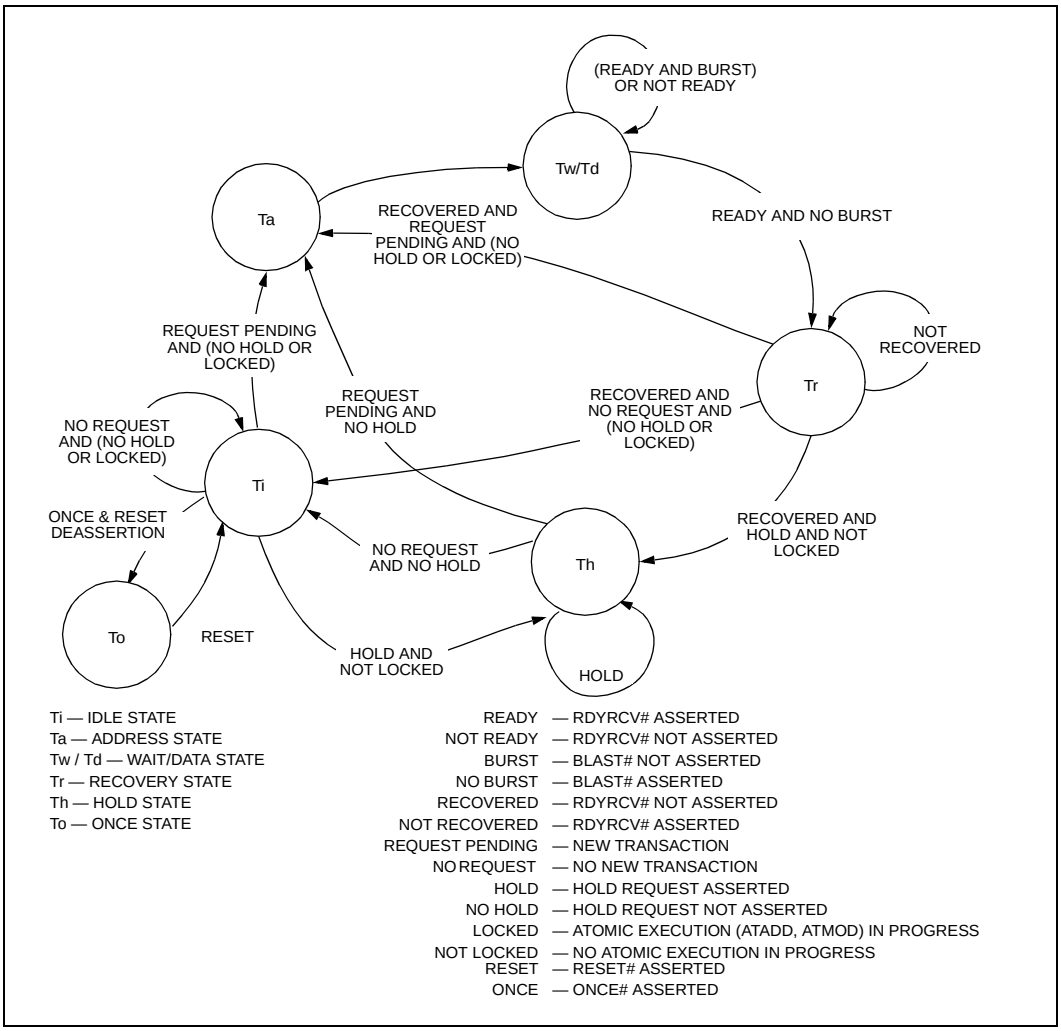
The bus occupies the idle (Ti) state when no address/data transactions are in progress and when RESET# is asserted. When the processor needs to initiate a bus access, it enters the Ta state to transmit the address.

Following a Ta state, the bus enters the Tw/Td state to transmit or receive data on the address/data lines. Assertion of the RDYRCV# input signal indicates completion of each transfer. When data is not ready, the processor may wait as long as necessary for the memory or I/O device to respond.

After the data transfer, the bus exits the Tw/Td state and enters the recovery (Tr) state. In the case of a burst transaction, the bus exits the Td state and re-enters the Td/Tw state to transfer the next data word. The processor asserts the BLAST# signal during the last Tw/Td states of an access. Once all data words transfer in a burst access (up to four), the bus enters the Tr state to allow devices on the bus to recover.

The processor remains in the Tr state until RDYRCV# is deasserted. When the recovery state completes, the bus enters the Ti state when no new accesses are required. When an access is pending, the bus enters the Ta state to transmit the new address.

Figure 52. Bus States with Arbitration



7.2 Boundary-Scan Register

The Boundary-Scan register contains a cell for each pin as well as cells for control of I/O and HIGHZ pins.

Table 42 shows the bit order of the 80960Jx processor Boundary-Scan register. All table cells that contain ‘CTL’ select the direction of bidirectional pins or HIGHZ output pins. When a 1 is loaded into the control cell, the associated pin(s) are HIGHZ or selected as input.

Table 42. Boundary-Scan Register—Bit Order

Bit	Signal	Input/ Output	Bit	Signal	Input/ Output	Bit	Signal	Input/ Output
0	**RDYRCV# (TDI)**	I	24	**DEN#**	O	48	**AD17**	I/O
1	**HOLD**	I	25	**HOLDA**	O	49	**AD16**	I/O
2	**XINT0#**	I	26	**ALE**	O	50	**AD15**	I/O
3	**XINT1#**	I	27	**LOCK#/ ONCE# cell**	Enable cell†	51	**AD14**	I/O
4	**XINT2#**	I	28	**LOCK#/ ONCE#**	I/O	52	**AD13**	I/O
5	**XINT3#**	I	29	**BSTAT**	O	53	**AD12**	I/O
6	**XINT4#**	I	30	**BE0#**	O	54	**AD cells**	Enable cell†
7	**XINT5#**	I	31	**BE1#**	O	55	**AD11**	I/O
8	**XINT6#**	I	32	**BE2#**	O	56	**AD10**	I/O
9	**XINT7#**	I	33	**BE3#**	O	57	**AD9**	I/O
10	**NMI#**	I	34	**AD31**	I/O	58	**AD8**	I/O
11	**FAIL#**	I	35	**AD30**	I/O	59	**AD7**	I/O
12	**ALE#**	O	36	**AD29**	I/O	60	**AD6**	I/O
13	**WIDTH/HLTD1**	O	37	**AD28**	I/O	61	**AD5**	I/O
14	**WIDTH/HLTD0**	O	38	**AD27**	I/O	62	**AD4**	I/O
15	**A2**	O	39	**AD26**	I/O	63	**AD3**	I/O
16	**A3**	O	40	**AD25**	I/O	64	**AD2**	I/O
17	**CONTROL1**	Enable cell†	41	**AD24**	I/O	65	**AD1**	I/O
18	**CONTROL2**	Enable cell†	42	**AD23**	I/O	66	**AD0**	I/O
19	**BLAST#**	O	43	**AD22**	I/O	67	**CLKIN**	I
20	**D/C#**	O	44	**AD21**	I/O	68	**RESET#**	I
21	**ADS#**	O	45	**AD20**	I/O	69	**STEST (TDO)**	I
22	**W/R#**	O	46	**AD19**	I/O			
23	**DT/R#**	O	47	**AD18**	I/O			

† Enable cells are active low.

Table 43. Natural Boundaries for Load and Store Accesses

Data Width	Natural Boundary (Bytes)
Byte	1
Short Word	2
Word	4
Double Word	8
Triple Word	16
Quad Word	16

Table 44. Summary of Byte Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	Byte access	Byte access	Byte access

Table 45. Summary of Short Word Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	Burst of 2 bytes	Short-word access	Short-word access
+1	Two byte accesses	Two byte accesses	Two byte accesses

Table 46. Summary of *n*-Word Load and Store Accesses (*n* = 1, 2, 3, 4)

Address Offset from Natural Boundary in Bytes	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned) (*n* =1, 2, 3, 4)	• *n* burst(s) of 4 bytes	• Case *n*=1: burst of 2 short words • Case *n*=2: burst of 4 short words • Case *n*=3: burst of 4 short words burst of 2 short words • Case *n*=4: 2 bursts of 4 short words	• Burst of *n* word(s)
+1 (*n* =1, 2, 3, 4) +5 (*n* = 2, 3, 4) +9 (*n* = 3, 4) +13 (*n* = 3, 4)	• Byte access • Burst of 2 bytes • *n*-1 burst(s) of 4 bytes • Byte access	• Byte access • Short-word access • *n*-1 burst(s) of 2 short words • Byte access	• Byte access • Short-word access • *n*-1 word access(es) • Byte access
+2 (*n* =1, 2, 3, 4) +6 (*n* = 2, 3, 4) +10 (*n* = 3, 4) +14 (*n* = 3, 4)	• Burst of 2 bytes • *n*-1 burst(s) of 4 bytes • Burst of 2 bytes	• Short-word access • *n*-1 burst(s) of 2 short words • Short-word access	• Short-word access • *n*-1 word access(es) • Short-word access
+3 (*n* =1, 2, 3, 4) +7 (*n* = 2, 3, 4) +11 (*n* = 3, 4) +15 (*n* = 3, 4)	• Byte access • *n*-1 burst(s) of 4 bytes • Burst of 2 bytes • Byte access	• Byte access • *n*-1 burst(s) of 2 short words • Short-word access • Byte access	• Byte access • *n*-1 word access(es) • Short-word access • Byte access
+4 (*n* = 2, 3, 4) +8 (*n* = 3, 4) +12 (*n* = 3, 4)	• *n* burst(s) of 4 bytes	• *n* burst(s) of 2 short words	• *n* word access(es)

Figure 53. Summary of Aligned and Unaligned Accesses (32-Bit Bus)

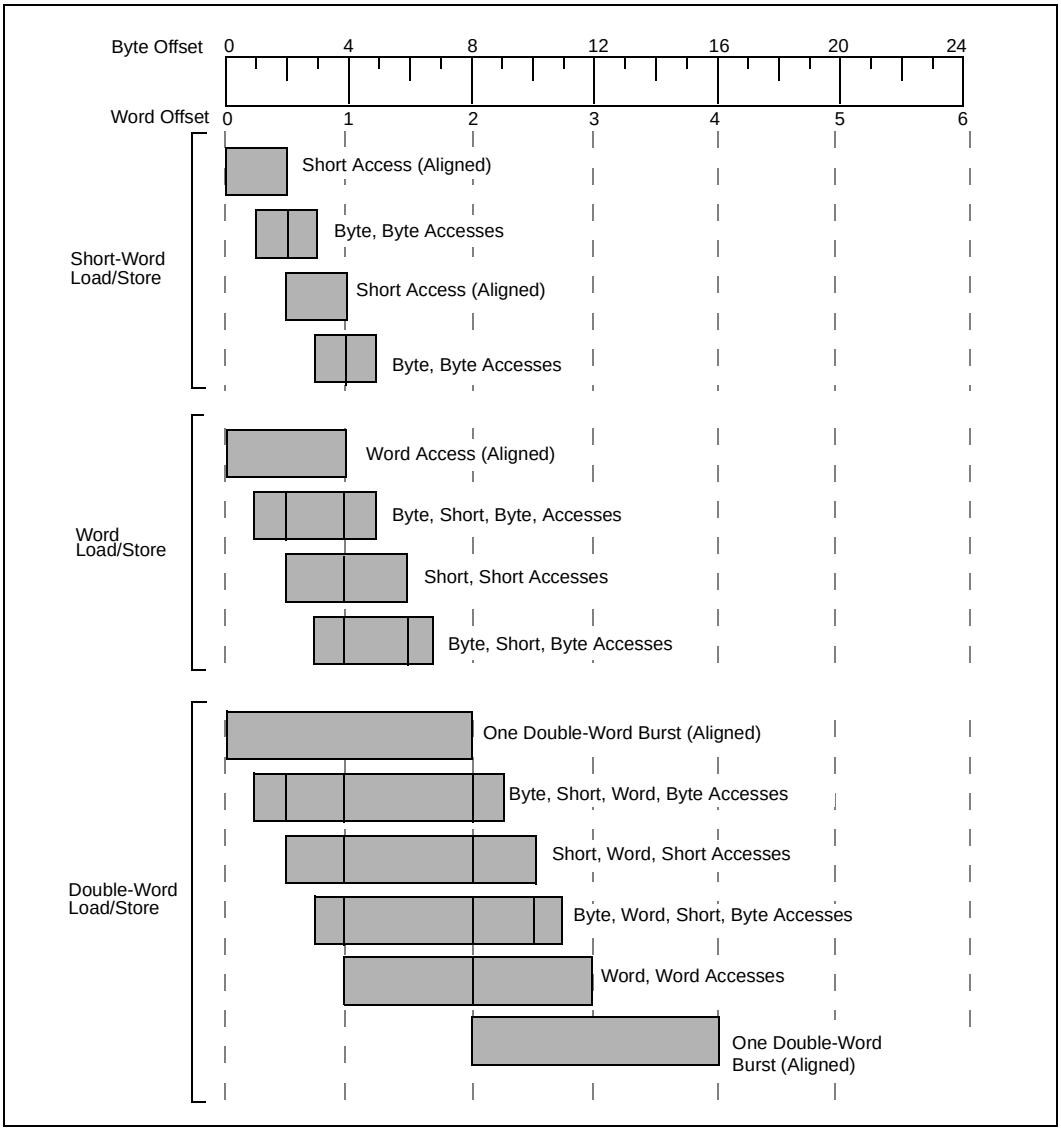
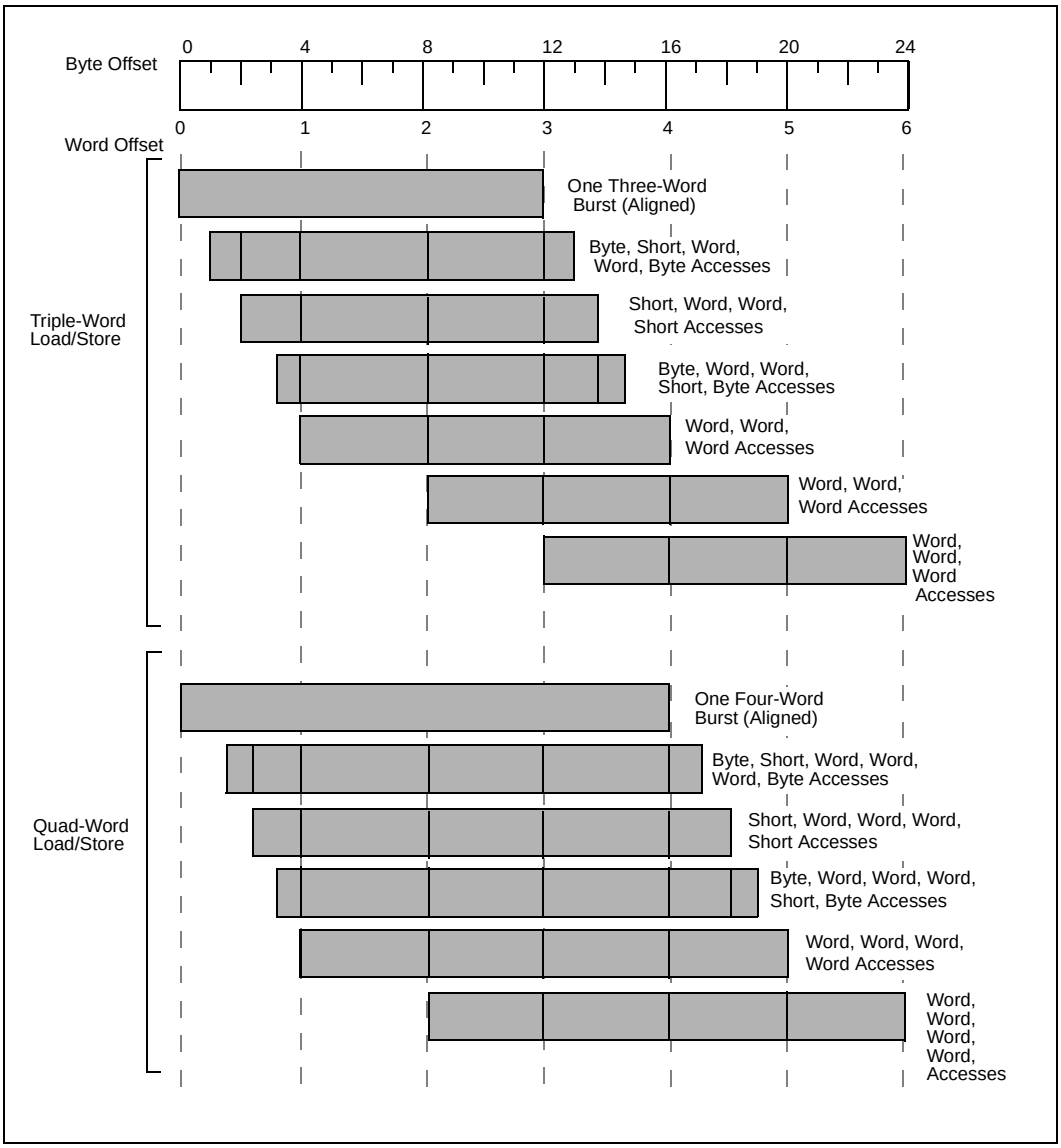


Figure 54. Summary of Aligned and Unaligned Accesses (32-Bit Bus) (Continued)



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