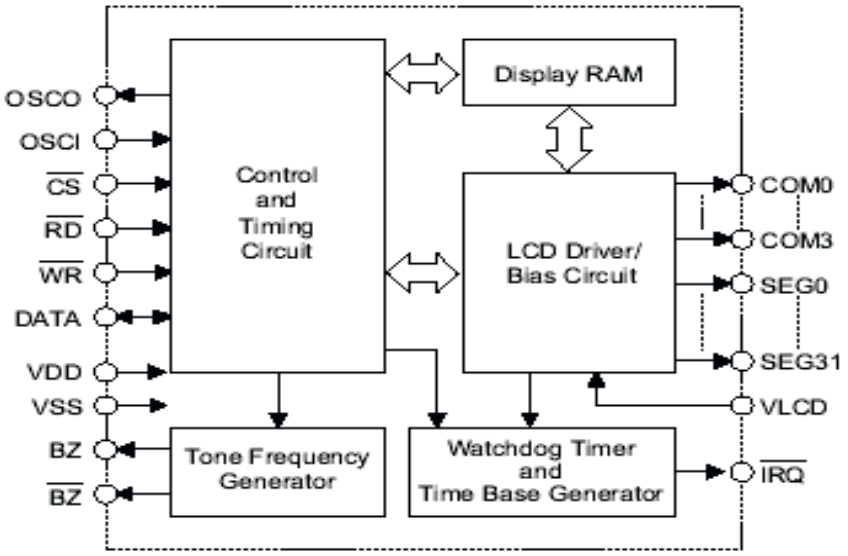
RAM Mapping 32x4 LCD Controller for I/O µC

The IZ1621 is a 128 pattern (32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the IZ1621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the HT1621. The IZ1621 contains a power down command to reduce power consumption.

FEATURES

- Operating voltage : 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32x4 LCD driver
- Built-in 32x4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage

BLOCK DIAGRAM



Note: $\overline{CS}$: Chip selection
$\overline{BZ}$, BZ: Tone outputs
$\overline{WR}$, $\overline{RD}$, DATA: Serial interface
COM0~COM3, SEG0~SEG31: LCD outputs
$\overline{IRQ}$: Time base or WDT overflow output

INTEGRAL

PAD DESCRIPTION

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the IZ1621 are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the IZ1621 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the IZ1621 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the IZ1621 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	V_{SS}	-	Negative power supply, ground
6	OSCO	O	The OSCO and OSCI pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCO and OSCI pads can be left open.
7	OSCI	I	
8	VLCD	I	LCD power input
9	VDD	-	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11, 12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
13÷16	COM0÷COM3	O	LCD common outputs
17÷48	SEG1÷SEG32	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage.....-0.3V÷5.5V

Input Voltage .....V_{SS} -0.3V÷V_{DD}+0.3V

Storage Temperature.....-50°C÷125°C

Operating Temperature.....-25°C÷75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

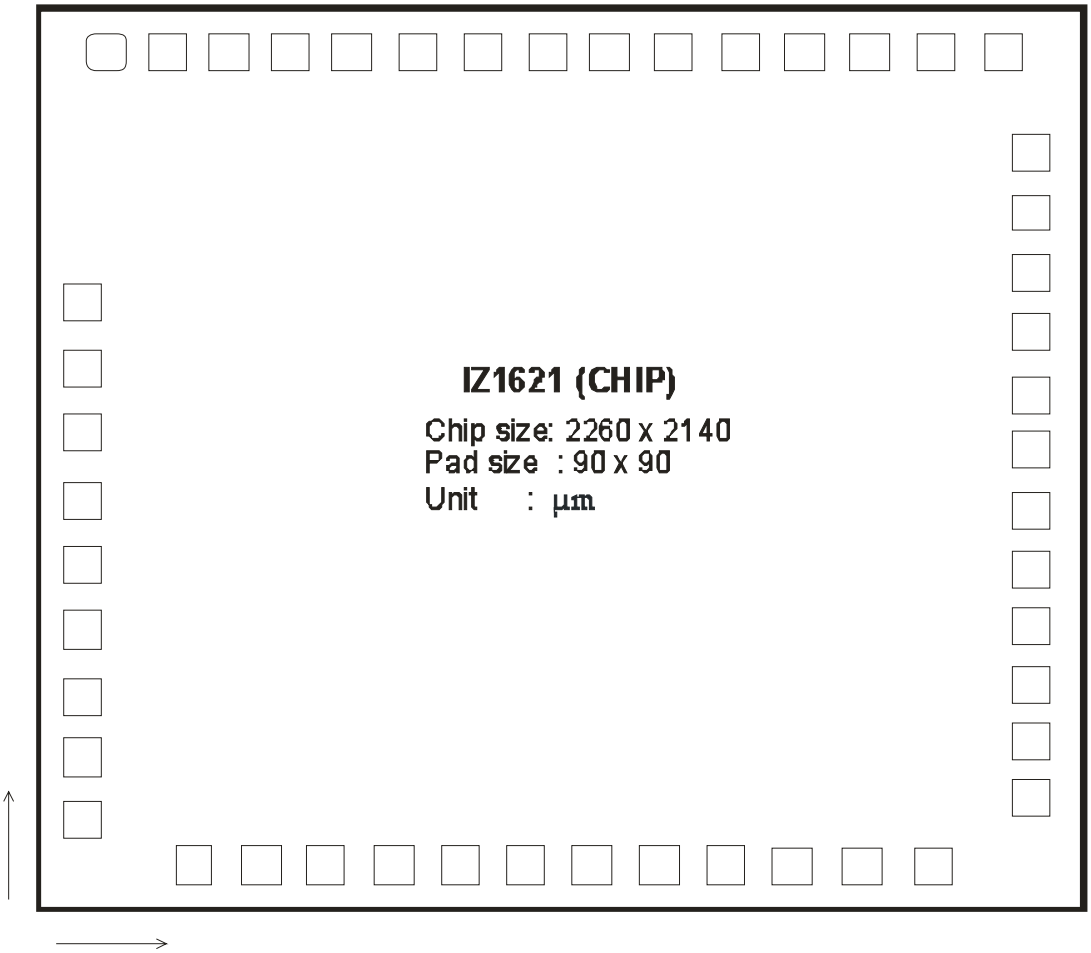
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	300	μA
		5V		—	300	600	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	60	120	μA
		5V		—	120	240	μA
I_{DD3}	Operating Current	3V	No load/LCD ON External clock source	—	100	200	μA
		5V		—	200	400	μA
I_{STB}	Standby Current	3V	No load Power down mode	—	0.1	5	μA
		5V		—	0.3	10	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.5	1.2	—	mA
		5V	V_{OL}=0.5V	1.3	2.6	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	–0.4	–0.8	—	mA
		5V	V_{OH}=4.5V	–0.9	–1.8	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	—	μA
		5V	V_{OL}=0.5V	150	250	—	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	–80	–120	—	μA
		5V	V_{OH}=4.5V	–120	–200	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	—	μA
		5V	V_{OL}=0.5V	120	200	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	–40	–70	—	μA
		5V	V_{OH}=4.5V	–70	–100	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	kΩ
		5V		30	60	100	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	—	256	—	kHz
		5V		—	256	—	kHz
f_{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f_{SYS3}	System Clock	3V	External clock source	—	256	—	kHz
		5V		—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	$f_{SYS1}/1024$	—	Hz
		—	Crystal oscillator	—	$f_{SYS2}/128$	—	Hz
		—	External clock source	—	$f_{SYS3}/1024$	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
f_{TONE}	Tone Frequency	—	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	µs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	—	µs
			Read mode	3.34	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

PAD DIAGRAM



Note: STEP by PAD 125 µm

PAD LOCATION

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	iSC	140	1960	17	SEG32	1140	80	33	SEG16	2080	1537
2	iRD	80	1231	18	SEG31	1280	80	34	SEG15	2080	1667
3	iWR	80	1101	19	SEG30	1420	80	35	SEG14	2000	1960
4	DATA	80	971	20	SEG29	1560	80	36	SEG13	1850	1960
5	V_{SS}	80	841	21	SEG28	1700	80	37	SEG12	1713	1960
6	OSCO	80	711	22	SEG27	1840	80	38	SEG11	1583	1960
7	OSCI	80	581	23	SEG26	2080	237	39	SEG10	1453	1960
8	VLCD	80	451	24	SEG25	2080	367	40	SEG9	1323	1960
9	V_{CC}	80	321	25	SEG24	2080	497	41	SEG8	1193	1960
10	iIRQ	80	191	26	SEG23	2080	627	42	SEG7	1063	1960
11	BZ	300	80	27	SEG22	2080	757	43	SEG6	933	1960
12	iBZ	440	80	28	SEG21	2080	887	44	SEG5	803	1960
13	COM0	580	80	29	SEG20	2080	1017	45	SEG4	673	1960
14	COM1	720	80	30	SEG19	2080	1147	46	SEG3	543	1960
15	COM2	860	80	31	SEG18	2080	1277	47	SEG2	413	1960
16	COM3	1000	80	32	SEG17	2080	1407	48	SEG1	277	1960