

512 x 8-Bit CMOS EEPROM with I²C-Bus Interface

The INF8594E-2 is a 4-Kbit (512 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability. IC works in systems with serial I²C-bus which consists of 2 lines: for data -serial data input/output (SDA) and for clock - serial clock input (SCL). Up to four INF8594E-2 devices may be connected to the I²C-bus. The programming of the array is implemented by electron's tunneling. The programming voltage is generated on-chip, using a voltage multiplier. Power consumption is low owing to the full CMOS technology used. Device is functionally identical to the PCF8594E-2, Philips. IC are made in 8-pin DIP and 8-pin SOP.

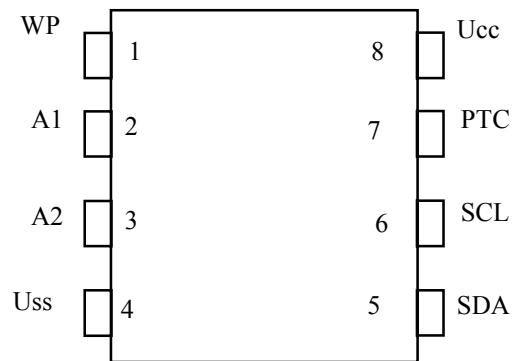
FEATURES

- ◆ Low Power CMOS
 - maximum active current 2.5 mA
 - maximum standby current 10 μA
- ◆ Non-volatile storage of 4-Kbits organized as two pages each 256 x 8-bits
- ◆ Single supply (Ucc=4,5 B - 5,5 B)
- ◆ On-chip voltage multiplier
- ◆ Serial input/output I²C-bus
- ◆ Automatically added word address
- ◆ Internal timer for writing (no external components)
- ◆ 100 000 ERASE/WRITE cycles per byte;
- ◆ Write operations
 - byte write mode
 - 8-byte page write mode (minimizes total write time per byte)
- ◆ Write protection input
- ◆ Read operations
 - sequential read
 - random read
- ◆ Power-on reset
- ◆ High reliability by using a redundant storage code (single bit error correction)
- ◆ Endurance
 - 100 k; T_{amb}=85°C
 - 10 years non-volatile data retention time
- ◆ Pin and Address compatible to PCx8582x-2 Family and PCx8598x2 Family
- ◆ Temperature range: -40°C ÷ +85°C

PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
WP	1	WRITE protection input
A1	2	address input 1
A2	3	address input 2
Uss	4	«GND»
SDA	5	Informational line, input/output
SCL	6	Clock line, input
PTC	7	programming management
Ucc	8	Supply voltage

PIN ASSIGNMENT



Electrical Characteristics

Parameter	Conditions	Symbol	Min.	Max
Supply current READ, mA	$f_{SCL}=100\text{kHz}$ $U_{CC}=5.5\text{B}$	$I_{CC0(RD)}$	-	200
Supply current ERASE/WRITE, mA	$f_{SCL}=100\text{kHz}$ $U_{CC}=5.5\text{B}$	$I_{CC0(EWR)}$	-	2,5
Standby Supply Current, μA	$U_{CC}=5,5\text{B}$	I_{CCS}	-	10.0
Clock input frequency, kHz		f_{SCL}	0	100
E/WR cycle time, ms		$t_{E/WR}$	4	10
PTC input				
Input high voltage, V		U_{IH}	$0,9U_{CC}$	$U_{CC}+0,8$
Input low voltage, V		U_{IL}	-0,8	$0,1U_{CC}$
SCL inputs				
Input high voltage, V		U_{IH}	$0,7U_{CC}$	$U_{CC}+0,8$
Input low voltage, V		U_{IL}	-0,8	$0,3U_{CC}$
Clock input frequency, kHz		f_{SCL}	0	100
Leakage current, μA	$U_i=U_{CC}$ or GND	I_{LI}		$\pm 1\mu\text{A}$
Input capacitance, pF	$U_i=\text{GND}$	C_i		7
SDA input/output				
Low input voltage, V		U_{IL}	-0.8	$0.3U_{CC}$
High input voltage, V		U_{IH}	$0.7U_{CC}$	$U_{CC}+0.8$
Low level output voltage, V	$I_{OL}=3\text{mA}$, $U_{CC}=U_{CCmin}$	U_{OL}		0.4
Output leakage current, μA	$U_{OH}=U_{CC}$	I_{LO}		1
Input capacitance, pF	$U_i=0\text{B}$	C_i		7
Duration of the ERASE/WRITE cycle				
	-internal generator	$t_{E/WR}$	4*	10*
	-external clock signal		4	10
Frequency of the external clock programming signals, kHz		f_p	25	60
Number of the ERASE/WRITE cycles per byte	$T=-40\text{--}+85^\circ\text{C}$, $t_{E/W}=4\text{--}10\text{ MC}$, $T=22^\circ\text{C}$, $t_{E/W}=5\text{ MC}$	$N_{E/W}$	100 000	
	$T = 55^\circ\text{C}$		10 000	
Time of data storage		t_s	10	