IND16305
40-BIT AC-PDP DRIVER

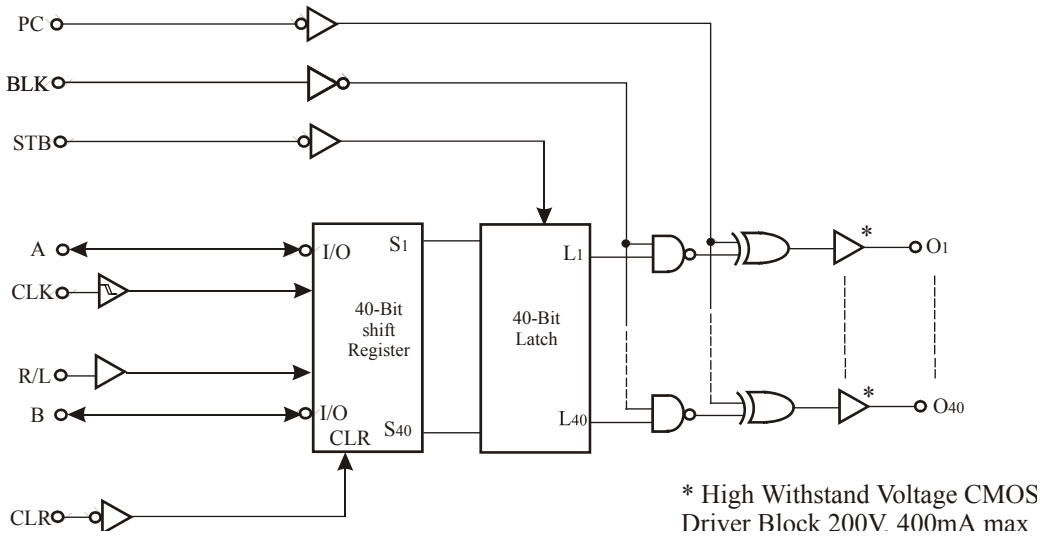
DESCRIPTION

The IND16305 is an AC plasma display panel (PDP) row driver which uses a high withstand voltage CMOS process. It is composed of a 40-bit bidirectional shift register, latch circuit, and a high withstand voltage CMOS driver block. The logic block operates on a 5 V power supply (CMOS level input), enabling direct connection to a microcomputer. The driver block is implemented by means of 200 V, 400 mA high withstand voltage CMOS.

FEATURES

- High withstand voltage CMOS structure
- High withstand voltage, high current output (200 V, 400 mA)
- On-chip 40-bit bidirectional shift register
- Low power dissipation (1 mA max. Ta = –40 to +85 ºC)
- Wide operating temperature range (–40 to +85 ºC)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C, V_{SS1} = V_{SS2} = 0 V)

PARAMETER	SYMBOL	RATING	UNIT
Logic block supply voltage	V_{DD1}	–0.5 to +7.0	V
Driver block supply voltage	V_{DD2}	–0.5 to +200	V
Logic block input voltage	V_I	–0.5 to VDD1 + 0.5	V
Driver block output current	I_O	400*	mA
Permissible package loss	P_D	1000	mW
Operating temperature	Topt.	–40 to +85	°C
Storage temperature	Tsrg.	–65 to +150	°C

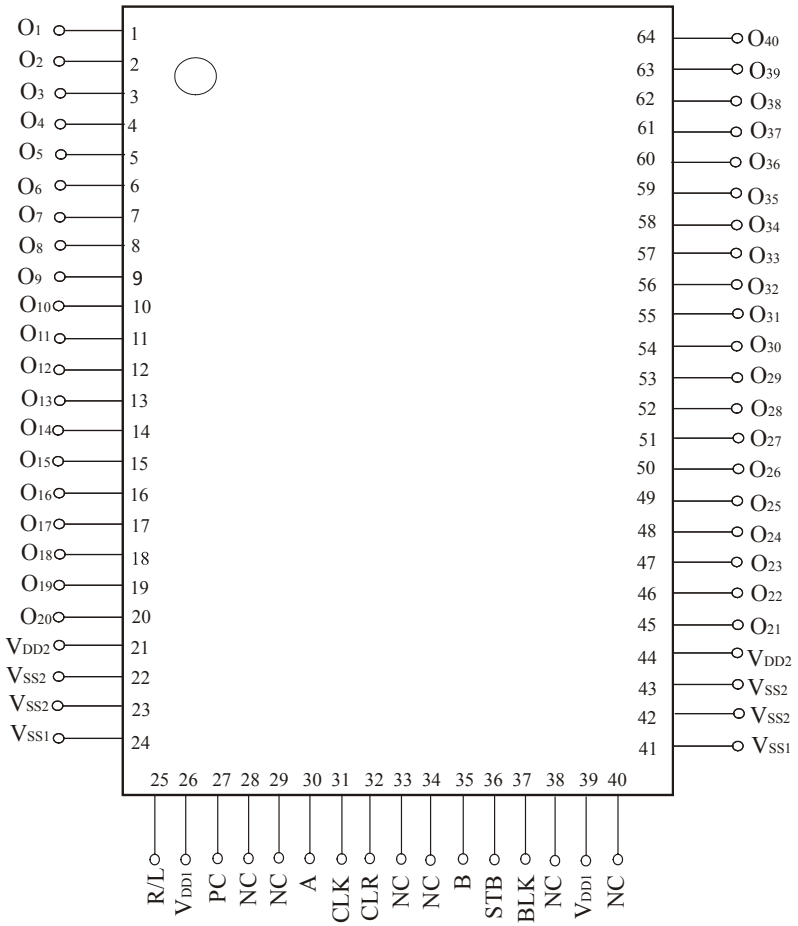
* Duty ≤ 1/40. Derate at -10 mW/°C at T_A = 25°C or higher

RECOMMENDED OPERATING CONDITIONS (Ta = –40 to + 85 °C, V_{SS1} = V_{SS2} = 0 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic block supply voltage	V_{DD1}	4.5	5.0	5.5	V
Driver block supply voltage	V_{DD2}	30		180	V
Input voltage high	V_{IH}	0.8 · V_{DD1}		V_{DD1}	V
Input voltage low	V_{IL}	0		0.2 · V_{DD1}	V
Driver output current	I_O			±300	mA

Korzhenevsky 12, Minsk, 220064, Republic of Belarus
Fax: +375 (17) 278 28 22
Tel: +375 (17) 278 49 09, 212 27 02
Tel/fax: +375 (17) 212 68 53
E-mail: office@bms.by
URL: www.bms.by

PIN CONFIGURATION (Top View)



- Ensure that the V_{DD1}, V_{DD2}, V_{SS1} and V_{SS2} pins are all used, and that V_{SS1} and V_{SS2} are used at the same potential (connect at same point near IC).
- Pin 33 is connected to the lead frame, and must therefore be left open.

DESCRIPTION OF PINS

Pin Symbol	Pin Name	Pin No.	Description
BLK	Output blank input	37	See truth table
A	RIGHT data input/output	30	Serial data input/output* When R/L = H A: Input B:Output
B	LEFT data input/output	35	When R/L = L A: Output B: Input
CLK	Clock input	31	Shift executed on rise
STB	Latch enable input	36	H: Latch, L: Data-through
R/L	Shift direction control input	25	H: Right shift modeA→O_1□···O_{40}→B L : Left shift mode B→O_{40}→···O_1□A
CLR	Clear input	32	L: Shift register ALL L
PC	Polarity reversal input	27	See truth table
O_1 to O_{40}	High withstand voltage outputs	1 to 20 45 to 64	200 V, 400 mA max.
V_{DD1}	Logic block power supply	26, 39	5 V ± 10 %
V_{DD2}	Driver block power supply	21, 44	30 V to 180 V
V_{SS1}	Logic block ground	24, 41	Connect to system GND
V_{SS2}	Driver block ground	22, 23, 42, 43	Connect to system GND at same point.
NC	Unused pins	28, 29, 33,	Non-connection
		34, 38, 40	Ensure that pin 33 is left open.

* Data resulting from inversion of the data input is input to the shift register, and data resulting from inversion of the shift register data is output to the output.

IND16305

ELECTRICAL SPECIFICATIONS (T_a = 25 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 180 V, V_{SS1} = V_{SS2} = 0 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Output voltage high	V_{OH1}	0.9 · V_{DD1}		V	Logic I_{OH} = –1 mA
Output voltage low	V_{OL1}		0.1 · V_{DD1}	V	Logic I_{OL} = 1 mA
Output voltage high	V_{OH21}	160		V	O_1 to O_{40}, I_{OH} = –150 mA
	V_{OH22}	140		V	O_1 to O_{40}, I_{OH} = –300 mA
Output voltage low	V_{OL21}		20	V	O_1 to O_{40}, I_{OL} = 150 mA
	V_{OL22}		40	V	O_1 to O_{40}, I_{OL} = 300 mA
Input current	I_I		±1	uA	V_I = V_{DD1} or V_{SS1}
Input voltage high	V_{IH}	0.8 · V_{DD1}		V	
Input voltage low	V_{IL}		0.2 · V_{DD1}	V	
Static comsumption current	I_{DD1}		100	uA	Logic Ta = –40 to +85 °C
	I_{DD1}		10	uA	Logic Ta = 25 °C
	I_{DD2}		1	mA	Driver Ta = –40 to +85 °C
	I_{DD2}		100	uA	Driver Ta = 25 °C

SWITCHING CHARACTERISTICS (T_a = 25 °C, V_{DD1} = 5 V, V_{DD2} = 180 V, Logic C_L = 15 pF, Driver C_L = 50 pF)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Transmission delay time	t_{PHL1}		120	ns	CLK →A/B
	t_{PLH1}		120	ns	
	t_{PLH2}		120	ns	CLR →A/B
	t_{PHL3}		200	ns	CLK →O1 to O40
	t_{PLH3}		200	ns	
	t_{PHL4}		200	ns	STB →O1 to O40
	t_{PLH4}		200	ns	
	t_{PHL5}		220	ns	BLK →O1 to O40
	t_{PLH5}		220	ns	
	t_{PHL6}		220	ns	PC →O1 to O40
	t_{PLH6}		220	ns	
Rise time	t_{TLH}		100	ns	O1 to O40
Fall time	t_{THL}		100	ns	O1 to O40
Maximum clock frequency (DATA)	$f_{max.}$	15		MHz	Duty = 50 %
Input capacitance	C_I		15	pF	

REQUIRED TIMING CONDITIONS (T_a = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS
Clock pulse width	PW_{CLK}	30		ns	
Strobe pulse width	PW_{STB}	60		ns	
Blank pulse width	PW_{BLK}	200		ns	
PC pulse width	PW_{PC}	300		ns	
Clear pulse width	PW_{CLR}	120		ns	
Data setup time	t_{SETUP}	20		ns	
Data hold time	t_{HOLD}	5		ns	
Clock-strobe time	$t_{CLK-STB}$	120		ns	CLK ↑→STB ↑

Korzhenevsky 12, Minsk, 220064, Republic of Belarus
Fax: +375 (17) 278 28 22
Tel: +375 (17) 278 49 09, 212 27 02
Tel/fax: +375 (17) 212 68 53
E-mail: office@bms.by
URL: www.bms.by

TRUTH TABLE 1 (Shift Register Block)

R/L	CLK	A	B	Shift Register
H	↑	Input	Output	Right shift execution
H	H or L			Hold
L	↑	Output	Input	Left shift execution
L	H or L			Hold

TRUTH TABLE 2 (Latch Block)

STB	Operation
H	Data immediately prior to STB becoming H is held
L	Shift register data is output

TRUTH TABLE 3 (Driver Block)

DATA	BLK	PC	On	Remarks
H	L	L	H	
L	L	L	L	
H	L	H	L	
L	L	H	H	
X	H	L	H	All outputs H
X	H	H	L	All outputs L

H→: High level

L→: Low level

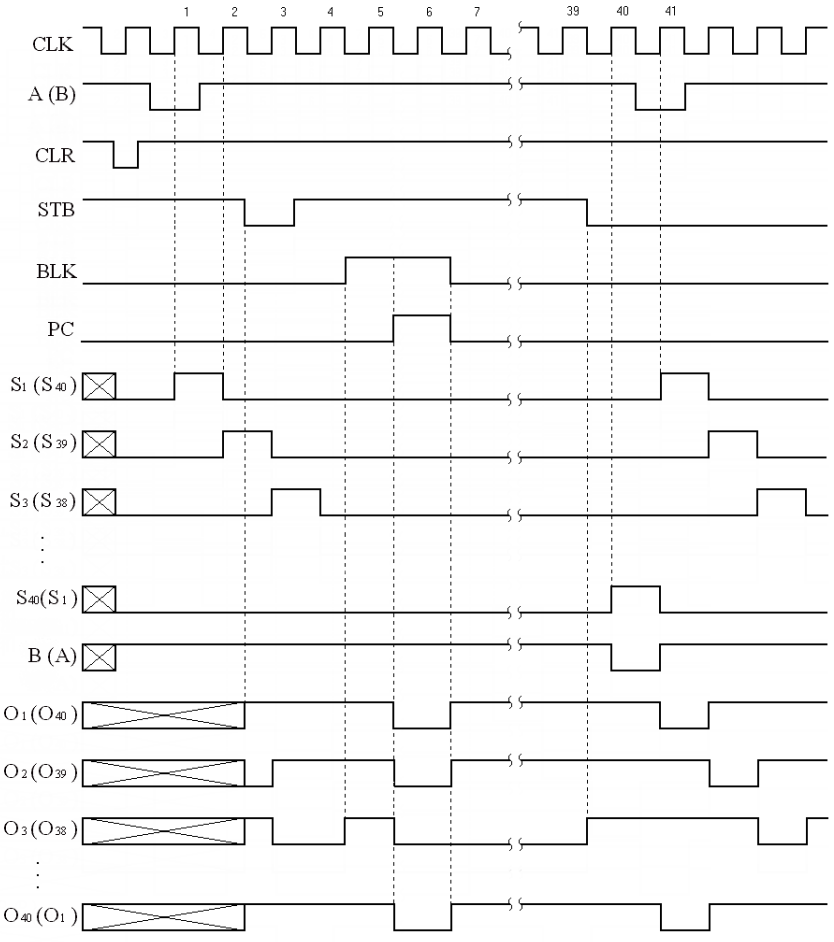
X→: H or L

DATA: Data input to A (B)

Caution To prevent latch up breakdown, the power should be turned on in the order V_{DD1}, logic signal, V_{DD2}. It should be turned off in the opposite order.

TIMING CHART

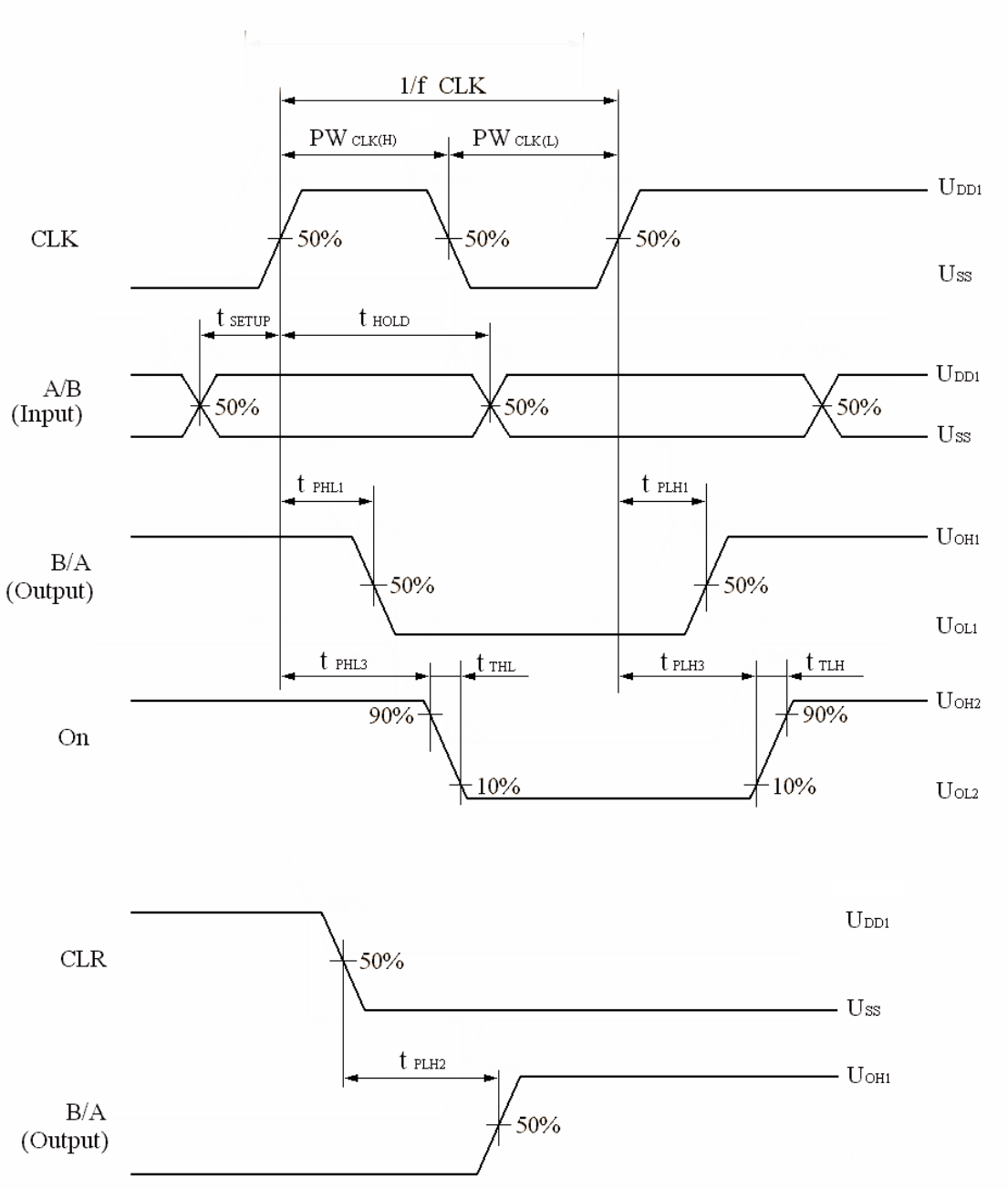
( ): When R/L=L



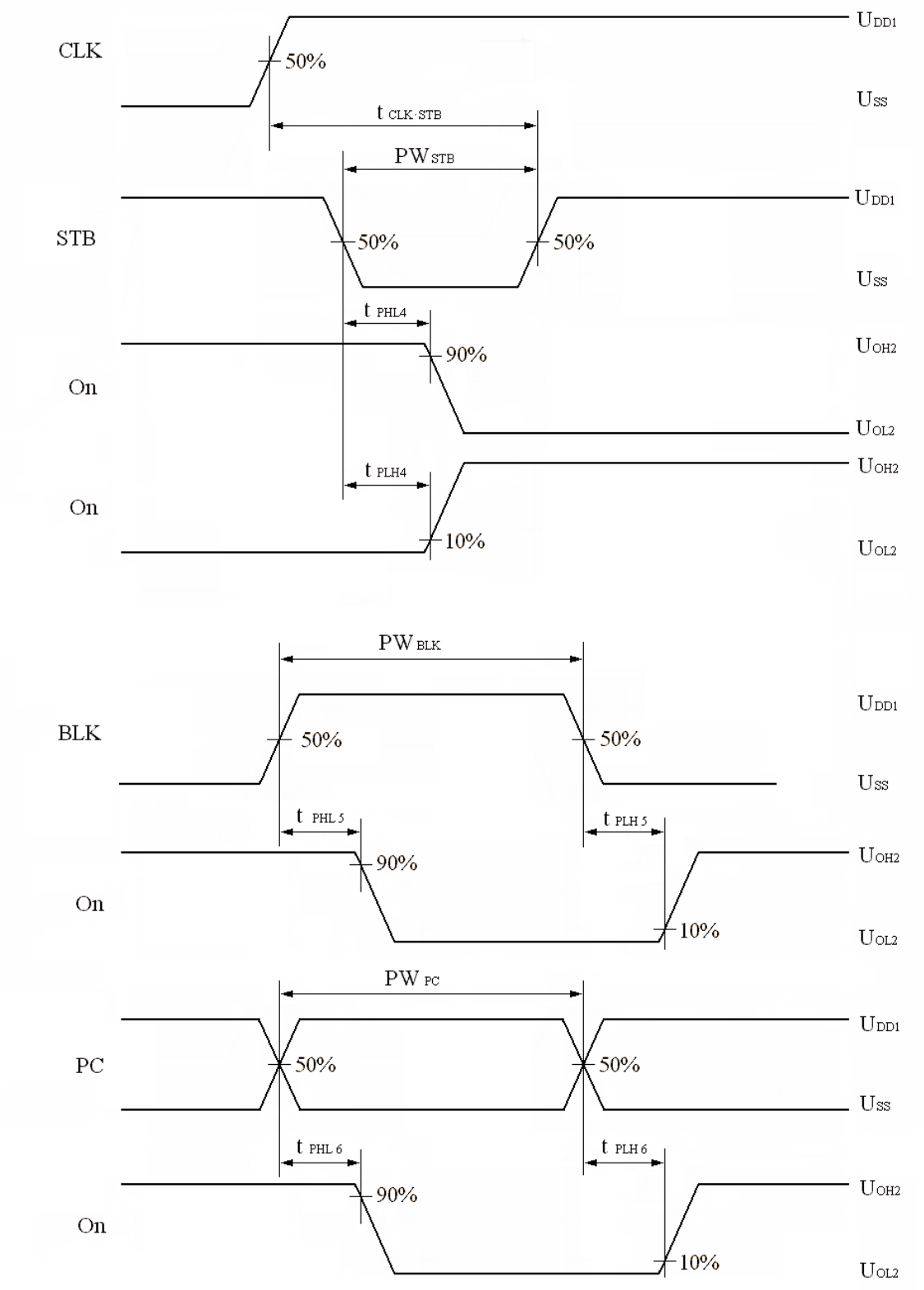
Fax: +375 (17) 278 28 22
Tel: +375 (17) 278 49 09, 212 27 02
Tel/fax: +375 (17) 212 68 53
E-mail: office@bms.by
URL: www.bms.by

IND16305

SWITCHING CHARACTERISTIC WAVEFORMS

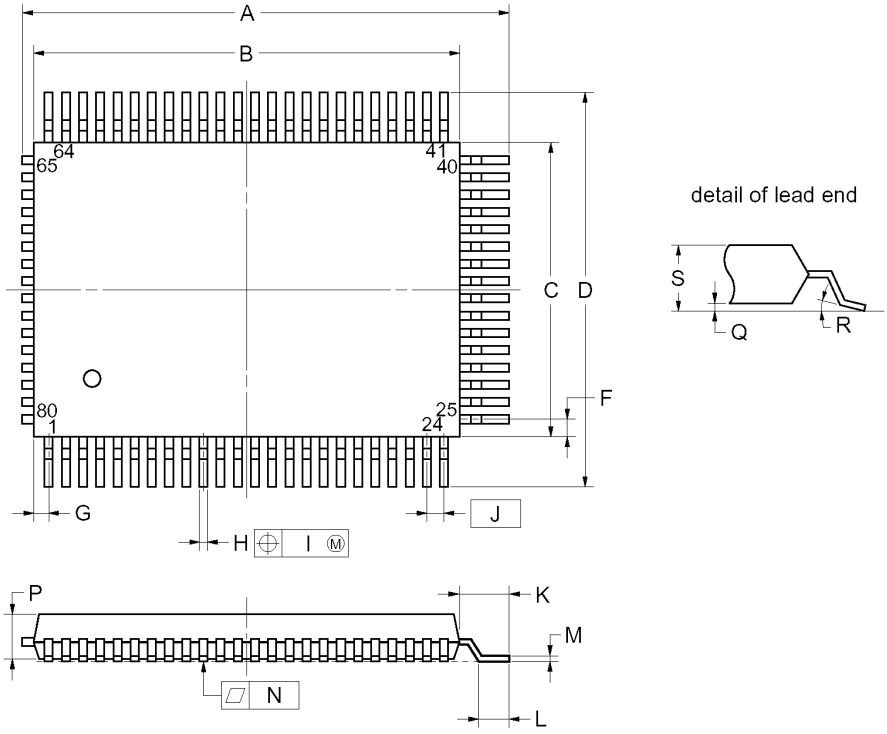


Korzhenevsky 12, Minsk, 220064, Republic of Belarus
Fax: +375 (17) 278 28 22
Tel: +375 (17) 278 49 09, 212 27 02
Tel/fax: +375 (17) 212 68 53
E-mail: office@bms.by
URL: www.bms.by



Korzhenevsky 12, Minsk, 220064, Republic of Belarus
Fax: +375 (17) 278 28 22
Tel: +375 (17) 278 49 09, 212 27 02
Tel/fax: +375 (17) 212 68 53
E-mail: office@bms.by
URL: www.bms.by

80 PIN PLASTIC QFP (THREE DIRECTIONS) (14x20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.3±0.4	0.878±0.016
B	20.0±0.2	0.795±0.009
C	14.0±0.2	0.551±0.009
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	0.014±0.005
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071+0.009
L	0.8±0.2	0.031±0.009
	+0.10	+0.004
M	0.15	0.006
	–0.05	–0.003
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.
		P80GF-80-3L9-2