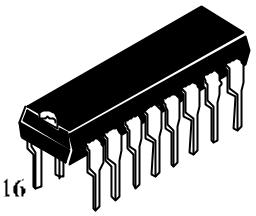
IN74LV174

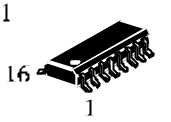
Hex D-type flip-flop with reset; positive edge-trigger

The 74LV174 is a low–voltage Si–gate CMOS device and is pin and function compatible with the 74HC/HCT174.
The 74LV174 has six edge–triggered D–type flip–flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip–flops simultaneously.
The register is fully edge–triggered. The state of each D input, one set–up time prior to the LOW–to–HIGH clock transition, is transferred to the corresponding output of the flip–flop.
A LOW level on the MR input forces all outputs LOW, independently of clock or data inputs.
The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.2 to 5.5 V
- Low input current: 1.0 µÀ; 0.1 µÀ at Ò = 25 °Ñ
- Output current: 6 mA at Vcc = 3.0 V; 12 mA at Vcc = 4.5 V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC

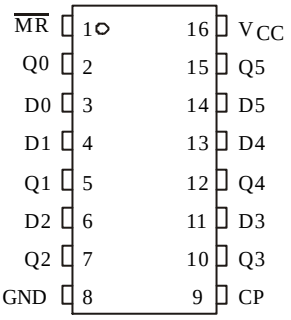


D SUFFIX
SOIC

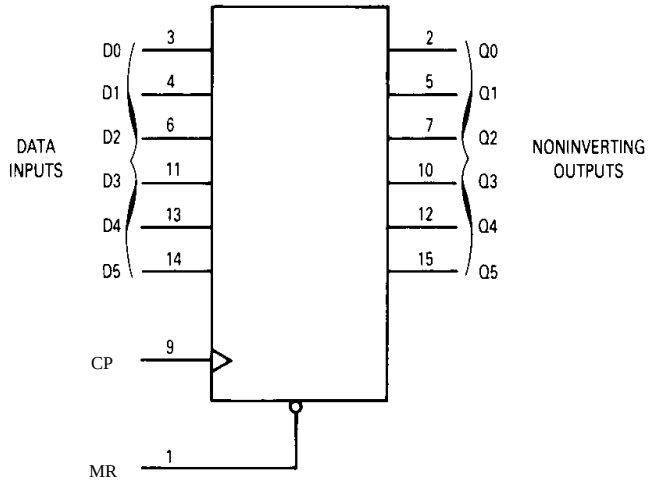
ORDERING INFORMATION

IN74LV174N Plastic
IN74LV174D SOIC
IZ74LV174 Chip
T_A = -40° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 08 = GND

FUNCTION TABLE

Inputs			Outputs
$\overline{MR}$	CP	Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	no change
H	↓	X	no change

H= high level
L = low level
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *1	Input diode current	±20	mA
I_{OK} *2	Output diode current	±50	mA
I_O *3	Output source or sink current	±25	mA
I_{CC}	V_{CC} current	±50	mA
I_{GND}	GND current	±50	mA
P_D	Power dissipation per package: *4 Plastic DIP SO	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	5.5	V
V_{IN}	DC Input Voltage		0	V_{CC}	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	1.0 Â ≤V_{CC} <2.0 Â 2.0 Â ≤V_{CC} <2.7 Â 2.7 Â ≤V_{CC} <3.6 Â 3.6 Â ≤V_{CC} ≤5.5 Â	0 0 0 0	500 200 100 50	ns/V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	V
V_{IL}	LOW level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -100 µA	1.2 2.0 2.7 3.0 3.6 4.5 5.5	1.05 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -6 mA	3.0	2.48	-	2.34	-	2.20	-	V
		$V_I = V_{IH}$ or V_{IL} I_O = -12 mA	4.5	3.70	-	3.60	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 100 µA	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.15 0.15 0.15 0.15 0.15 0.15 0.15	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	V
		$V_I = V_{IH}$ or V_{IL} I_O = 6 mA	3.0	-	0.33	-	0.40	-	0.50	V
		$V_I = V_{IH}$ or V_{IL} I_O = 12 mA	4.5	-	0.40	-	0.55	-	0.65	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	5.5	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 µA	5.5	-	8.0	-	80	-	160	µA
I_{CC1}	Additional quiescent supply	$V_I = V_{CC}$ – 0.6 V	2.7 3.6	-	0.2 0.2	-	0.5 0.5	-	0.85 0.85	mA

	current per input									

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, R_L = 1 kΩ, t_r=t_f=2.5 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay CP to Qn	V_I = 0 V or V_{CC} Figure 1, 4	1.2 2.0 2.7 3.0 4.5	- - - - -	200 34 24 20 17	- - - - -	230 43 31 25 21	- - - - -	260 53 39 31 26	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	V_I = 0 V or V_{CC} Figure 2, 4	1.2 2.0 2.7 3.0 4.5	- - - - -	160 34 24 20 17	- - - - -	190 43 31 25 21	- - - - -	220 53 39 31 26	ns
t_W	Clock pulse width HIGH or LOW	V_I = 0 V or V_{CC} Figure 1, 4	1.2 2.0 2.7 3.0 4.5	100 28 21 17 14	- - - - -	140 34 25 20 17	- - - - -	180 41 30 24 20	- - - - -	ns
t_W	Master reset pulse width LOW	V_I = 0 V or V_{CC} Figure 1, 4	1.2 2.0 2.7 3.0 4.5	100 28 21 17 14	- - - - -	140 34 25 20 17	- - - - -	180 41 30 24 20	- - - - -	ns
t_{REM}	Removal time $\overline{MR}$ to CP	V_I = 0 V or V_{CC} Figure 3, 4	1.2 2.0 2.7 3.0 4.5	40 19 13 11 9	- - - - -	60 22 16 13 11	- - - - -	80 26 19 15 13	- - - - -	ns
t_{SU}	Set-up time Dn to CP	V_I = 0 Â or V_{CC} Đèñóí î ê 3, 4	1.2 2.0 2.7 3.0 4.5	50 5 5 5 5	- - - - -	50 5 5 5 5	- - - - -	50 5 5 5 5	- - - - -	ns
t_h	Hold time Dn to CP	V_I = 0 Â or V_{CC} Đèñóí î ê 2, 4	1.2 2.0 2.7 3.0 4.5	50 5 5 5 5	- - - - -	50 5 5 5 5	- - - - -	50 5 5 5 5	- - - - -	ns
C_I	Input capacitance	Ò$_A$ = 25°C	5.0	-	7.0	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per flip-flop)	V_I = 0 V or V_{CC} T_A = 25°C	5.5	-	34	-	-	-	-	pF
fmax	Maximum clock pulse frequency	V_I = 0 Â or V_{CC} Đèñóí î ê 1	1.2 2.0 2.7 3.0 4.5	- - - - -	2.0 16 22 27 32	- - - - -	1.0 14 19 24 27	- - - - -	1.0 12 16 20 24	MHz

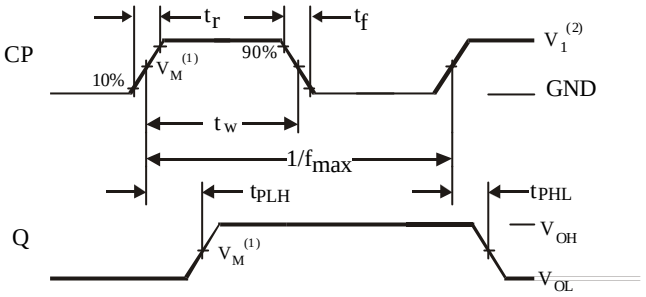


Figure 1. Switching Waveforms

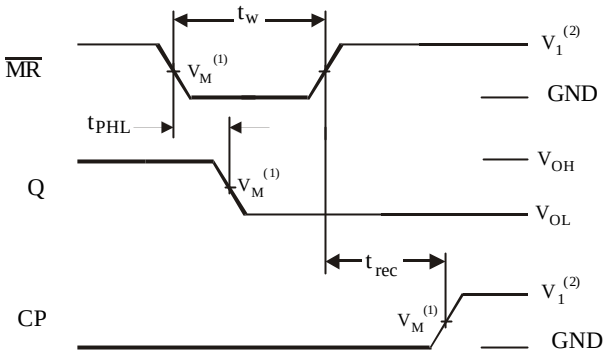


Figure 2. Switching Waveforms

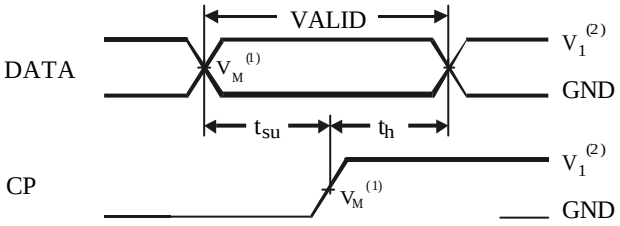
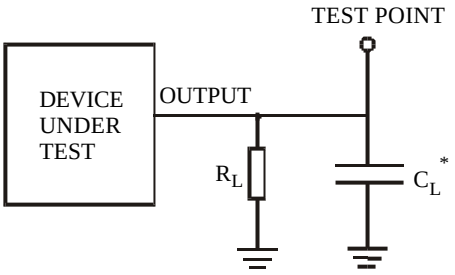


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

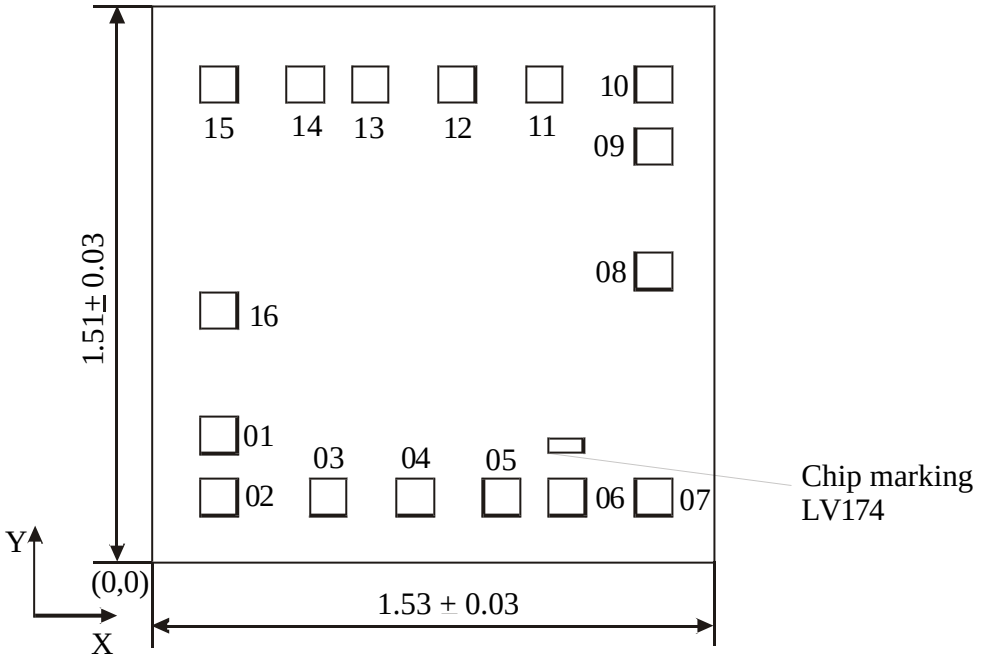
Figure 4. Test Circuit

Note:

(1) $V_M = 1.5$ V at $V_{CC} = 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} = 1.2$ V, 2.0 V, 3.0 V, 4.5 V

(2) $V_1 = V_{CC}$ at $V_{CC} = 1.2$ V, 2.0 V, 2.7 V, 4.5 V
$V_1 = 2.7$ V at $V_{CC} = 3.0$ V

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=1.080, y=0.296

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	$\overline{MR}$	0.132	0.295	0.100 x 0.100
02	Q0	0.132	0.127	0.100 x 0.100
03	D0	0.430	0.127	0.100 x 0.100
04	D1	0.667	0.127	0.100 x 0.100
05	Q1	0.902	0.127	0.100 x 0.100
06	D2	1.080	0.127	0.100 x 0.100
07	Q2	1.315	0.127	0.100 x 0.100
08	GND	1.315	0.741	0.100 x 0.100
09	CP	1.315	1.079	0.100 x 0.100
10	Q3	1.315	1.247	0.100 x 0.100
11	D3	1.017	1.247	0.100 x 0.100
12	Q4	0.780	1.247	0.100 x 0.100
13	D4	0.545	1.247	0.100 x 0.100
14	D5	0.367	1.247	0.100 x 0.100
15	Q5	0.132	1.247	0.100 x 0.100
16	V_{CC}	0.132	0.633	0.100 x 0.100

Note: Pad location is given as per metallization layer