

IN472-3

Liquid Crystal Display Controller

The IN472-3-3 Liquid Crystal Display (LDC) Controller is a peripheral member of the COPS™ family, fabricated using CMOS technology. The IN472-3 drives a multiplexed liquid crystal directly. Data is loaded serially and is held in internal latches. The In472-3 contains an on-chip oscillator and generates all the multi-level waveforms for back-planes and segment outputs on a triplex display. One IN472-3 can drive 36 segments multiplexed as 3 x 12 (4½ digit display). Two IN472-3 devices can be used together to drive 72 segments (3 x 24) which could be an 8½ digit display.

- Direct interface to TRIPLEX LCD
- Low power dissipation (100 µW typ.)
- Low cost
- Compatible with all COP400 processors
- Needs no refresh from processor
- On-chip oscillator and latches
- Expandable to longer displays
- Software compatible with COP470 V.F.Display Driver Chip
- Operates from display voltage
- MICROWIRE™ compatible serial I/O
- 20-pin Dual-In-Line package

Pin Description

Pin	Description
CS	Chip select
V _{DD}	Power supply (display voltage)
GND	Ground
DI	Serial data input
SK	Serial clock input
BP _A	Display backplane A (or oscillator in)
BP _B	Display backplane B
BP _C	Display backplane C (or oscillator out)
SA1~SA4	12 multiplexed outputs

N SUFFIX PLASTIC

DW SUFFIX SOIC

ORDERING INFORMATION
 IN472-3N Plastic
 IN472-3DW SOIC
 T_A = 0° to 70° C
 for all packages

PIN ASSIGNMENT

SB1	1 ●	20	SA4
SC3	2	19	SA3
SB3	3	18	SC1
$\overline{\text{CS}}$	4	17	BPB
V _{DD}	5	16	BPC
GND	6	15	BPA
DI	7	14	SK
SA2	8	13	SC4
SB4	9	12	SC2
SB2	10	11	SA1

DC ELECTRICAL CHARACTERISTICS (GND=0 V, V_{DD}=3.0 V to 5.5 V, T_A= 0°C to 70°C
(depends on display characteristics))

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V _{DD}	Power Supply Voltage		3.0	5.5	V
I _{DD}	Power Supply Current (Note 1)	V _{DD} =5.5 V		250	μA
V _{IL}	Input Levels DI, SK, CS			0.8	V
V _{IH}			0.7 V _{DD}	V _{DD}	
V _{IL}	BPA (as Osc. in)			0.6	V
V _{IH}			V _{DD} -0.6	V _{DD}	
V _{OL}	Output Levels, BPC (as Osc. Out)			0.4	V
V _{OH}			V _{DD} -0.4	V _{DD}	
V _{BPA,BPB,BPC ON}	Backplane Outputs (BPA,BPB,BPC)	During BP + Time	V _{DD} -ΔV	V _{DD}	V
V _{BPA,BPB,BPC OFF}			1/3V _{DD} -ΔV	1/3V _{DD} +ΔV	
V _{BPA,BPB,BPC ON}	Backplane Outputs (BPA,BPB,BPC)	During BP - Time	0	ΔV	V
V _{BPA,BPB,BPC OFF}			2/3V _{DD} -ΔV	2/3V _{DD} +ΔV	
V _{SEG ON}	Segment Outputs (SA ₁ ~ SA ₄)	During BP + Time	0	ΔV	V
V _{SEG OFF}			2/3V _{DD} -ΔV	2/3V _{DD} +ΔV	
V _{SEG ON}	Segment Outputs (SA ₁ ~ SA ₄)	During BP - Time	V _{DD} -ΔV	V _{DD}	V
V _{SEG OFF}			1/3V _{DD} -ΔV	1/3V _{DD} +ΔV	
	Internal Oscillator Frequency		15	80	kHz
	Frame Time (Int. Osc. ÷ 192)		2.4	12.8	ms
1/T _{SCAN}	Scan Frequency		39	208	Hz
	SK Clock Frequency		4	250	kHz
	SK Width		1.7		μs
t _{SETUP}	DI Data Stup		1.0		μs
t _{HOLD}	DI Data Hold		100		ns
t _{SETUP}	CS		1.0		μs
t _{HOLD}			1.0		
	Output Loading Capacitance			100	pF

Note 1: Power supply current as measured in stand-alone mode with all outputs open and all inputs at V_{DD}.

Note 2: ΔV - 0.05V_{DD}.

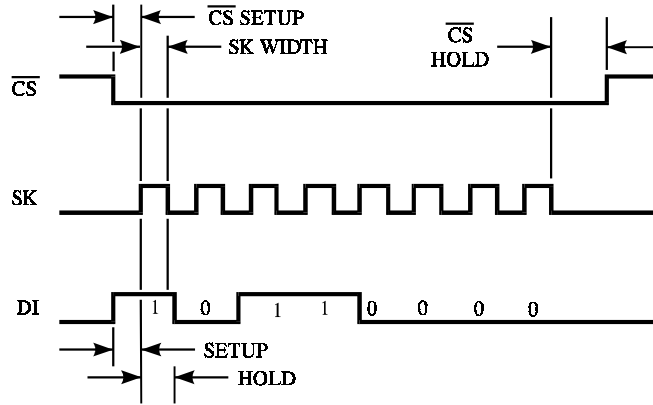


Figure 1. Serial Load Timing Diagram

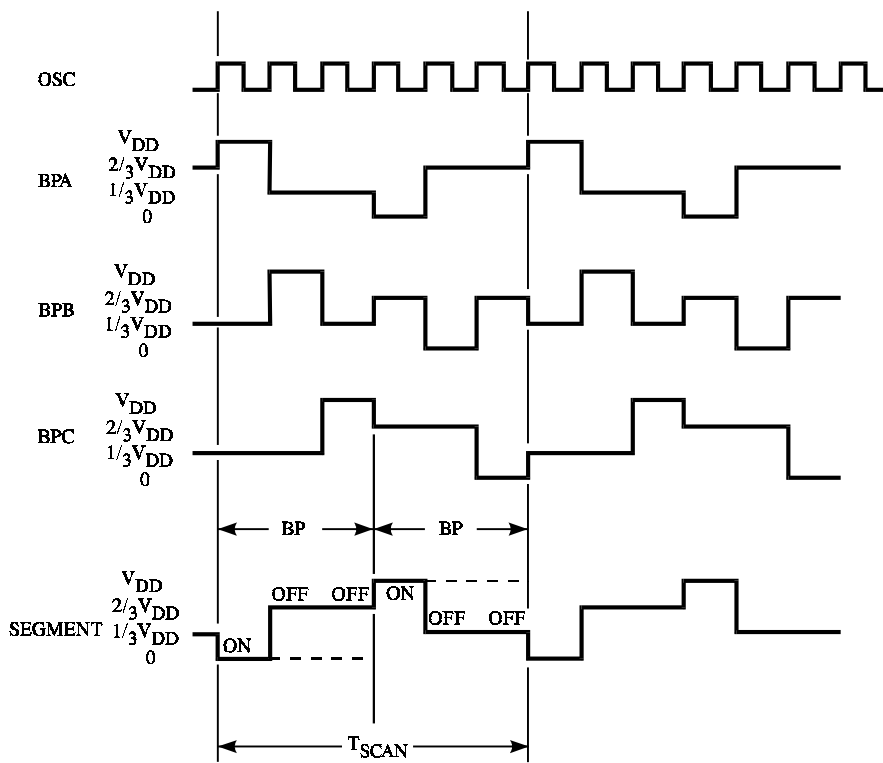


Figure 2. Backplane and Segment Waveforms