Data Sheet, Rev. 1.10, Jan. 2006

HYS64T32000HU–[2.5F/.../5]–B
HYS[64/72]T64000HU–[2.5F/.../5]–B
HYS[64/72]T128020HU–[2.5F/.../5]–B

240-Pin unbuffered DDR2 SDRAM Modules

DDR2 SDRAM
UDIMM SDRAM
RoHS Compliant

Memory Products

infineon

Never stop thinking

Edition 2006-01

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HYS64T32000HU–[2.5F/…/5]–B,
HYS[64/72]T64000HU–[2.5F/…/5]–B,
HYS[64/72]T128020HU–[2.5F/…/5]–B

Revision History: 2006-01, Rev. 1.10

Previous Version:

Page	Subjects (major changes since last revision)
7	added PC2-6400-555 product types
42	added I_{DD} currents
51	added SPD codes for PC2-6400-555 product types
48	added I_{DD} Measurement Contions for DDR2-800D
26	added Speed Grade bin for DDR2-800D

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Table of Contents

1 Overview

This chapter gives an overview of the 240-Pin unbuffered DDR2 SDRAM Modules product family and describes its main characteristics.

1.1 Features

Feature list and performance tables

- 240-Pin PC2–6400, PC2–5300, PC2–4200 and PC2–3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 32M × 64, 64M × 64, 64M × 72, 128M × 64 and 128M ×72 module organization,and 32M × 16, 64M × 8 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512-Mbit DDR2 SDRAMs in P-TFBGA-84 and P-TFBGA-60 chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- UDIMM and EDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference layouts Raw Card “C”, “D”,”E”,”F” and “G“
- RoHS compliant products[1)]
- All speed grades faster than DDR400 comply with DDR400 timing specifications.

A list of the performance tables for the various speeds can be found below

- **Table 1 “Performance for DDR2–800” on Page 6**
- **Table 2 “Performance for DDR2–667” on Page 6**
- **Table 3 “Performance for DDR2–533C” on Page 6**
- **Table 4 “Performance for DDR2–400B” on Page 7**

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 1 Performance for DDR2–800

Product Type Speed Code			–2.5F	–2.5	Unit
Speed Grade			**DDR2–800D 5–5–5**	**DDR2–800E 6–6–6**	**—**
max. Clock Frequency	@CL6	f_{CK6}	400	400	MHz
	@CL5	f_{CK5}	400	333	MHz
	@CL4	f_{CK4}	266	266	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	12.5	15	ns
min. Row Precharge Time		t_{RP}	12.5	15	ns
min. Row Active Time		t_{RAS}	45	45	ns
min. Row Cycle Time		t_{RC}	57.5	60	ns

Table 2 Performance for DDR2–667

Product Type Speed Code			–3	–3S	Unit
Speed Grade			**DDR2–667C 4–4–4**	**DDR2–667D 5–5–5**	**—**
max. Clock Frequency	@CL5	f_{CK5}	333	333	MHz
	@CL4	f_{CK4}	333	266	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	12	15	ns
min. Row Precharge Time		t_{RP}	12	15	ns
min. Row Active Time		t_{RAS}	45	45	ns
min. Row Cycle Time		t_{RC}	57	60	ns

Table 3 Performance for DDR2–533C

Product Type Speed Code			–3.7	Unit
Speed Grade			**DDR2–533C 4–4–4**	**—**
max. Clock Frequency	@CL5	f_{CK5}	266	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	45	ns
min. Row Cycle Time		t_{RC}	60	ns

Table 4 Performance for DDR2–400B

Product Type Speed Code			–5	Units
Speed Grade			**DDR2–400B 3–3–3**	**—**
max. Clock Frequency	@CL5	f_{CK5}	200	MHz
	@CL4	f_{CK4}	200	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	40	ns
min. Row Cycle Time		t_{RC}	55	ns

1.2 Description

The INFINEON HYS[64/72]T[32/64/128]xxxHU-[2.5F/…/5]-B module family are unbuffered DIMM modules “UDIMMs” with 30,0 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 32M × 64 (256 MB), 64M × 64 (512 MB) and 128M × 64(1 GB), and as ECC modules in 64M × 72 (512 MB), 128M × 72(1 GB) organization and density, intended for mounting into 240-pin connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

Table 5 Ordering Information for RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2–6400			
HYS64T32000HU–25F–B	256 MB 1R×16 PC2–6400U–555–12–C1	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–25F–B	512 MB 1R×8 PC2–6400U–555–12–D0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–25F–B	512 MB 1R×8 PC2–6400E–555–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020HU–25F–B	1 GB 2R×8 PC2–6400U–555–12–E0	2 Ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–25F–B	1 GB 2R×8 PC2–6400E–555–12–G0	2 Ranks, ECC	512 Mbit (×8)
PC2–6400			
HYS64T32000HU–2.5–B	256 MB 1R×16 PC2–6400U–666–12–C1	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–2.5–B	512 MB 1R×8 PC2–6400U–666–12–D0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–2.5–B	512 MB 1R×8 PC2–6400E–666–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020HU–2.5–B	1 GB 2R×8 PC2–6400U–666–12–E0	2 Ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–2.5–B	1 GB 2R×8 PC2–6400E–666–12–G0	2 Ranks, ECC	512 Mbit (×8)
PC2–5300			
HYS64T32000HU–3–B	256 MB 1R×16 PC2–5300U–444–12–C1	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–3–B	512 MB 1R×8 PC2–5300U–444–12–D0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–3–B	512 MB 1R×8 PC2–5300E–444–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020HU–3–B	1 GB 2R×8 PC2–5300U–444–12–E0	2 Ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–3–B	1 GB 2R×8 PC2–5300E–444–12–G0	2 Ranks, ECC	512 Mbit (×8)

Table 5 Ordering Information for RoHS Compliant Products (cont'd)

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2–5300			
HYS64T32000HU–3S–B	256 MB 1R×16 PC2–5300U–555–12–C1	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–3S–B	512 MB 1R×8 PC2–5300U–555–12–D0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–3S–B	512 MB 1R×8 PC2–5300E–555–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020HU–3S–B	1 GB 2R×8 PC2–5300U–555–12–E0	2 Ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–3S–B	1 GB 2R×8 PC2–5300E–555–12–G0	2 Ranks, ECC	512 Mbit (×8)
PC2–4200			
HYS64T32000HU–3.7–B	256 MB 1R×16 PC2–4200U–444–12–C1	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–3.7–B	512 MB 1R×8 PC2–4200U–444–12–D0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–3.7–B	512 MB 1R×8 PC2–4200E–444–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020HU–3.7–B	1 GB 2R×8 PC2–4200U–444–12–E0	2 Ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–3.7–B	1 GB 2R×8 PC2–4200E–444–12–G0	2 Ranks, ECC	512 Mbit (×8)
PC2–3200			
HYS64T32000HU–5–B	256 MB 1R×16 PC2–3200U–333–12–C1	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–5–B	512 MB 1R×8 PC2–3200U–333–12–D0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–5–B	512 MB 1R×8 PC2–3200E–333–12–F0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020HU–5–B	1 GB 2R×8 PC2–3200U–333–12–E0	2 Ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–5–B	1 GB 2R×8 PC2–3200E–333–12–G0	2 Ranks, ECC	512 Mbit (×8)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS64T16000HU–5–A, indicating Rev. "B" dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see **Chapter 6** of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2–4200U–444–11–C1", where 4200U means Unbuffered DIMM modules with 4.26 GB/sec Module Bandwidth and "444-11" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card "C".

Table 6 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
256 MByte	32M × 64	1	Non-ECC	4	13/2/10	C
512 MByte	64M × 64	1	Non-ECC	8	14/2/10	D
512 MByte	72M × 64	1	ECC	9	14/2/10	F
1 GByte	128M × 64	2	Non-ECC	16	14/2/10	E
1 GByte	128M × 72	2	ECC	18	14/2/10	G

Table 7 Components on Modules [1)]

Product Type[2)]	DRAM Components[2)]	DRAM Density	DRAM Organisation
HYS64T32000HU	HYB18T512160BF	512 Mbit	32M × 16
HYS64T64000HU	HYB18T512800BF	512 Mbit	64M × 8
HYS72T64000HU	HYB18T512800BF	512 Mbit	64M × 8
HYS64T128020HU	HYB18T512800BF	512 Mbit	64M × 8
HYS72T128020HU	HYB18T512800BF	512 Mbit	64M × 8

1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2) Green Product

2 Pin Configurations and Block Diagrams

2.1 Pin Configuration

The pin configuration of the Unbuffered DDR2 SDRAM DIMM is listed by function in **Table 8** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 9** and **Table 10** respectively. The pin numbering is depicted in **Figure 1** for non-ECC modules (×64) and **Figure 2** for ECC modules (×72).

Table 8 Pin Configuration of UDIMM

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signals 2:0, Complement Clock Signals 2:0** The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
137	CK1	I	SSTL	
220	CK2	I	SSTL	
186	CK0	I	SSTL	
138	CK1	I	SSTL	
221	CK2	I	SSTL	
52	CKE0	I	SSTL	**Clock Enable Rank 1:0** Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode. *Note: 2 Ranks module*
171	CKE1	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1 Rank module*
Control Signals				
193	S0	I	SSTL	**Chip Select Rank 1:0** Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. Ranks are also called "Physical banks". *Note: 2 Ranks module*
76	S1	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1 Rank module*
192	RAS	I	SSTL	**Row Address Strobe** When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
74	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
73	$\overline{WE}$	I	SSTL	**Write Enable**

Table 8 Pin Configuration of UDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0** Selects which DDR2 SDRAM internal bank of four or eight is activated.
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	NC	—	**Not Connected** Less than 1Gb DDR2 SDRAMS
188	A0	I	SSTL	**Address Bus 12:0** During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge.
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module and 512M ×4/×8*
	NC	NC	—	**Not Connected** *Note: Module based on 1 Gbit ×16* *Note: Module based on 512 Mbit ×16 or smaller*
174	A14	I	SSTL	**Address Signal 14** *Note: Modules based on 2 Gbit*
	NC	NC	—	**Not Connected** *Note: Modules based on 1 Gbit or smaller*
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	

Table 8 Pin Configuration of UDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
12	DQ8	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	

Table 8 Pin Configuration of UDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
98	DQ48	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bit Signals				
42	CB0	I/O	SSTL	**Check Bit 0** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*
43	CB1	I/O	SSTL	**Check Bit 1** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*
48	CB2	I/O	SSTL	**Check Bit 2** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*
49	CB3	I/O	SSTL	**Check Bit 3** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*
161	CB4	I/O	SSTL	**Check Bit 4** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*

Table 8 Pin Configuration of UDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
162	CB5	I/O	SSTL	**Check Bit 5** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*
167	CB6	I/O	SSTL	**Check Bit 6** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: ECC type module only*
168	CB7	I/O	SSTL	**Check Bit 7** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC module*
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobe Bus 8:0** The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} and DDR2 SDRAM mode registers programmed appropriately. *Note: See block diagram for corresponding DQ signals*
16	DQS1	I/O	SSTL	
28	DQS2	I/O	SSTL	
37	DQS3	I/O	SSTL	
84	DQS4	I/O	SSTL	
93	DQS5	I/O	SSTL	
105	DQS6	I/O	SSTL	
114	DQS7	I/O	SSTL	
46	DQS8	I/O	SSTL	
6	$\overline{\text{DQS0}}$	I/O	SSTL	**Complement Data Strobe Bus 8:0** *Note: See block diagram for corresponding DQ signals*
15	$\overline{\text{DQS1}}$	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	

Table 8 Pin Configuration of UDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Mask Signals				
125	DM0	I	SSTL	**Data Mask Bus 8:0** The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect. *Note: See block diagram for corresponding DQ M signals*
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock** This signal is used to clock data into and out of the SPD EEPROM.
119	SDA	I/O	OD	**Serial Bus Data** This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.
239	SA0	I	CMOS	**Serial Address Select Bus 2:0** Address pins used to select the Serial Presence Detect base address.
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage** Reference voltage for the SSTL-18 inputs.
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply** Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
51,56,62,72,75,,78,170,175,181,,191,194	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
53,59,64,67,69,,172,178,184,187,189,197	V_{DD}	PWR	—	**Power Supply** Power supplies for core, I/O, Serial Presence Detect, and ground for the module.

Table 8 Pin Configuration of UDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2,5,8,11,14,17,, 20,23,26,29,32, 35,38,41,44,47,, 50,65,66,79,82, 85,88,91,94,97,, 100,103,106, 109,112,115,118 ,121,124,127,, 130,133,136,139 ,142,145,148,, 151,154,157,160 ,163,166,169, 198,201,204,207 ,210,213,216,, 219,222,225,228 ,231,234,237	V_{SS}	GND	—	**Ground Plane** Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
Other Pins				
195	ODT0	I	SSTL	**On-Die Termination Control 0**
77	ODT1	I	SSTL	**On-Die Termination Control 1** Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. *Note: 2 Rank modules*
	NC	NC	—	**Not Connected** *Note: 1 Rank modules*
18,19,55,68,102, 126,135,147, 156,165,173,203 ,212, 224,233	NC	NC	—	**Not connected** *Note: Pins not connected on Infineon UDIMMs*

Table 9 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 10 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.

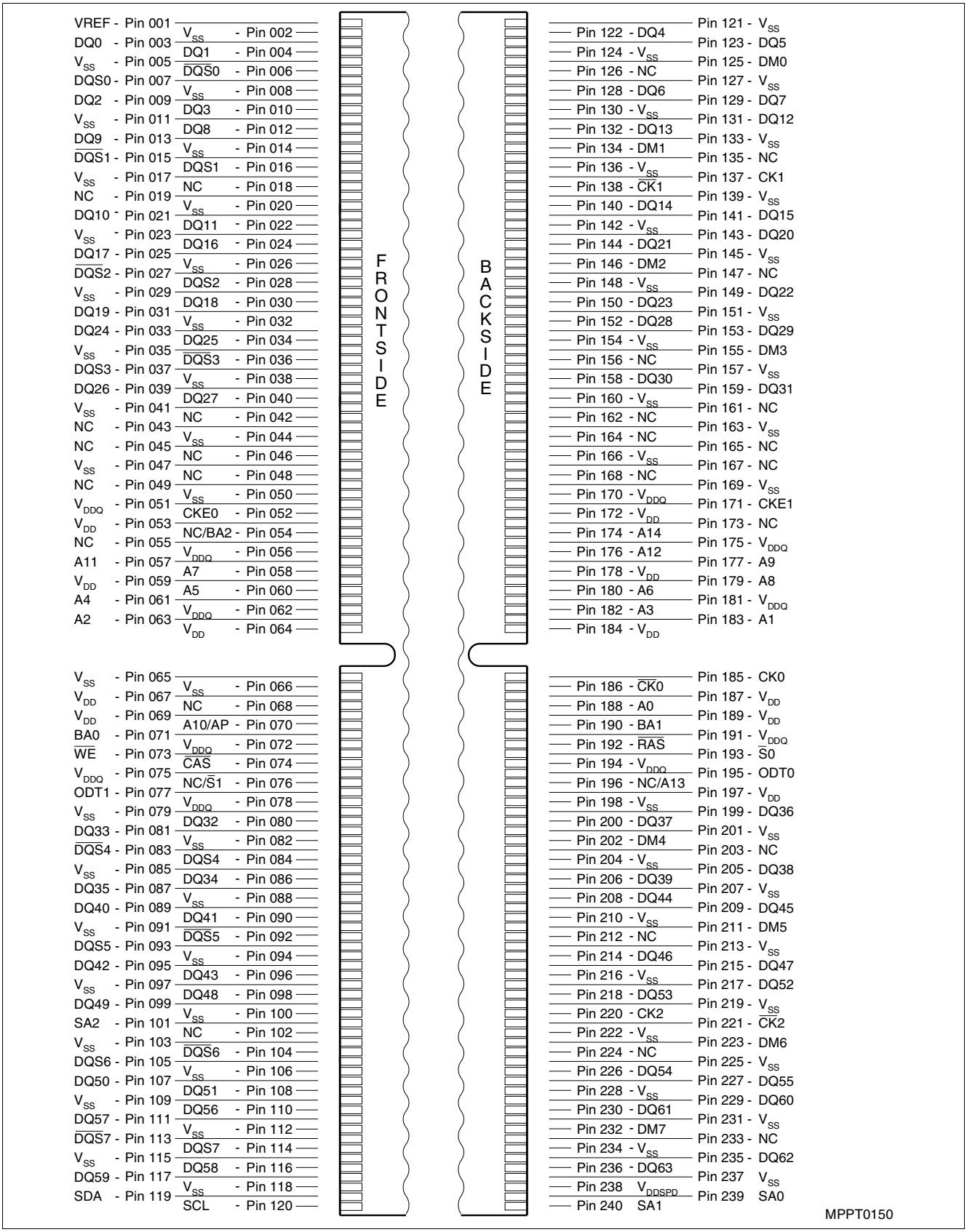

Figure 1 Pin Configuration UDIMM ×64 (240 Pin)

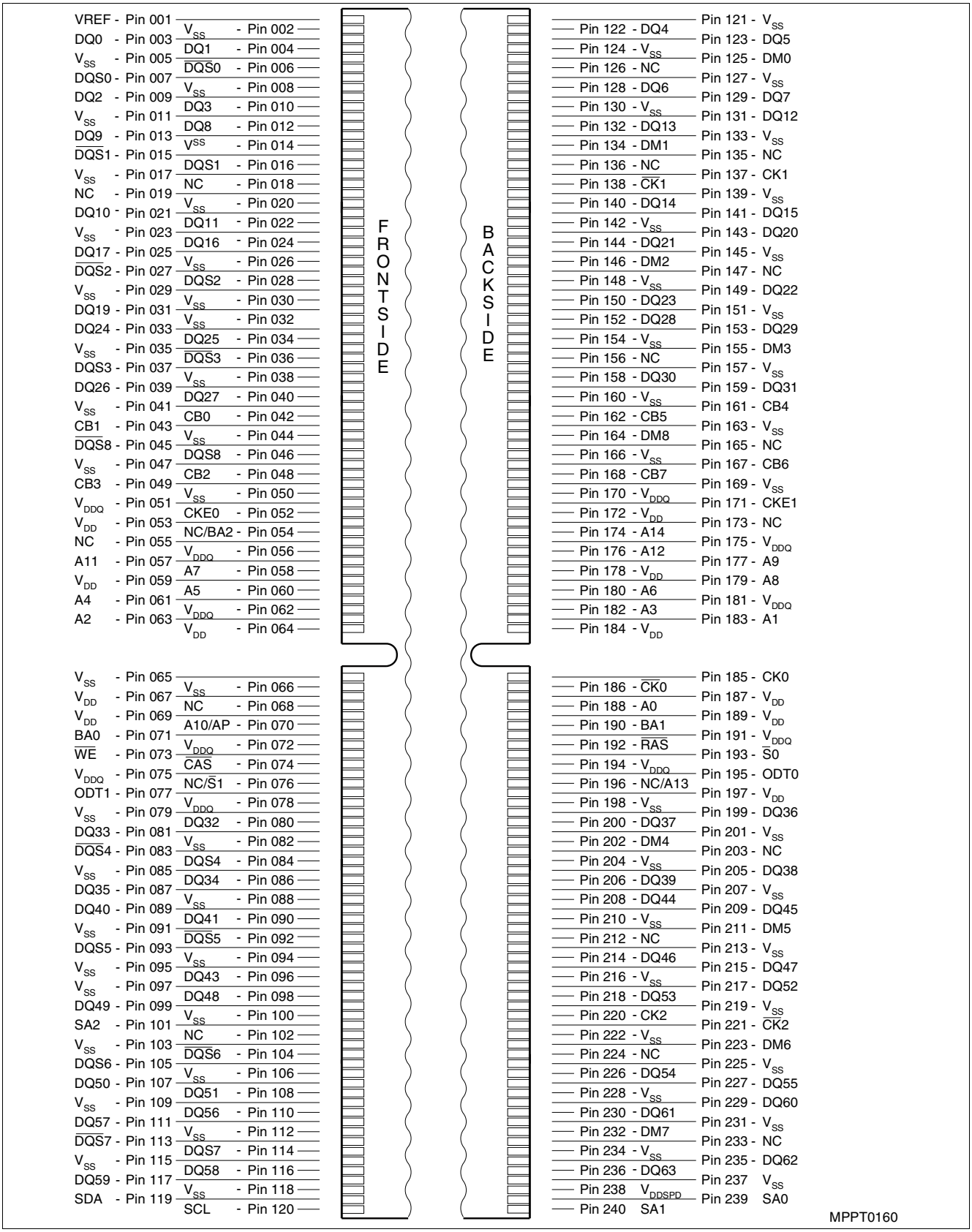

Figure 2 Pin Configuration UDIMM ×72 (240 Pin)

2.2 Block Diagrams

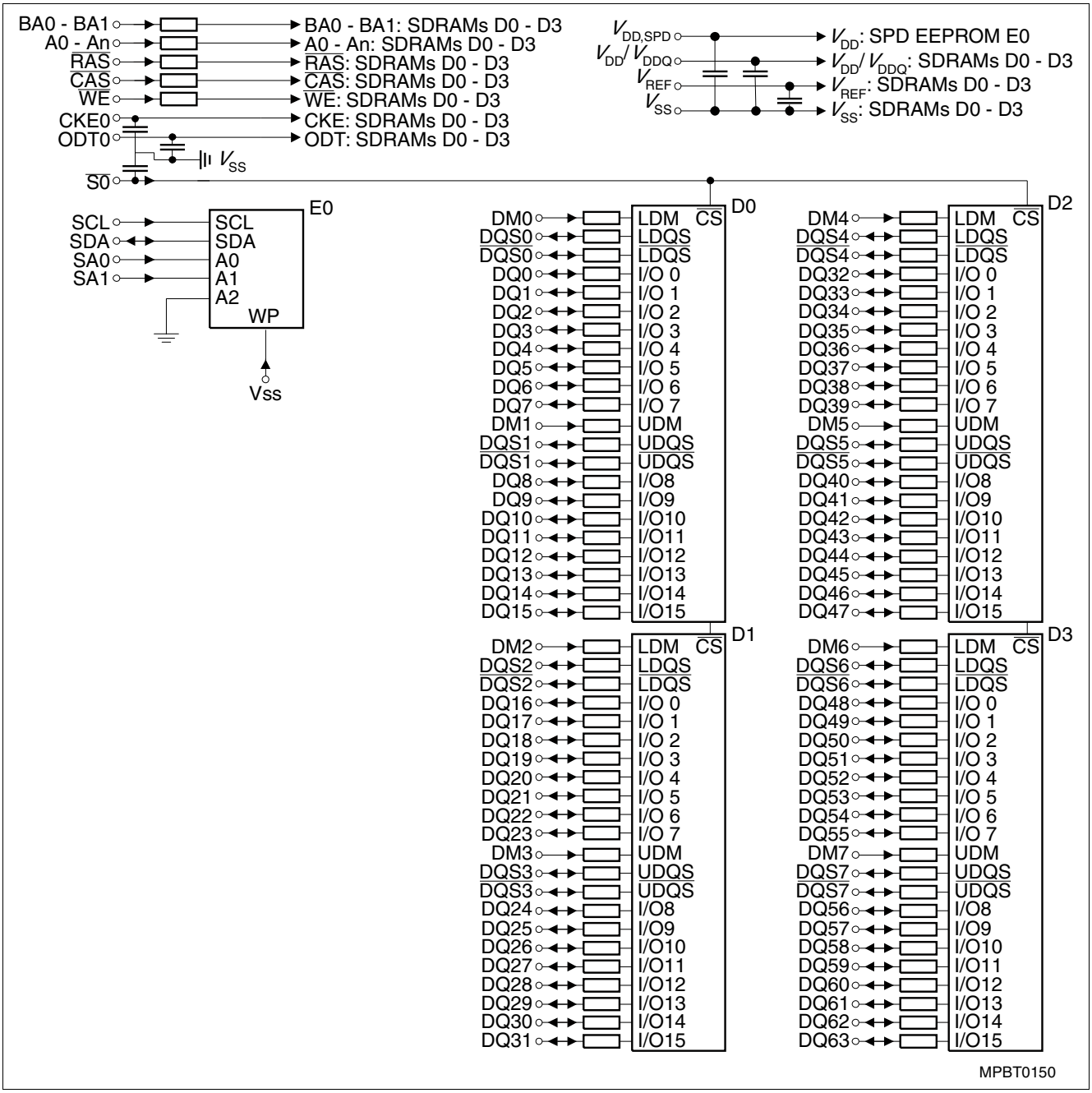

Figure 3 Block Diagram Raw Card C UDIMM (x64, 1 Rank, x16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ± 5 %*
2. *BAn, An, RAS, CAS, WE resistors are 10 Ω ± 5 %*

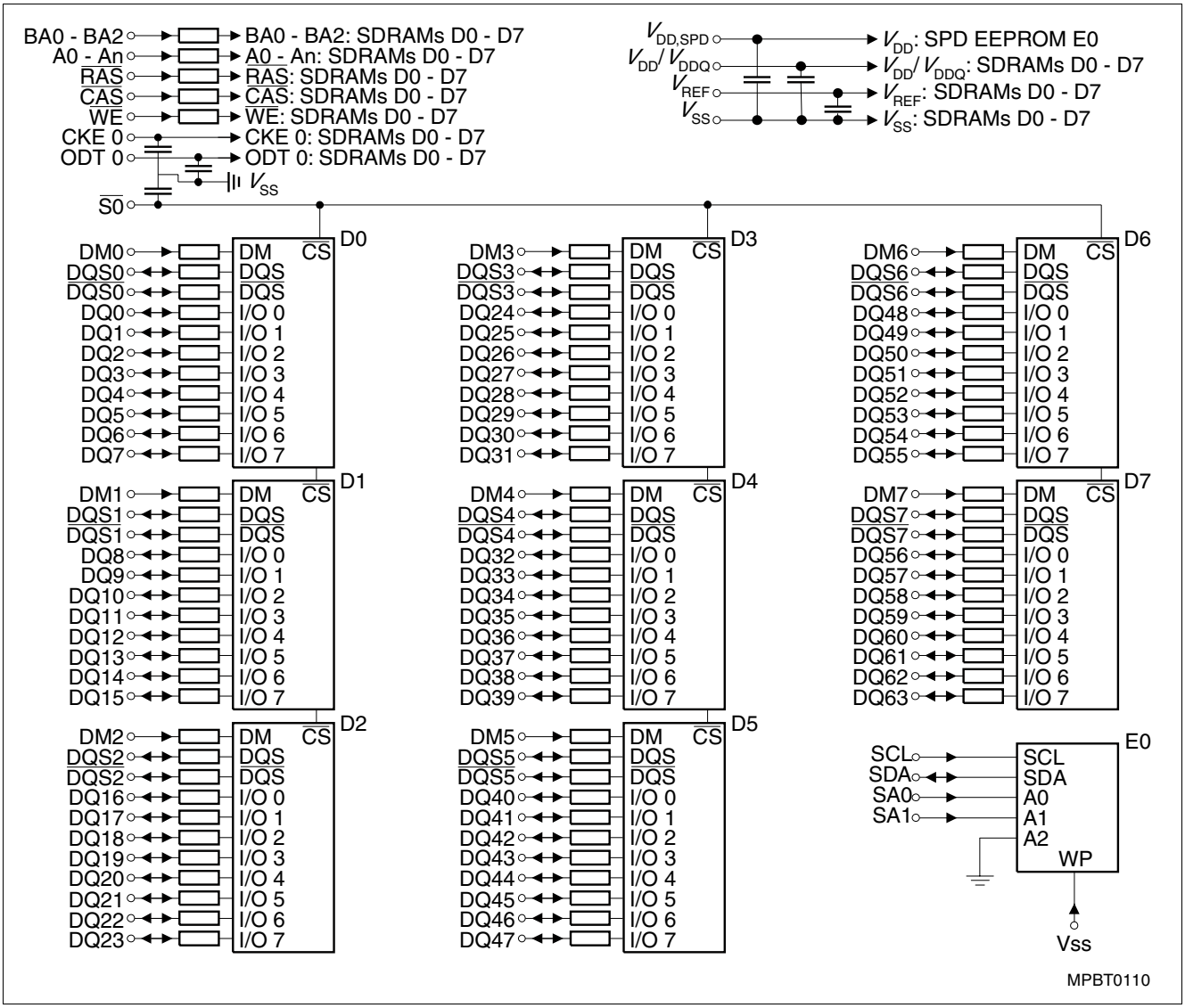

Figure 4 Block Diagram Raw Card D UDIMM (×64, 1 Rank, ×8)

Notes

1. *DQ,DQS,$\overline{DQS}$,DM,CB resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All CK lines have resistor termination between CK an $\overline{CK}$.*

Table 11 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	4	
CK1,$\overline{CK1}$	6	
CK2,$\overline{CK2}$	6	

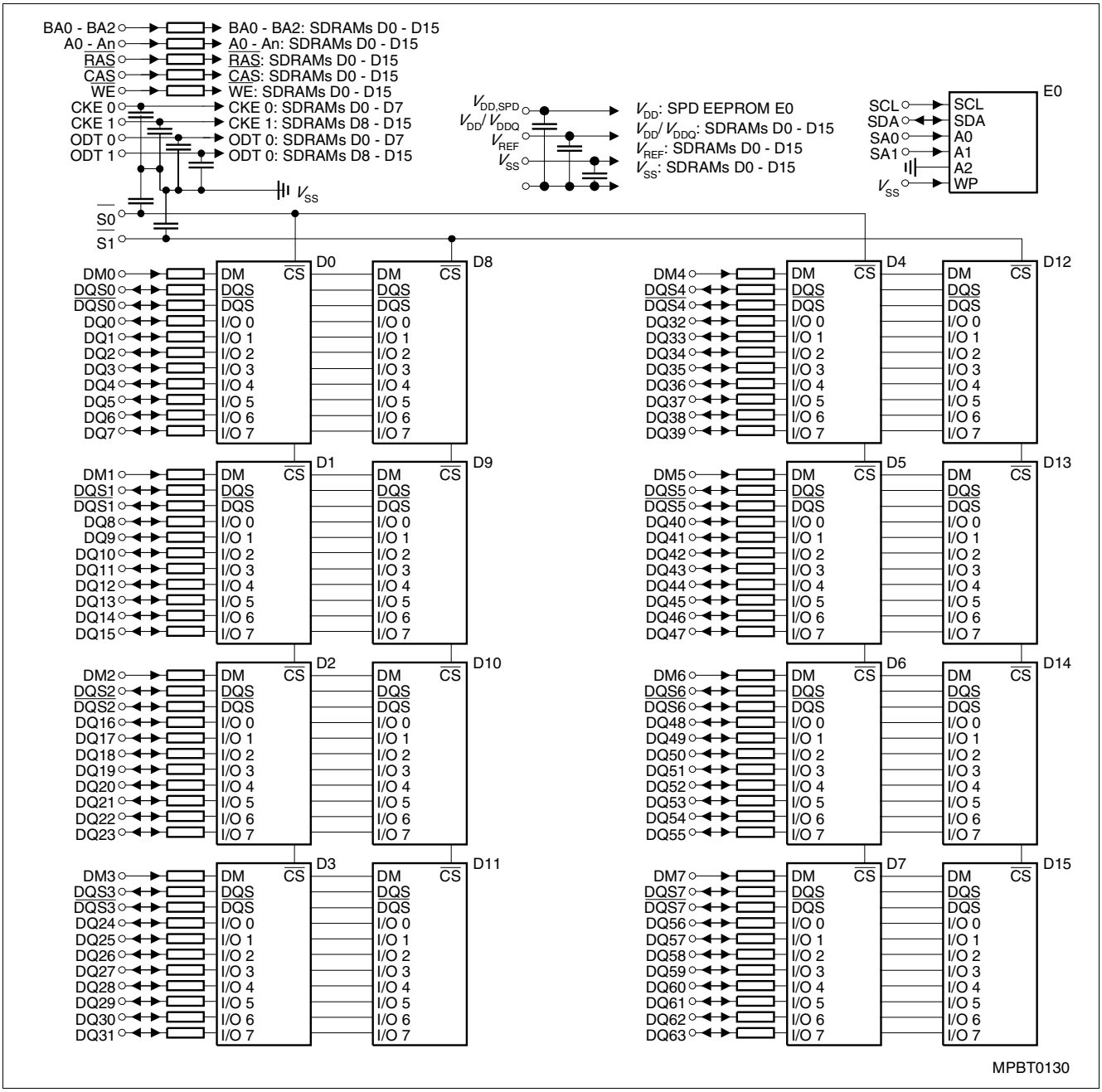

Figure 5 Block Diagram Raw Card E UDIMM (×64, 2 Ranks, ×8)

Notes

1. *DQ,DQS,$\overline{DQS}$,DM,CB resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All CK lines have resistor termination between CK an $\overline{CK}$.*

Table 12 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	2	
CK1,$\overline{CK1}$	3	
CK2,$\overline{CK2}$	3	

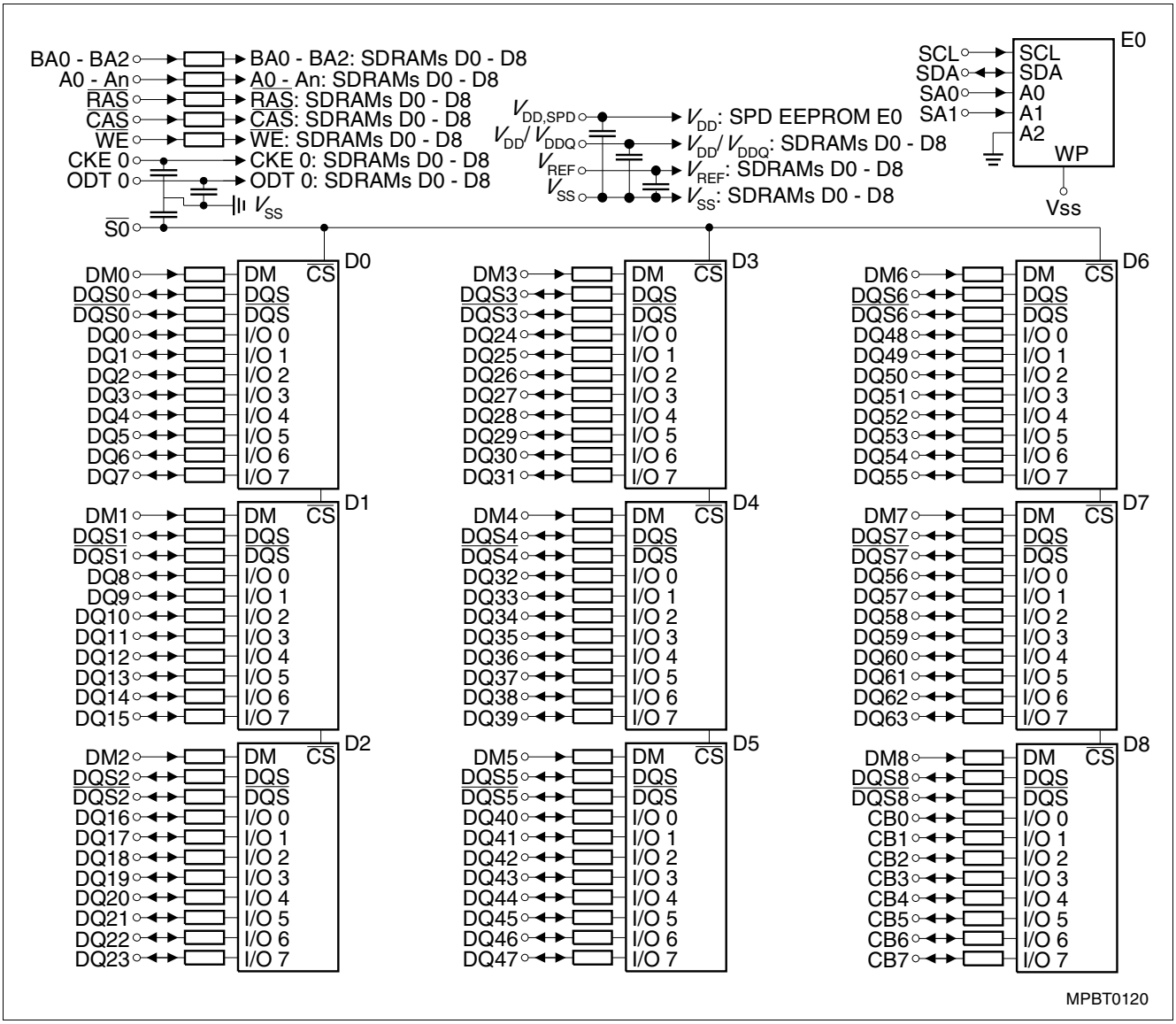

Figure 6 Block Diagram Raw Card F UDIMM (×72, 1 Rank, ×8)

Notes

1. *DQ,DQS,$\overline{DQS}$,DM resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All CK lines have resistor termination between CK an $\overline{CK}$.*

Table 13 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	2	
CK1,$\overline{CK1}$	3	
CK2,$\overline{CK2}$	3	

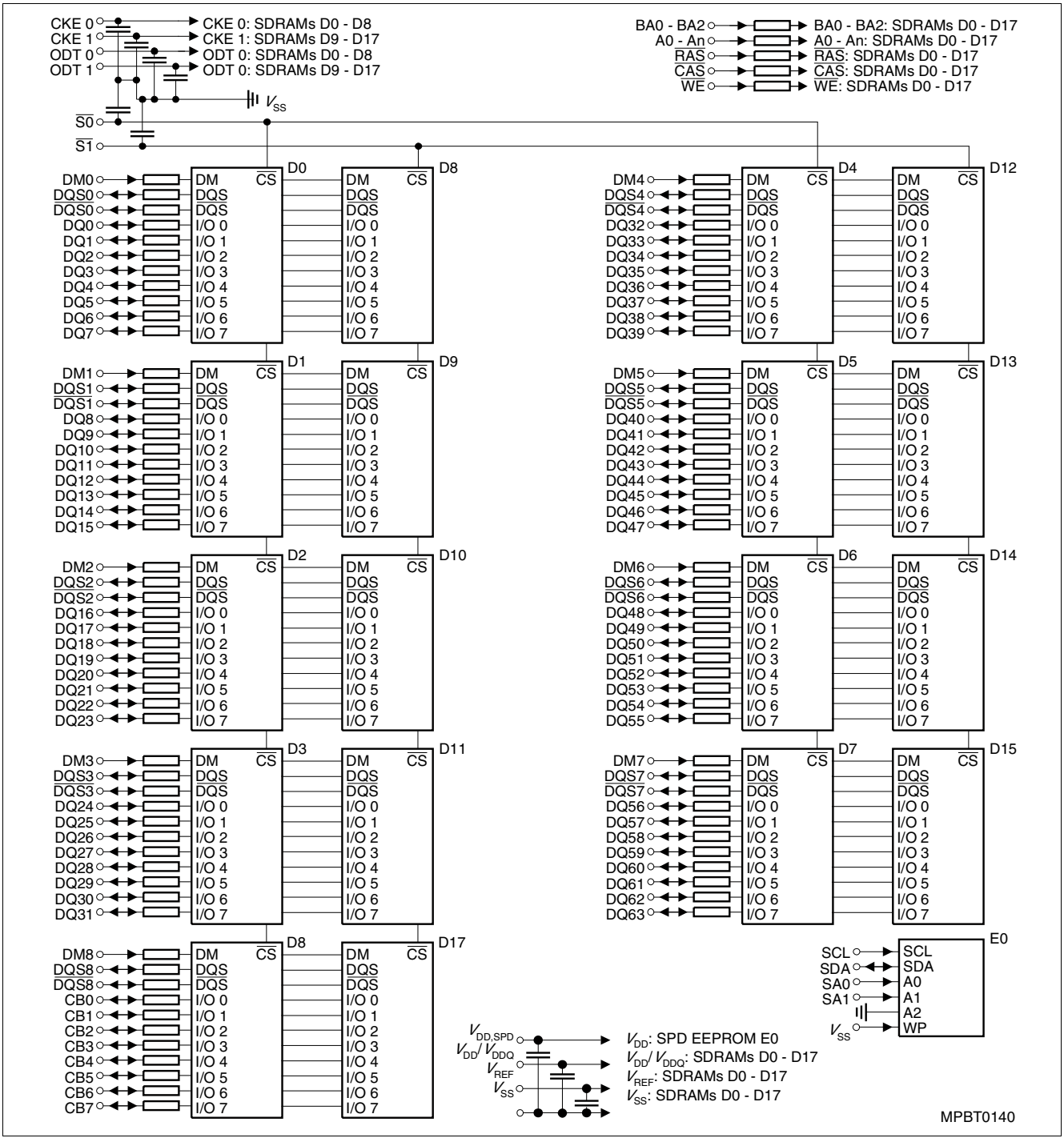

Figure 7 Block Diagram Raw Card G UDIMM (×72, 2 Ranks, ×8)

Notes

1. DQ,DQS,$\overline{DQS}$,DM resistors are 22 Ω ± 5 %
2. BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ± 5 %
3. ODT,CKE,$\overline{S}$ capacitors are 24 pF
4. All CK lines have resistor termination between CK an $\overline{CK}$.

Table 14 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	2	
CK1,$\overline{CK1}$	3	
CK2,$\overline{CK2}$	3	

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 15 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V	
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V	
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	– 0.5	2.3	V	
Storage Humidity (without condensation)	H_{STG}	5	95	%	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values maycause irreversible damage to the integrated circuit.

3.2 DC Operating Conditions

Table 16 Operating Conditions

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	×C	
DRAM Case Temperature	T_{CASE}	0	+95	×C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	×C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs
4) For Self Refresh Operation above 85 °C it is necessary to set extended mode register 2 (EMR(2)) Bit A7 to "1" to enable the High Temperature Self Refresh option.
5) Up to 3000 m.

Table 17 Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1)
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	4)

1) V_{DDQ} tracks with V_{DD}, V_{DDDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDDL} tied together.
2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
3) Peak to peak ac noise on V_{REF} may not exceed ± 2% V_{REF} (dc)
4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}.

3.3 AC Characteristics

3.3.1 Speed Grade Definitions

All Speed grades faster than DDR2-DDR400B comply with DDR2-DDR400B timing specifications(t_{CK} = 5ns with t_{RAS} = 40ns).

List of Speed Grade Definition tables:

- **Table 18 “Speed Grade Definition Speed Bins DDR2–800” on Page 26**
- **Table 19 “Speed Grade Definition Speed Bins for DDR2–667” on Page 27**
- **Table 20 “Speed Grade Definition Speed Bins for DDR2–533C” on Page 27**
- **Table 21 “Speed Grade Definition Speed Bins for DDR2–400B” on Page 28**

Table 18 Speed Grade Definition Speed Bins DDR2–800

Speed Grade			DDR2–800D		DDR2–800E		Unit	Note
IFX Sort Name			–2.5F		–2.5			
CAS-RCD-RP latencies			5–5–5		6–6–6		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 19 Speed Grade Definition Speed Bins for DDR2–667

Speed Grade			DDR2–667C		DDR2–667D		Unit	Notes
IFX Sort Name			–3		–3S			
CAS-RCD-RP latencies			4–4–4		5–5–5		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 20 Speed Grade Definition Speed Bins for DDR2–533C

Speed Grade			DDR2–533C		Unit	Note
IFX Sort Name			–3.7			
CAS-RCD-RP latencies			4–4–4		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 21 Speed Grade Definition Speed Bins for DDR2–400B

Speed Grade			DDR2–400B		Unit	Note
IFX Sort Name			–5			
CAS-RCD-RP latencies			3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 AC Timing Parameters

List of Timing Parameters for DDR2-800, DDR2-667(**Table 22**), and DDR2-533, DDR2-400(**Table 23**)

Table 22 Timing Parameter by Speed Grade - DDR2–800

Parameter	Symbol	DDR2–800		Unit	Notes[1)2)3)4)5) 6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–400	+400	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	125	—	ps	

Table 22 Timing Parameter by Speed Grade - DDR2–800 (cont'd)

Parameter	Symbol	DDR2–800		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	—	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–350	+350	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	200	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	50	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	—	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	250	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	175	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	t_{HP}–t_{QHS}	—		
Data hold skew factor	t_{QHS}	—	300	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	
		—	3.9	µs	
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	9)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.35 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	

Table 22 Timing Parameter by Speed Grade - DDR2–800 (cont'd)

Parameter	Symbol	DDR2–800		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	8)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1 V. See notes 5)6)7)1)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8.2 of this data sheet. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the Reference Load for Timing Measurements in Chapter 8.1 only.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/$\overline{CK}$, DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in Chapter 8.3.4 of this data sheet.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}. See Chapter 8.1 for the reference load for timing measurements.
8) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

Table 23 Timing Parameter by Speed Grade - DDR2–667

Parameter	Symbol	DDR2–667		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	175	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	—	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	240	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	—	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	275	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	200	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	t_{HPQ} – t_{QHS}	—		
Data hold skew factor	t_{QHS}	—	340	ps	

Table 23 Timing Parameter by Speed Grade - DDR2–667 (cont'd)

Parameter	Symbol	DDR2–667		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	
		—	3.9	µs	
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	28)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.35 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	8)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet

2) V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1 V. See notes 5)6)7)20)

3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8.2 of this data sheet. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the Reference Load for Timing Measurements in Chapter 8.1 only.

5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode;
The input reference level for signals other than CK/$\overline{CK}$, DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in Chapter 8.3.4 of this data sheet.

6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

7) The output timing reference voltage level is V_{TT}. See Chapter 8.1 for the reference load for timing measurements.

8) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

Table 24 Timing Parameter by Speed Grade - DDR2-533

Parameter	Symbol	DDR2–533		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	375	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—		

Table 24 Timing Parameter by Speed Grade - DDR2-533 (cont'd)

Parameter	Symbol	DDR2–533		Unit	Notes[1)2)3)4) 5)6)7)]
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	400	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	
		—	3.9	µs	
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	47)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	8)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1 V. See notes 5)6)7)39)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8.2 of this data sheet. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the Reference Load for Timing Measurements according to Chapter 8.1 only.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode;
The input reference level for signals other than CK/$\overline{CK}$, DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in Chapter 8.3.4 of this data sheet.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}. See Chapter 8.1 for the reference load for timing measurements.

8) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

Table 25 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	150	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	350	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		

Table 25 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Notes[1)2)3)4) 5)6)7)]
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	
		—	3.9	µs	
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	66)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	8)
Internal Write to Read command delay	t_{WTR}	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1 V. See notes [5)6)7)20)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8.2 of this data sheet. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the Reference Load for Timing Measurements according to Chapter 8.1 only.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode;
The input reference level for signals other than CK/$\overline{CK}$, DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in Chapter 8.3.4 of this data sheet.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}. See Chapter 8.1 for the reference load for timing measurements.

8) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

3.3.3 ODT AC Electrical Characteristics

List of ODT tables.

Table 26 ODT AC Characteristics and Operating Conditions for DDR2-667 and DDR2-800

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

Table 27 ODT AC Characteristics and Operating Conditions for DDR2-533 and DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

3.4 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

Table 28 I_{DD} Measurement Conditions [1)2)3)4)5)6)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; t_{CK} = $t_{CK.MIN}$, t_{RC} = $t_{RC.MIN}$, t_{RAS} = $t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, t_{CK} = $t_{CK.MIN}$, t_{RC} = $t_{RC.MIN}$, t_{RAS} = $t_{RAS.MIN}$, t_{RCD} = $t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t_{CK} = $t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t_{CK} = $t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; t_{CK} = $t_{CK.MIN}$; t_{RAS} = $t_{RAS.MAX}$, t_{RP} = $t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Active Power-Down Current All banks open; t_{CK} = $t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; t_{CK} = $t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Operating Current urst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; t_{CK} = $t_{CK.MIN}$; t_{RAS} = $t_{RAS.MAX.}$, t_{RP} = $t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current t_{CK} = $t_{CK.MIN.}$, Refresh command every t_{RFC} = $t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current t_{CK} = $t_{CK.MIN.}$, Refresh command every t_{RFC} = t_{REFI} interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 28 I_{DD} Measurement Conditions (cont'd)[1)2)3)4)5)6)]

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 29**
4) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
6) For details and notes see the relevant INFINEON component data sheet

Table 29 Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are V_{REF} = V_{DDQ}/2
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

Table 30 I_{DD} Specification for HYS[64/72]T[32/64/128]xxxHU-2.5F-B

Product Type	HYS64T32000HU–2.5F–B	HYS64T64000HU–2.5F–B	HYS72T64000HU–2.5F–B	HYS64T128020HU–2.5F–B	HYS72T128020HU–2.5F–B	Unit	Note[1)]
Organization	**256MB**	**512MB**	**512MB**	**1GB**	**1GB**		
	1 Rank	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
	×64	**×64**	**×72**	**×64**	**×72**		
	-2.5F	**-2.5F**	**-2.5F**	**-2.5F**	**-2.5F**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	420	670	760	730	820	mA	2)
I_{DD1}	480	800	900	860	960	mA	2)
I_{DD2P}	30	60	60	110	130	mA	3)
I_{DD2N}	200	410	460	820	920	mA	3)
I_{DD2Q}	180	360	410	720	810	mA	3)
$I_{DD3P(MRS=0)}$	160	310	350	620	700	mA	3)
$I_{DD3P(MRS=1)}$	40	70	80	140	160	mA	3)
I_{DD3N}	240	480	540	960	1080	mA	3)
I_{DD4R}	720	1240	1400	1300	1460	mA	2)
I_{DD4W}	800	1240	1400	1300	1460	mA	2)
I_{DD5B}	580	1160	1310	1220	1370	mA	2)
I_{DD5D}	40	70	80	140	160	mA	3)4)
I_{DD6}	28	56	63	112	126	mA	3)4)
I_{DD7}	1060	1360	1530	1420	1590	mA	2)

1) Calculated values from component data. ODT disabled. $I_{DD1,}$ $I_{DD4R,}$ and $I_{DD7,}$ are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD}current mode

4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C.

Table 31 I_{DD} Specification for HYS[64/72]T[32/64/128]xxxHU-2.5-B

Product Type	HYS64T32000HU–2.5–B	HYS64T64000HU–2.5–B	HYS72T64000HU–2.5–B	HYS64T128020HU–2.5–B	HYS72T128020HU–2.5–B	Unit	Note[1)]
Organization	**256MB**	**512MB**	**512MB**	**1GB**	**1GB**		
	1 Rank	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
	×64	**×64**	**×72**	**×64**	**×72**		
	-2.5	**-2.5**	**-2.5**	**-2.5**	**-2.5**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	400	640	720	700	780	mA	2)
I_{DD1}	460	760	860	820	920	mA	2)
I_{DD2P}	30	60	60	110	130	mA	3)
I_{DD2N}	200	410	460	820	920	mA	3)
I_{DD2Q}	180	360	410	720	810	mA	3)
$I_{DD3P(MRS=0)}$	160	310	350	620	700	mA	3)
$I_{DD3P(MRS=1)}$	40	70	80	140	160	mA	3)
I_{DD3N}	240	480	540	960	1080	mA	3)
I_{DD4R}	720	1240	1400	1300	1460	mA	2)
I_{DD4W}	800	1240	1400	1300	1460	mA	2)
I_{DD5B}	580	1160	1310	1220	1370	mA	2)
I_{DD5D}	40	70	80	140	160	mA	3)4)
I_{DD6}	28	56	63	112	126	mA	3)4)
I_{DD7}	1020	1280	1440	1340	1500	mA	2)

1) Calculated values from component data. ODT disabled. $I_{DD1,}$ $I_{DD4R,}$ and $I_{DD7,}$ are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD} current mode

4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C

Table 32 I_{DD} Specification for HYS[64/72]T[32/64/128]xxxHU-3-B

Product Type	HYS64T32000HU–3–B	HYS64T64000HU–3–B	HYS72T64000HU–3–B	HYS64T128020HU–3–B	HYS72T128020HU–3–B	Unit	Note[1)]
Organization	256MB	512MB	512MB	1GB	1GB		
	1 Rank	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×64	×64	×72	×64	×72		
	-3	-3	-3	-3	-3		
Symbol	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	380	600	680	660	740	mA	2)
I_{DD1}	420	720	810	780	870	mA	2)
I_{DD2P}	30	60	60	110	130	mA	3)
I_{DD2N}	180	360	410	720	810	mA	3)
I_{DD2Q}	160	320	360	640	720	mA	3)
$I_{DD3P(MRS=0)}$	130	260	300	530	590	mA	3)
$I_{DD3P(MRS=1)}$	40	70	80	140	160	mA	3)
I_{DD3N}	200	400	450	800	900	mA	3)
I_{DD4R}	620	1040	1170	1100	1230	mA	2)
I_{DD4W}	680	1040	1170	1100	1230	mA	2)
I_{DD5B}	560	1120	1260	1180	1320	mA	2)
I_{DD5D}	40	70	80	140	160	mA	3)4)
I_{DD6}	28	56	63	112	126	mA	3)4)
I_{DD7}	1010	1280	1440	1340	1500	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD}current mode

4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C.

Table 33 I_{DD} Specification for HYS[64/72]T[32/64/128]xxxHU-3S-B

Product Type	HYS64T32000HU–3S–B	HYS64T64000HU–3S–B	HYS72T64000HU–3S–B	HYS64T128020HU–3S–B	HYS72T128020HU–3S–B	Unit	Note[1)]
Organization	**256MB**	**512MB**	**512MB**	**1GB**	**1GB**		
	1 Rank	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
	×64	**×64**	**×72**	**×64**	**×72**		
	-3S	**-3S**	**-3S**	**-3S**	**-3S**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	360	570	640	620	700	mA	2)
I_{DD1}	400	680	770	740	830	mA	2)
I_{DD2P}	30	60	60	110	130	mA	3)
I_{DD2N}	180	360	410	720	810	mA	3)
I_{DD2Q}	160	320	360	640	720	mA	3)
$I_{DD3P(MRS=0)}$	130	260	300	530	590	mA	3)
$I_{DD3P(MRS=1)}$	40	70	80	140	160	mA	3)
I_{DD3N}	200	400	450	800	900	mA	3)
I_{DD4R}	620	1040	1170	1100	1230	mA	2)
I_{DD4W}	680	1040	1170	1100	1230	mA	2)
I_{DD5B}	560	1120	1260	1180	1320	mA	2)
I_{DD5D}	40	70	80	140	160	mA	3)4)
I_{DD6}	28	56	63	112	126	mA	3)4)
I_{DD7}	960	1220	1370	1270	1430	mA	2)

1) Calculated values from component data. ODT disabled. $I_{DD1,}$ $I_{DD4R,}$ and $I_{DD7,}$ are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD}current mode

4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C.

Table 34 I_{DD} Specification for HYS[64/72]T[32/64/128]xxxHU-3.7-B

Product Type	HYS64T32000HU–3.7–B	HYS64T64000HU–3.7–B	HYS72T64000HU–3.7–B	HYS64T128020HU–3.7–B	HYS72T128020HU–3.7–B	Unit	Note[1)]
Organization	**256MB**	**512MB**	**512MB**	**1GB**	**1GB**		
	1 Rank	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
	×64	**×64**	**×72**	**×64**	**×72**		
	-3.7	**-3.7**	**-3.7**	**-3.7**	**-3.7**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	320	520	590	580	650	mA	2)
I_{DD1}	360	600	680	660	740	mA	2)
I_{DD2P}	30	60	60	110	130	mA	3)
I_{DD2N}	150	300	340	610	680	mA	3)
I_{DD2Q}	140	280	320	560	630	mA	3)
$I_{DD3P(\ MRS\ =\ 0)}$	110	220	250	450	500	mA	3)
$I_{DD3P(\ MRS\ =\ 1)}$	40	70	80	140	160	mA	3)
I_{DD3N}	170	340	390	690	770	mA	3)
I_{DD4R}	520	880	990	940	1050	mA	2)
I_{DD4W}	580	880	990	940	1050	mA	2)
I_{DD5B}	520	1040	1170	1100	1230	mA	2)
I_{DD5D}	40	70	80	140	160	mA	3)4)
I_{DD6}	28	56	63	112	126	mA	3)4)
I_{DD7}	920	1160	1310	1220	1370	mA	2)

1) Calculated values from component data. ODT disabled. $I_{DD1,}$ $I_{DD4R,}$ and $I_{DD7,}$ are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD}current mode

4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C.

Table 35 I_{DD} Specification for HYS[64/72]T[32/647128]xxxHU-5-B

Product Type	HYS64T32000HU–5–B	HYS64T64000HU–5–B	HYS72T64000HU–5–B	HYS64T128020HU–5–B	HYS72T128020HU–5–B	Unit	Note[1)]
Organization	256MB	512MB	512MB	1GB	1GB		
	1 Rank	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×64	×64	×72	×64	×72		
	-5	-5	-5	-5	-5		
Symbol	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	300	490	550	540	610	mA	2)
I_{DD1}	330	560	630	620	690	mA	2)
I_{DD2P}	30	60	60	110	130	mA	3)
I_{DD2N}	140	270	310	540	610	mA	3)
I_{DD2Q}	130	260	290	510	580	mA	3)
$I_{DD3P(MRS=0)}$	100	190	220	380	430	mA	3)
$I_{DD3P(MRS=1)}$	40	70	80	140	160	mA	3)
I_{DD3N}	160	310	350	620	700	mA	3)
I_{DD4R}	460	760	860	820	920	mA	2)
I_{DD4W}	520	760	860	820	920	mA	2)
I_{DD5B}	500	1000	1130	1060	1190	mA	2)
I_{DD5D}	40	70	80	140	160	mA	3)4)
I_{DD6}	28	56	63	112	126	mA	3)4)
I_{DD7}	880	1130	1270	1180	1330	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.

2) I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD}current mode

4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C

3.4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the timing parameters as shown in the tables below are used.

- Table 36 “IDD Measurement Test Condition for DDR2–800” on Page 48
- Table 37 “IDD Measurement Test Condition for DDR2–667C” on Page 48
- Table 38 “IDD Measurement Test Condition for DDR2–667D” on Page 49
- Table 39 “IDD Measurement Test Condition for DDR2–533C” on Page 49
- Table 40 “IDD Measurement Test Condition for DDR2–400B” on Page 50

Table 36 I_{DD} Measurement Test Condition for DDR2–800

Parameter		Symbol	–2.5F	–2.5	Unit	Notes
			DDR2–800D	DDR2–800E		
CAS Latency		CL_{IDD}	5	6	t_{CK}	
Clock Cycle Time		$t_{CK.IDD}$	2.5	2.5	ns	
Active to Read or Write delay		$t_{RCD.IDD}$	12.5	15	ns	
Active to Active / Auto-Refresh command period		$t_{RC.IDD}$	57.5	60	ns	
Active bank A to Active bank B command delay		$t_{RRD.IDD}$	7.5	7.5	ns	1)
			10	10	ns	2)
Active to Precharge Command		$t_{RAS.MIN.IDD}$	45	45	ns	
		$t_{RAS.MAX.IDD}$	70000	70000	ns	
Precharge Command Period		$t_{RP.IDD}$	12.5	15	ns	
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC.IDD}$	105	105	ns	
Average periodic Refresh interval	0°C ≤ T_{CASE} ≤ 85°C	t_{REFI}	7.8	7.8	µs	
	85°C ≤ T_{CASE} ≤ 95°C	t_{REFI}	3.9	3.9	µs	

1) ×4 & ×8 (1 KByte page size)
2) ×16 (2 KByte page size)

Table 37 I_{DD} Measurement Test Condition for DDR2–667C

Parameter		Symbol	–3	Unit	Notes
			DDR2–667C		
CAS Latency		CL_{IDD}	4	t_{CK}	
Clock Cycle Time		$t_{CK.IDD}$	3	ns	
Active to Read or Write delay		$t_{RCD.IDD}$	12	ns	
Active to Active / Auto-Refresh command period		$t_{RC.IDD}$	57	ns	
Active bank A to Active bank B command delay		$t_{RRD.IDD}$	7.5	ns	1)
			10	ns	2)
Active to Precharge Command		$t_{RAS.MIN.IDD}$	45	ns	
		$t_{RAS.MAX.IDD}$	70000	ns	
Precharge Command Period		$t_{RP.IDD}$	12	ns	
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC.IDD}$	105	ns	
Average periodic Refresh interval	0°C ≤ T_{CASE} ≤ 85°C	t_{REFI}	7.8	µs	
	85°C ≤ T_{CASE} ≤ 95°C	t_{REFI}	3.9	µs	

1) ×4 & ×8 (1 kB page size)
2) ×16 (2 kB page size)

Table 38 I_{DD} Measurement Test Condition for DDR2–667D

Parameter		Symbol	–3S	Unit	Notes
			DDR2–667D		
CAS Latency		CL_{IDD}	5	t_{CK}	
Clock Cycle Time		$t_{CK.IDD}$	3	ns	
Active to Read or Write delay		$t_{RCD.IDD}$	15	ns	
Active to Active / Auto-Refresh command period		$t_{RC.IDD}$	60	ns	
Active bank A to Active bank B command delay		$t_{RRD.IDD}$	7.5	ns	1)
			10	ns	2)
Active to Precharge Command		$t_{RAS.MIN.IDD}$	45	ns	
		$t_{RAS.MAX.IDD}$	70000	ns	
Precharge Command Period		$t_{RP.IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC.IDD}$	105	ns	
Average periodic Refresh interval	0°C ≤ T_{CASE} ≤ 85°C	t_{REFI}	7.8	µs	
	85°C ≤ T_{CASE} ≤ 95°C	t_{REFI}	3.9	µs	

1) ×4 & ×8 (1 kB page size)
2) ×16 (2 kB page size)

Table 39 I_{DD} Measurement Test Condition for DDR2–533C

Parameter		Symbol	–3.7	Unit	Notes
			DDR2–533C		
CAS Latency		CL_{IDD}	4	t_{CK}	
Clock Cycle Time		$t_{CK.IDD}$	3.75	ns	
Active to Read or Write delay		$t_{RCD.IDD}$	15	ns	
Active to Active / Auto-Refresh command period		$t_{RC.IDD}$	60	ns	
Active bank A to Active bank B command delay		$t_{RRD.IDD}$	7.5	ns	1)
			10	ns	2)
Active to Precharge Command		$t_{RAS.MIN.IDD}$	45	ns	
		$t_{RAS.MAX.IDD}$	7000	ns	
Precharge Command Period		$t_{RP.IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC.IDD}$	105	ns	
Average periodic Refresh interval	0°C ≤ T_{CASE} ≤ 85°C	t_{REFI}	7.8	µs	
	85°C ≤ T_{CASE} ≤ 95°C	t_{REFI}	3.9	µs	

1) ×4 & ×8 (1 kB page size)
2) ×16 (2 kB page size)

Table 40 I_{DD} Measurement Test Condition for DDR2–400B

Parameter		Symbol	–5	Unit	Notes
			DDR2–400B		
CAS Latency		CL_{IDD}	3	t_{CK}	
Clock Cycle Time		$t_{CK.IDD}$	5	ns	
Active to Read or Write delay		$t_{RCD.IDD}$	15	ns	
Active to Active / Auto-Refresh command period		$t_{RC.IDD}$	55	ns	
Active bank A to Active bank B command delay		$t_{RRD.IDD}$	7.5	ns	1)
			10	ns	2)
Active to Precharge Command		$t_{RAS.MIN.IDD}$	40	ns	
		$t_{RAS.MAX.IDD}$	7000	ns	
Precharge Command Period		$t_{RP.IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC.IDD}$	105	ns	
Average periodic Refresh interval	0°C ≤ T_{CASE} ≤ 85°C	t_{REFI}	7.8	µs	
	85°C ≤ T_{CASE} ≤ 95°C	t_{REFI}	3.9	µs	

1) ×4 & ×8 (1 kB page size)
2) ×16 (2 kB page size)

3.4.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 41 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

Table 42 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–25F–B

Product Type		**HYS64T32000HU–25F–B**	**HYS64T64000HU–25F–B**	**HYS72T64000HU–25F–B**	**HYS64T128020HU–25F–B**	**HYS72T128020HU–25F–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0D	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60	61	61
6	Data Width	40	40	48	40	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40	40	40
11	Error Correction Support (non-ECC, ECC)	00	00	02	00	02
12	Refresh Rate and Type	82	82	82	82	82

Table 42 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–25F–B

Product Type		HYS64T32000HU–25F–B	HYS64T64000HU–25F–B	HYS72T64000HU–25F–B	HYS64T128020HU–25F–B	HYS72T128020HU–25F–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	70	70	70	70	70
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	02	02	02	02	02
21	DIMM Attributes	00	00	00	00	00
22	Component Attributes	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	25	25	25	25	25
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50	50	50
27	$t_{RP.MIN}$ [ns]	32	32	32	32	32
28	$t_{RRD.MIN}$ [ns]	28	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	32	32	32	32	32
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	40	80	80	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	15	15	15	15	15
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	22	22	22	22	22
34	$t_{DS.MIN}$ [ns]	05	05	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E

Table 42 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–25F–B

Product Type		HYS64T32000HU–25F–B	HYS64T64000HU–25F–B	HYS72T64000HU–25F–B	HYS64T128020HU–25F–B	HYS72T128020HU–25F–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	39	39	39	39	39
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E	1E	1E
46	PLL Relock Time	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	56	50	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A	7A	7A
49	ΔT_0 (DT0)	7F	5F	5F	5F	5F
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	3B	3B	3B	3B	3B
51	ΔT_{2P} (DT2P)	36	36	36	36	36
52	ΔT_{3N} (DT3N)	2E	2E	2E	2E	2E
53	$\Delta T_{3P.fast}$ (DT3P fast)	5A	5A	5A	5A	5A
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	68	5A	5A	5A	5A
56	ΔT_{5B} (DT5B)	22	22	22	22	22
57	ΔT_7 (DT7)	3D	27	27	27	27
58	Psi(ca) PLL	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00
62	SPD Revision	12	12	12	12	12

Table 42 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–25F–B

Product Type		HYS64T32000HU–25F–B	HYS64T64000HU–25F–B	HYS72T64000HU–25F–B	HYS64T128020HU–25F–B	HYS72T128020HU–25F–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
63	Checksum of Bytes 0-62	22	07	19	08	1A
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	37	36	37
74	Product Type, Char 2	34	34	32	34	32
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	33	36	36	31	31
77	Product Type, Char 5	32	34	34	32	32
78	Product Type, Char 6	30	30	30	38	38
79	Product Type, Char 7	30	30	30	30	30
80	Product Type, Char 8	30	30	30	32	32
81	Product Type, Char 9	48	48	48	30	30
82	Product Type, Char 10	55	55	55	48	48
83	Product Type, Char 11	32	32	32	55	55
84	Product Type, Char 12	35	35	35	32	32
85	Product Type, Char 13	46	46	46	35	35
86	Product Type, Char 14	42	42	42	46	46
87	Product Type, Char 15	20	20	20	42	42

Table 42 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–25F–B

Product Type		**HYS64T32000HU–25F–B**	**HYS64T64000HU–25F–B**	**HYS72T64000HU–25F–B**	**HYS64T128020HU–25F–B**	**HYS72T128020HU–25F–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**	**PC2–6400U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

Table 43 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–2.5–B

Product Type		HYS64T32000HU–2.5–B	HYS64T64000HU–2.5–B	HYS72T64000HU–2.5–B	HYS64T128020HU–2.5–B	HYS72T128020HU–2.5–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0D	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60	61	61
6	Data Width	40	40	48	40	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40	40	40
11	Error Correction Support (non-ECC, ECC)	00	00	02	00	02
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	70	70	70	70	70
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	02	02	02	02	02
21	DIMM Attributes	00	00	00	00	00
22	Component Attributes	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45	45	45

Table 43 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–2.5–B (cont'd)

Product Type		**HYS64T32000HU–2.5–B**	**HYS64T64000HU–2.5–B**	**HYS72T64000HU–2.5–B**	**HYS64T128020HU–2.5–B**	**HYS72T128020HU–2.5–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50	50	50
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	40	80	80	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	15	15	15	15	15
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	22	22	22	22	22
34	$t_{DS.MIN}$ [ns]	05	05	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E	1E	1E
46	PLL Relock Time	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	55	50	50	50	50
48	Psi(T-A) DRAM	72	7A	7A	7A	7A
49	ΔT_0 (DT0)	6F	5B	5B	5B	5B

Table 43 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–2.5–B (cont'd)

Product Type		**HYS64T32000HU–2.5–B**	**HYS64T64000HU–2.5–B**	**HYS72T64000HU–2.5–B**	**HYS64T128020HU–2.5–B**	**HYS72T128020HU–2.5–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	37	3B	3B	3B	3B
51	ΔT_{2P} (DT2P)	33	36	36	36	36
52	ΔT_{3N} (DT3N)	2B	2E	2E	2E	2E
53	$\Delta T_{3P.fast}$ (DT3P fast)	54	5A	5A	5A	5A
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	62	5A	5A	5A	5A
56	ΔT_{5B} (DT5B)	1F	22	22	22	22
57	ΔT_{7} (DT7)	37	25	25	25	25
58	Psi(ca) PLL	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	09	23	35	24	36
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	37	36	37
74	Product Type, Char 2	34	34	32	34	32

Table 43 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–2.5–B (cont'd)

Product Type		**HYS64T32000HU–2.5–B**	**HYS64T64000HU–2.5–B**	**HYS72T64000HU–2.5–B**	**HYS64T128020HU–2.5–B**	**HYS72T128020HU–2.5–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**	**PC2–6400U–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	33	36	36	31	31
77	Product Type, Char 5	32	34	34	32	32
78	Product Type, Char 6	30	30	30	38	38
79	Product Type, Char 7	30	30	30	30	30
80	Product Type, Char 8	30	30	30	32	32
81	Product Type, Char 9	48	48	48	30	30
82	Product Type, Char 10	55	55	55	48	48
83	Product Type, Char 11	32	32	32	55	55
84	Product Type, Char 12	2E	2E	2E	32	32
85	Product Type, Char 13	35	35	35	2E	2E
86	Product Type, Char 14	42	42	42	35	35
87	Product Type, Char 15	20	20	20	42	42
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

Table 44 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3–B

Product Type		HYS64T32000HU–3–B	HYS64T64000HU–3–B	HYS72T64000HU–3–B	HYS64T128020HU–3–B	HYS72T128020HU–3–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0D	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60	61	61
6	Data Width	40	40	48	40	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	02	00	02
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	02	02	02	02	02
21	DIMM Attributes	00	00	00	00	00
22	Component Attributes	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45	45	45

Table 44 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3–B (cont'd)

Product Type		**HYS64T32000HU–3–B**	**HYS64T64000HU–3–B**	**HYS72T64000HU–3–B**	**HYS64T128020HU–3–B**	**HYS72T128020HU–3–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	30	30	30	30	30
28	$t_{RRD.MIN}$ [ns]	28	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	30	30	30	30	30
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	40	80	80	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	39	39	39	39	39
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22	22	22
46	PLL Relock Time	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	50	50	50	50
48	Psi(T-A) DRAM	72	7A	7A	7A	7A
49	ΔT_0 (DT0)	67	53	53	53	53
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	31	34	34	34	34

Table 44 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3–B (cont'd)

Product Type		**HYS64T32000HU–3–B**	**HYS64T64000HU–3–B**	**HYS72T64000HU–3–B**	**HYS64T128020HU–3–B**	**HYS72T128020HU–3–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
51	ΔT_{2P} (DT2P)	33	36	36	36	36
52	ΔT_{3N} (DT3N)	24	27	27	27	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	4C	4C	4C	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	54	4C	4C	4C	4C
56	ΔT_{5B} (DT5B)	1E	20	20	20	20
57	ΔT_{7} (DT7)	37	25	25	25	25
58	Psi(ca) PLL	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	DF	F7	09	F8	0A
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	37	36	37
74	Product Type, Char 2	34	34	32	34	32
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	33	36	36	31	31

Table 44 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3–B (cont'd)

Product Type		**HYS64T32000HU–3–B**	**HYS64T64000HU–3–B**	**HYS72T64000HU–3–B**	**HYS64T128020HU–3–B**	**HYS72T128020HU–3–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**	**PC2–5300U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
77	Product Type, Char 5	32	34	34	32	32
78	Product Type, Char 6	30	30	30	38	38
79	Product Type, Char 7	30	30	30	30	30
80	Product Type, Char 8	30	30	30	32	32
81	Product Type, Char 9	48	48	48	30	30
82	Product Type, Char 10	55	55	55	48	48
83	Product Type, Char 11	33	33	33	55	55
84	Product Type, Char 12	42	42	42	33	33
85	Product Type, Char 13	20	20	20	42	42
86	Product Type, Char 14	20	20	20	20	20
87	Product Type, Char 15	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	1x	2x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

Table 45 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3S–B

Product Type		HYS64T32000HU–3S–B	HYS64T64000HU–3S–B	HYS72T64000HU–3S–B	HYS64T128020HU–3S–B	HYS72T128020HU–3S–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0D	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60	61	61
6	Data Width	40	40	48	40	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	02	00	02
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	02	02	02	02	02
21	DIMM Attributes	00	00	00	00	00
22	Component Attributes	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50	50

Table 45 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3S–B (cont'd)

Product Type		HYS64T32000HU–3S–B	HYS64T64000HU–3S–B	HYS72T64000HU–3S–B	HYS64T128020HU–3S–B	HYS72T128020HU–3S–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	40	80	80	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22	22	22
46	PLL Relock Time	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	50	50	50	50
48	Psi(T-A) DRAM	72	7A	7A	7A	7A
49	ΔT_0 (DT0)	5F	4B	4B	4B	4B

Table 45 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3S–B (cont'd)

Product Type		**HYS64T32000HU–3S–B**	**HYS64T64000HU–3S–B**	**HYS72T64000HU–3S–B**	**HYS64T128020HU–3S–B**	**HYS72T128020HU–3S–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	31	34	34	34	34
51	ΔT_{2P} (DT2P)	33	36	36	36	36
52	ΔT_{3N} (DT3N)	24	27	27	27	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	4C	4C	4C	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	54	4C	4C	4C	4C
56	ΔT_{5B} (DT5B)	1E	20	20	20	20
57	ΔT_{7} (DT7)	34	23	23	23	23
58	Psi(ca) PLL	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	07	20	32	21	33
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	37	36	37
74	Product Type, Char 2	34	34	32	34	32

Table 45 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3S–B (cont'd)

Product Type		**HYS64T32000HU–3S–B**	**HYS64T64000HU–3S–B**	**HYS72T64000HU–3S–B**	**HYS64T128020HU–3S–B**	**HYS72T128020HU–3S–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**	**PC2–5300U–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	33	36	36	31	31
77	Product Type, Char 5	32	34	34	32	32
78	Product Type, Char 6	30	30	30	38	38
79	Product Type, Char 7	30	30	30	30	30
80	Product Type, Char 8	30	30	30	32	32
81	Product Type, Char 9	48	48	48	30	30
82	Product Type, Char 10	55	55	55	48	48
83	Product Type, Char 11	33	33	33	55	55
84	Product Type, Char 12	53	53	53	33	33
85	Product Type, Char 13	42	42	42	53	53
86	Product Type, Char 14	20	20	20	42	42
87	Product Type, Char 15	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	2x	2x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

Table 46 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3.7–B

Product Type		HYS64T32000HU–3.7–B	HYS64T64000HU–3.7–B	HYS72T64000HU–3.7–B	HYS64T128020HU–3.7–B	HYS72T128020HU–3.7–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0D	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60	61	61
6	Data Width	40	40	48	40	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	00	00	02	00	02
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	02	02	02	02	02
21	DIMM Attributes	00	00	00	00	00
22	Component Attributes	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50	50

Table 46 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3.7–B (cont'd)

Product Type		**HYS64T32000HU–3.7–B**	**HYS64T64000HU–3.7–B**	**HYS72T64000HU–3.7–B**	**HYS64T128020HU–3.7–B**	**HYS72T128020HU–3.7–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	40	80	80	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28	28	28
46	PLL Relock Time	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	50	50	50	50
48	Psi(T-A) DRAM	72	7A	7A	7A	7A
49	ΔT_0 (DT0)	53	43	43	43	43

Table 46 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3.7–B (cont'd)

Product Type		HYS64T32000HU–3.7–B	HYS64T64000HU–3.7–B	HYS72T64000HU–3.7–B	HYS64T128020HU–3.7–B	HYS72T128020HU–3.7–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	29	2C	2C	2C	2C
51	ΔT_{2P} (DT2P)	33	36	36	36	36
52	ΔT_{3N} (DT3N)	1F	21	21	21	21
53	$\Delta T_{3P.fast}$ (DT3P fast)	3D	41	41	41	41
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	46	40	40	40	40
56	ΔT_{5B} (DT5B)	1C	1E	1E	1E	1E
57	ΔT_{7} (DT7)	32	22	22	22	22
58	Psi(ca) PLL	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	16	34	46	35	47
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	37	36	37
74	Product Type, Char 2	34	34	32	34	32

Table 46 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–3.7–B (cont'd)

Product Type		HYS64T32000HU–3.7–B	HYS64T64000HU–3.7–B	HYS72T64000HU–3.7–B	HYS64T128020HU–3.7–B	HYS72T128020HU–3.7–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**	**PC2–4200U–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	33	36	36	31	31
77	Product Type, Char 5	32	34	34	32	32
78	Product Type, Char 6	30	30	30	38	38
79	Product Type, Char 7	30	30	30	30	30
80	Product Type, Char 8	30	30	30	32	32
81	Product Type, Char 9	48	48	48	30	30
82	Product Type, Char 10	55	55	55	48	48
83	Product Type, Char 11	33	33	33	55	55
84	Product Type, Char 12	2E	2E	2E	33	33
85	Product Type, Char 13	37	37	37	2E	2E
86	Product Type, Char 14	42	42	42	37	37
87	Product Type, Char 15	20	20	20	42	42
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	2x	2x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

Table 47 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–5–B

Product Type		HYS64T32000HU–5–B	HYS64T64000HU–5–B	HYS72T64000HU–5–B	HYS64T128020HU–5–B	HYS72T128020HU–5–B
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0D	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60	61	61
6	Data Width	40	40	48	40	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	50	50	50	50	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	60	60	60	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	02	00	02
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	02	02	02	02	02
21	DIMM Attributes	00	00	00	00	00
22	Component Attributes	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	50	50	50	50	50
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	60	60	60	60	60

Table 47 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–5–B (cont'd)

Product Type		**HYS64T32000HU–5–B**	**HYS64T64000HU–5–B**	**HYS72T64000HU–5–B**	**HYS64T128020HU–5–B**	**HYS72T128020HU–5–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	28	28	28	28	28
31	Module Density per Rank	40	80	80	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35	35	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47	47	47	47
34	$t_{DS.MIN}$ [ns]	15	15	15	15	15
35	$t_{DH.MIN}$ [ns]	27	27	27	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28	28	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	37	37	37	37	37
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23	23	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D	2D	2D	2D
46	PLL Relock Time	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	50	50	50	50
48	Psi(T-A) DRAM	72	7A	7A	7A	7A
49	ΔT_0 (DT0)	4B	3B	3B	3B	3B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	25	27	27	27	27

Table 47 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–5–B (cont'd)

Product Type		**HYS64T32000HU–5–B**	**HYS64T64000HU–5–B**	**HYS72T64000HU–5–B**	**HYS64T128020HU–5–B**	**HYS72T128020HU–5–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
51	ΔT_{2P} (DT2P)	33	36	36	36	36
52	ΔT_{3N} (DT3N)	1C	1E	1E	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	34	38	38	38	38
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	3E	38	38	38	38
56	ΔT_{5B} (DT5B)	1B	1D	1D	1D	1D
57	ΔT_{7} (DT7)	30	21	21	21	21
58	Psi(ca) PLL	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	6D	8B	9D	8C	9E
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	37	36	37
74	Product Type, Char 2	34	34	32	34	32
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	33	36	36	31	31

Table 47 SPD Codes for HYS[64/72]T[32/64/128]xxxHU–5–B (cont'd)

Product Type		**HYS64T32000HU–5–B**	**HYS64T64000HU–5–B**	**HYS72T64000HU–5–B**	**HYS64T128020HU–5–B**	**HYS72T128020HU–5–B**
Organization		**256 MB**	**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**	**PC2–3200U–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
77	Product Type, Char 5	32	34	34	32	32
78	Product Type, Char 6	30	30	30	38	38
79	Product Type, Char 7	30	30	30	30	30
80	Product Type, Char 8	30	30	30	32	32
81	Product Type, Char 9	48	48	48	30	30
82	Product Type, Char 10	55	55	55	48	48
83	Product Type, Char 11	35	35	35	55	55
84	Product Type, Char 12	42	42	42	35	35
85	Product Type, Char 13	20	20	20	42	42
86	Product Type, Char 14	20	20	20	20	20
87	Product Type, Char 15	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	2x	2x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

5 Package Outlines

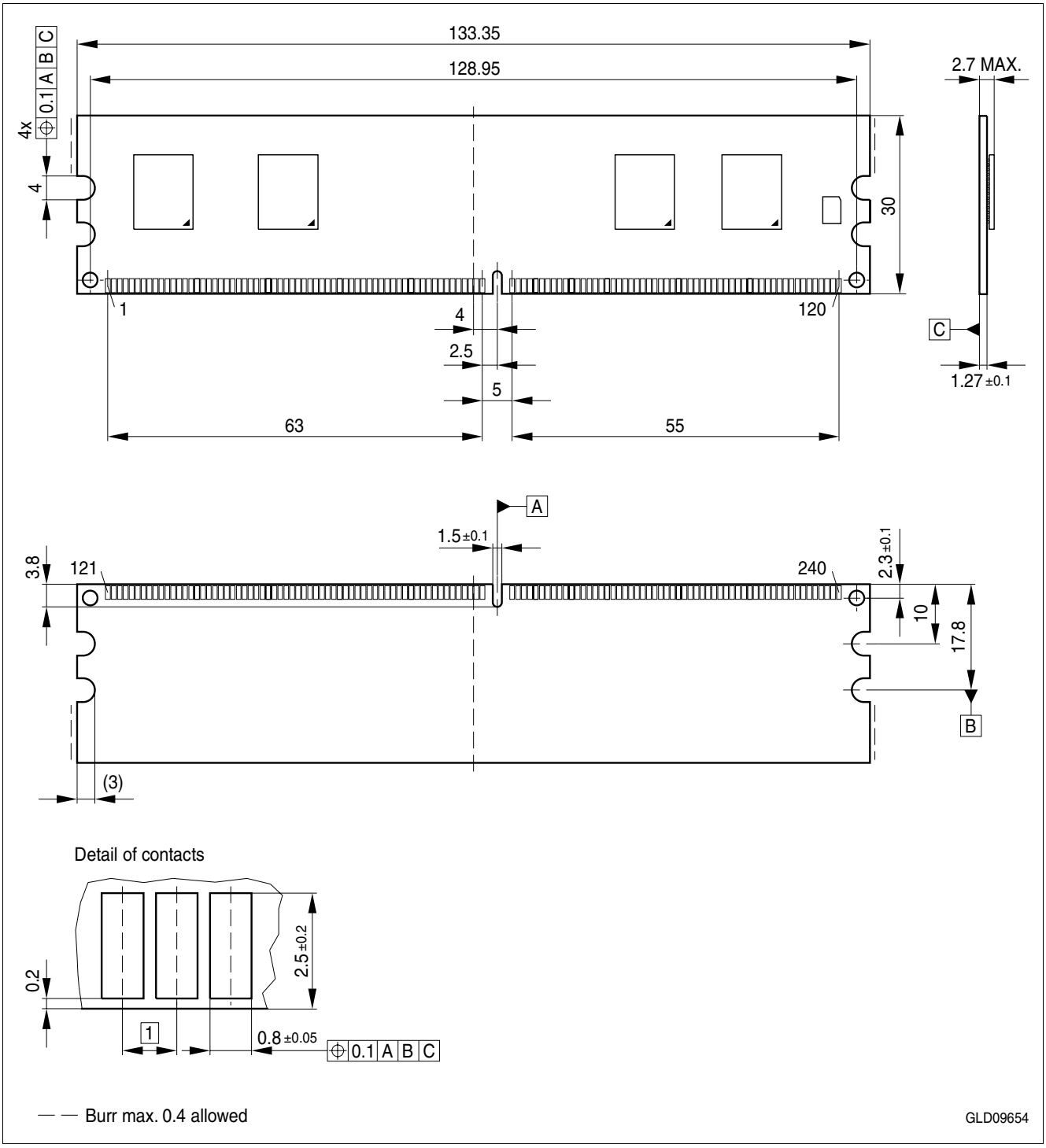

Figure 8 Package Outline Raw Card C – L-DIM-240-3

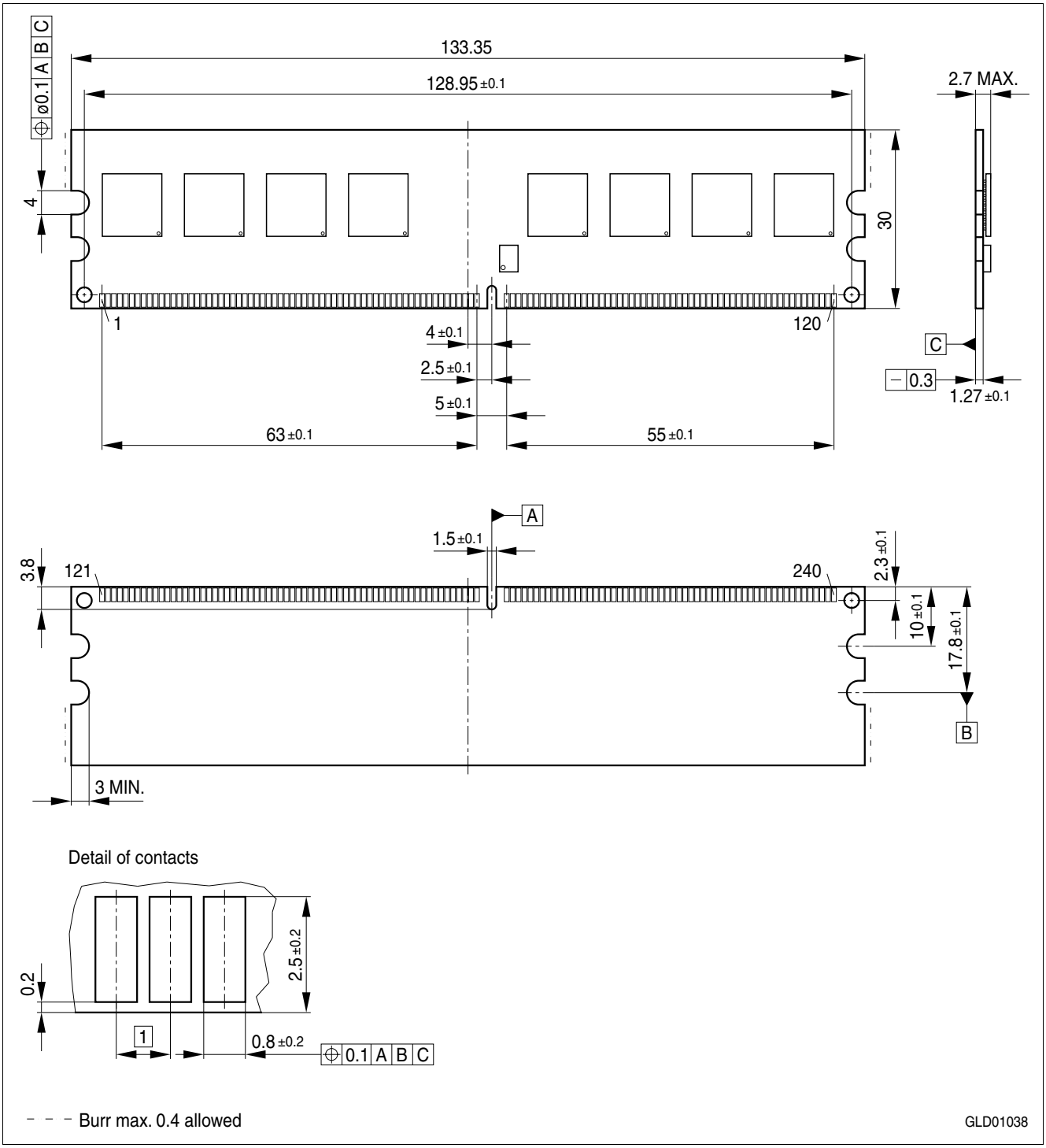

Figure 9 Package Outline Raw Card D L-DIM-240-8

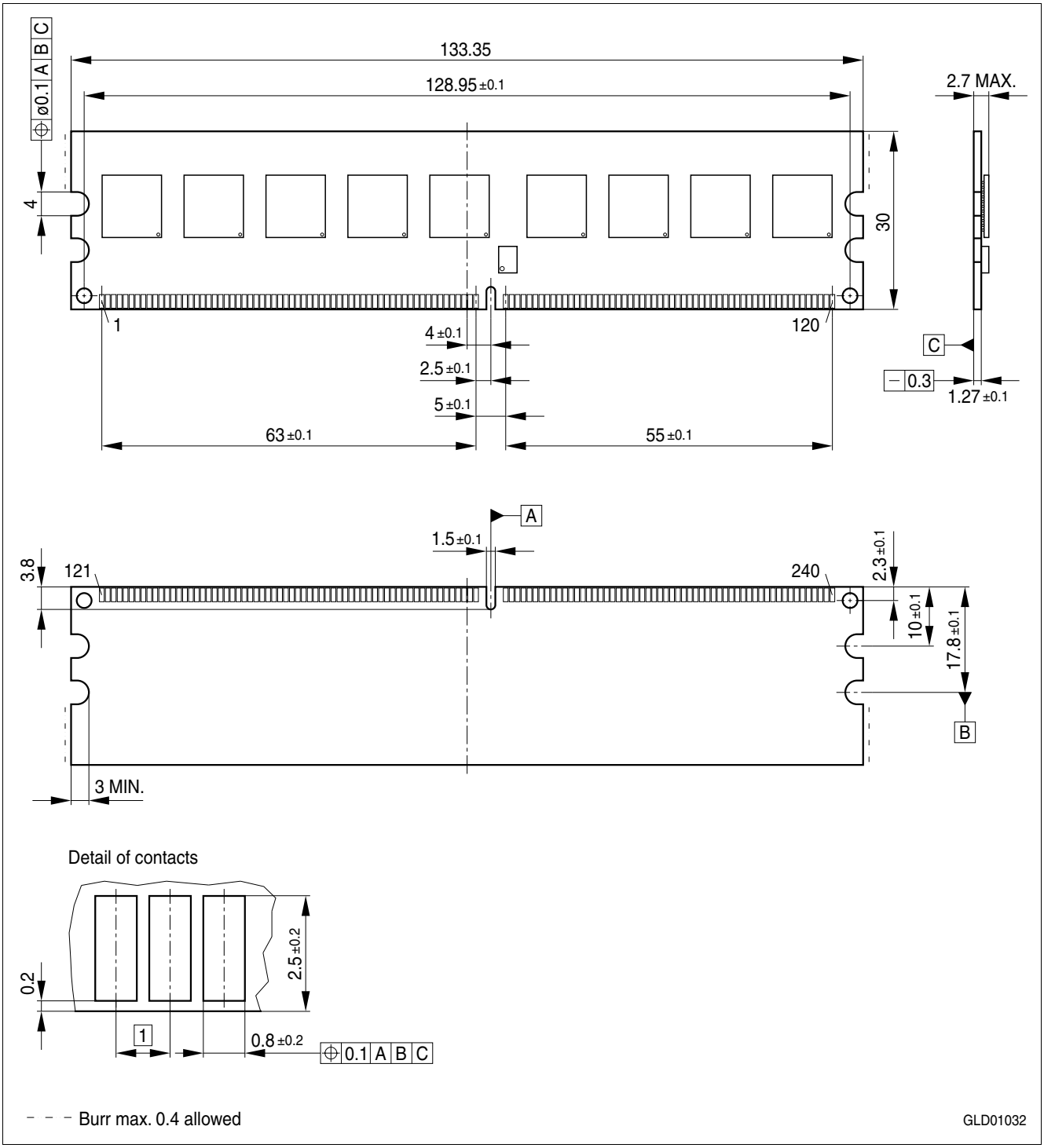

Figure 10 Package Outline Raw Card F L-DIM-240-6

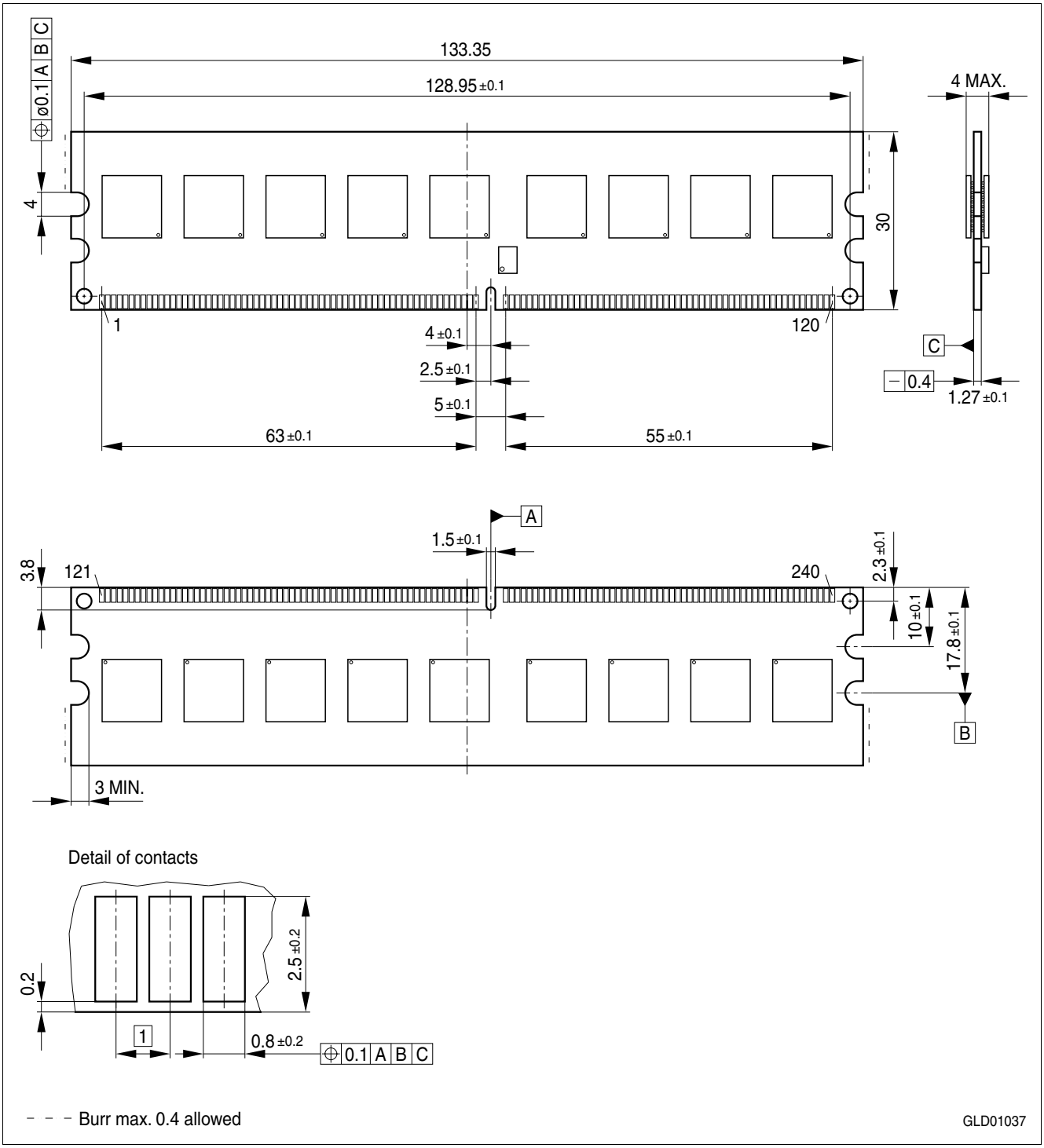

Figure 11 Package Outline Raw Card G L-DIM-240-7

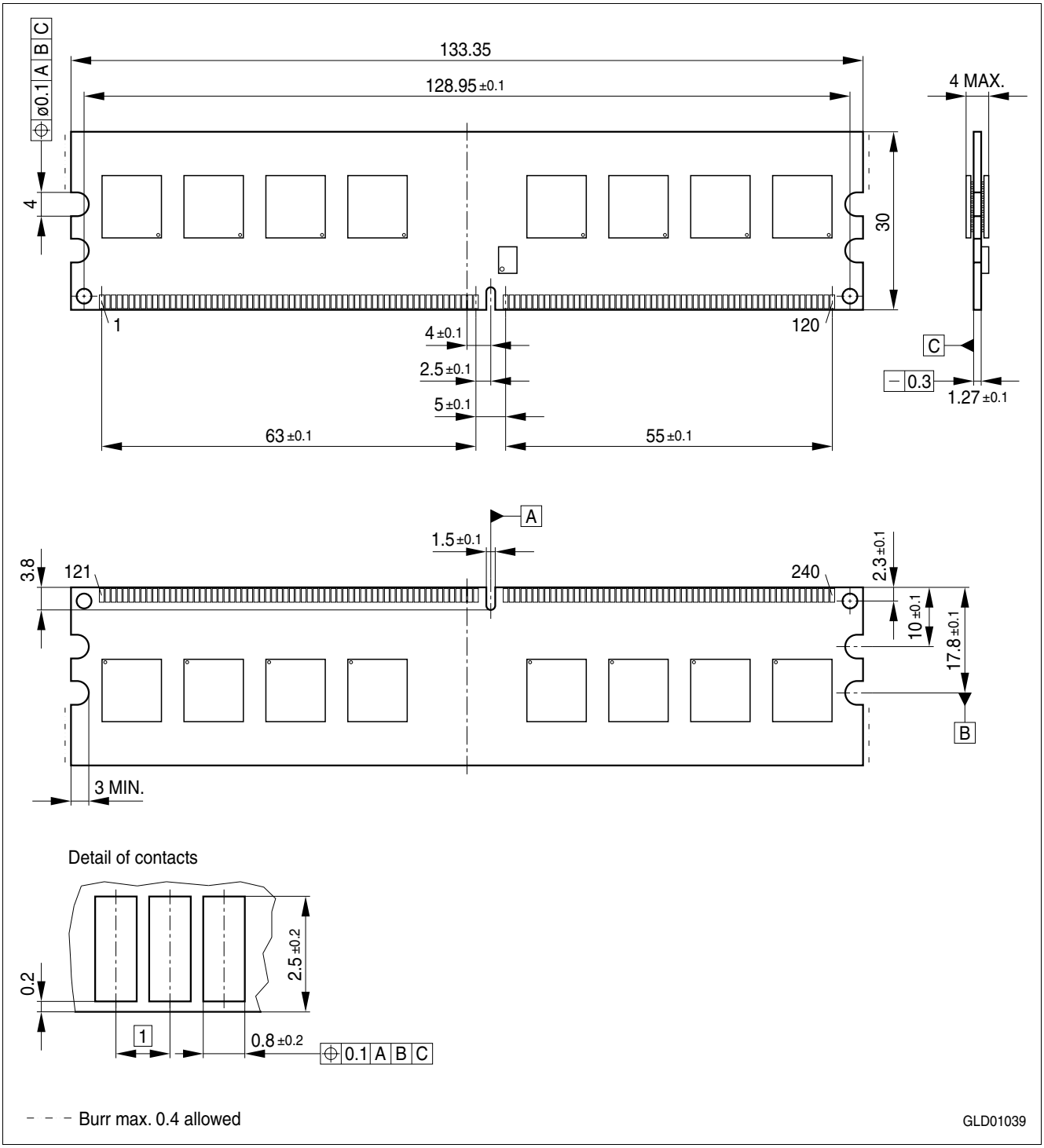

Figure 12 Package Outline Raw Card E L-DIM-240-9

6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some propriatory coding. Table 48 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 49 and for components in Table 50.

Table 48 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 49 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered
10	Speed Grade	–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 50 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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