Data Sheet, V1.0, Aug. 1999

FOA3251B1

High Speed Clock and Data Recovery for Fiber Optic Applications

ICs for Communications

Infineon technologies

Never stop thinking.

FOA3251B1
S1028C1
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Previous Version:

Page	Subjects (major changes since last revision)
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Preface

The transceiver IC FOA3251 is designed for fibre optic application in the data bit range of 2.5 GBit. The FOA3251 fulfills the jitter requirements specified in ITU G958 and Bellcore GR253.

Organization of this Document

This Data Sheet is divided into 8 chapters. It is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product , lists the key features, and presents some typical applications.
- **Chapter 2, Functional Description**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
  Blockdiagram and block description.
- **Chapter 3, Operational Description**
- **Chapter 4, Electrical Characteristics**
  DC and AC Characteristics, Power consumption, interface specification.
- **Chapter 5, External Components**
  Application notes and recommended suppliers
- **Chapter 6, Measurement Results**
- **Chapter 7, Package Outlines**

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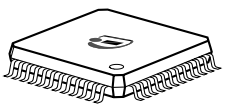
BIPOLAR

1 Overview

The transceiver IC FOA3251 is designed for fibre optic application in the data bit range of 2.5 GBit. The FOA3251 fulfills the jitter requirements specified in ITU G958 and Bellcore GR253.



P-LQFP-48-1

1.1 Features

- Data rate up to 2.633 Gb/s
- All jitter data meet ITU-T G958 and GR-253-Core requirements
- Supply range from +3.0 V to 5.0 V
- Supply current < 210 mA
- Input sensitivity < 5 mVpp differential (BER = 10^{-12})
- Loss of signal (LOS) detection
- Programmable delay element to adjust clock- to data output
- Lock indication

1.2 Applications

- Fibre optic communication systems
- SDH / SONET / ATM applications

Type	Ordering Code	Package
FOA3251B1		P-LQFP-48-1

2 Functional Description

The FOA3251 consists of a clock and data recovery block (CDR), a clock multiplier unit (CMU) and a programmable delay line.

2.1 Pin Configuration (top view)

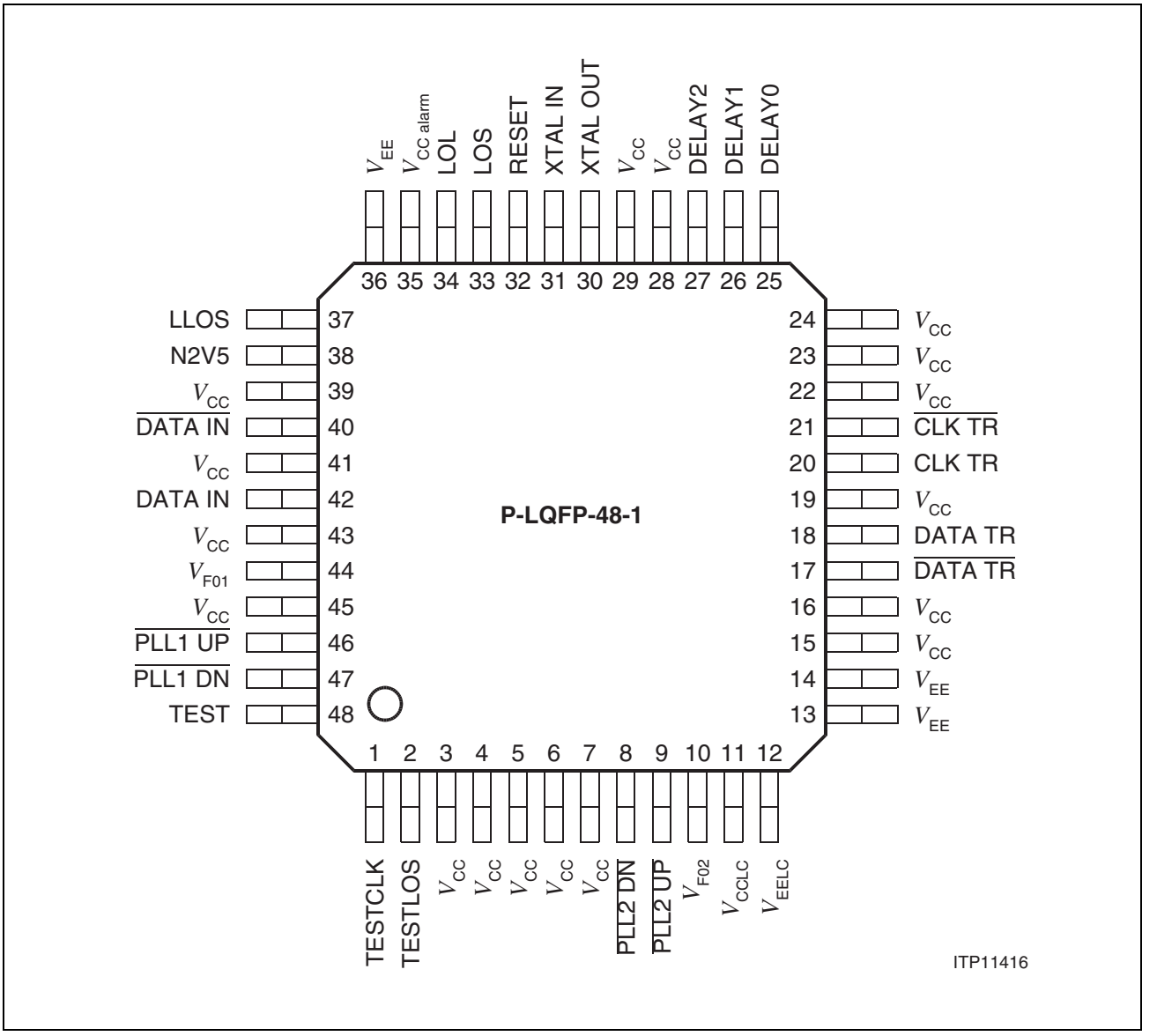


Figure 1 Pin Configuration

2.2 Pin Definition and Function

Table 1 Pin Definition and Function

Pin	Symbol	Input (I) Output (O)	Function
1	TESTCLK	In	Clock signal for test mode only
2	TESTLOS	In	
3	V_{CC}		
4	V_{CC}		Can be open.
5	V_{CC}		Can be open.
6	V_{CC}		
7	V_{CC}	In	Can be open.
8	$\overline{\text{PLL2 DN}}$	Out	Inverted down signal from PLL2
9	$\overline{\text{PLL2 UP}}$	Out	Inverted up signal from PLL2
10	V_{F02}	In	Control voltage for VCO2
11	V_{CCLC}		V_{CC} V_{CO2}
12	V_{EELC}		V_{EE} V_{CO2}
13	V_{EE}		
14	V_{EE}		
15	V_{CC}		
16	V_{CC}		
17	$\overline{\text{DATA TR}}$	Out	Inverted recovered data signal
18	DATA TR	Out	Recovered data signal
19	V_{CC}		
20	CLK TR	Out	Recovered clock signal
21	$\overline{\text{CLK TR}}$	Out	Inverted recovered clock signal
22	V_{CC}		
23	V_{CC}		
24	V_{CC}		
25	DELAY0	In	Delay select bit 0. (See **Table 2**)
26	DELAY1	In	Delay select bit 1. (See **Table 2**)
27	DELAY2	In	Delay select bit 2. (See **Table 2**)
28	V_{CC}		

Table 1 Pin Definition and Function (cont'd)

Pin	Symbol	Input (I) Output (O)	Function
29	V_{CC}		
30	XTAL OUT	Out	Crystal
31	XTAL IN	In	Crystal
32	RESET	In	Reset for test mode only
33	LOS	Out	Loss of signal (ESD only to V_{EE})
34	LOL	Out	Loss of Lock
35	$V_{CC\ alarm}$		$V_{CC\ alarm}$ supply. Max. 5 V, Min 0 V = V_{CC} (no ESD)
36	V_{EE}		
37	LLOS	In	Adjustment for Level LOS
38	N2V5	In	Negative supply voltage for V_{CO1}
39	V_{CC}		
40	$\overline{\text{DATA IN}}$	In	Inverted data input (no ESD)
41	V_{CC}		
42	DATA IN	In	Data input (no ESD)
43	V_{CC}		
44	V_{F01}	In	Control voltage V_{CO1}
45	V_{CC}		
46	$\overline{\text{PLL1 UP}}$		Inverted up signal PLL1
47	$\overline{\text{PLL1 DN}}$		Inverted down signal PLL1
48	TEST	In	Test mode on/off

2.3 Functional Block Diagram

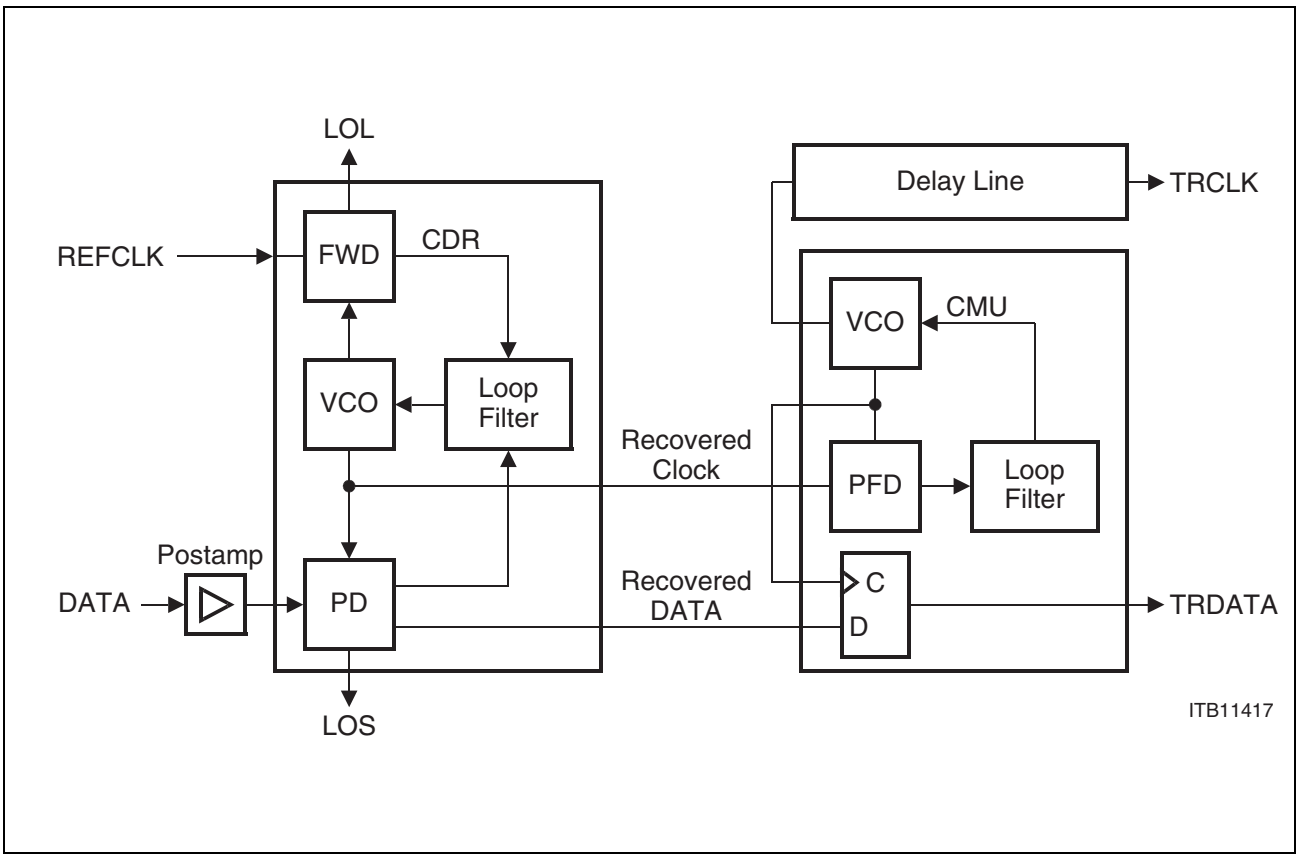


Figure 2 Block Diagram

2.4 Functional Block Description

The clock and data recovery block (CDR) consists of a bang-bang phase detector (PD), a frequency window detector (FWD) and a VCO. The PD also provides a kind of statistical BER signal that is used to generate a loss of signal (LOS) signal. The FWD moves the VCO in the right frequency range. The frequency window is about 10000 ppm of the center frequency. When the frequency is out of range a los of lock signal (LOL) is generated. The center frequency is given by a reference clock signal which is (signal frequency)/128. The VCO is a 3 stage ring oscillator type.

The clock multiplier unit (CMU) consist of a phase frequency detector (PFD), a VCO and a retiming Flip-Flop. The PFD is type 4 phase and frequency detector. The low pass filtered PFD signal as a function of the phase error is shown in **Figure 3**.

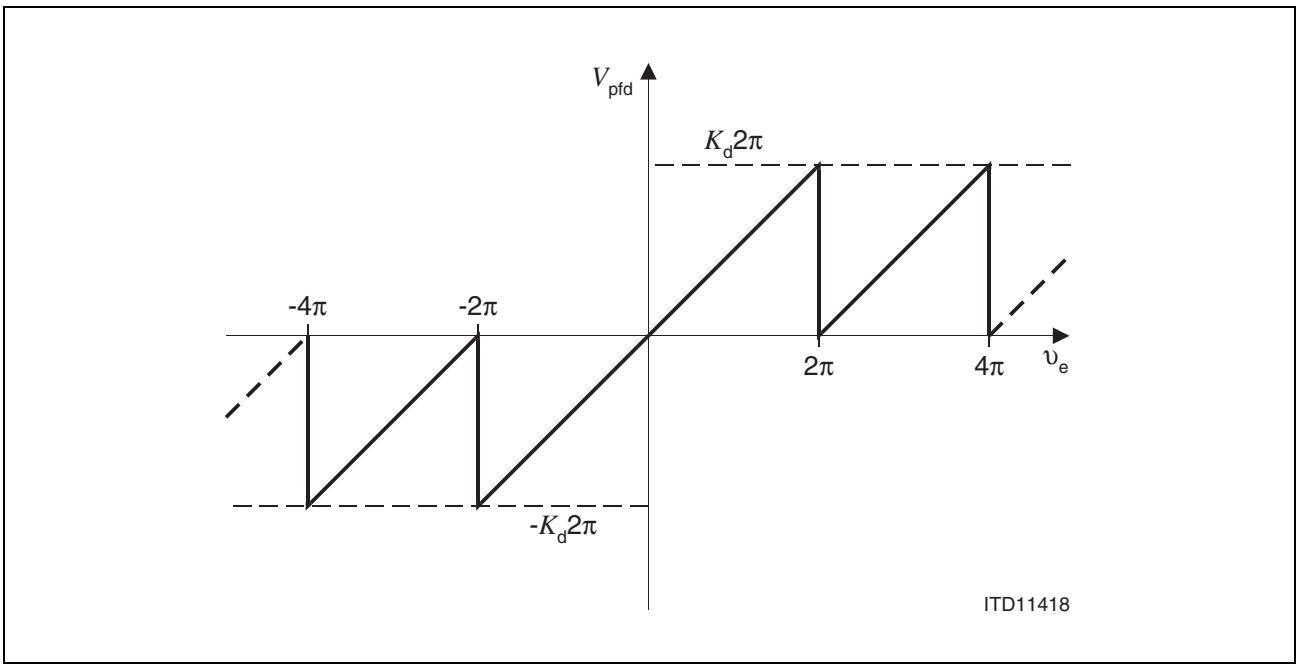


Figure 3 PFD Characteristic

The VCO is a LC type with a center frequency of 2.5 GHz. The measured tuning range is shown in **Figure 4**.

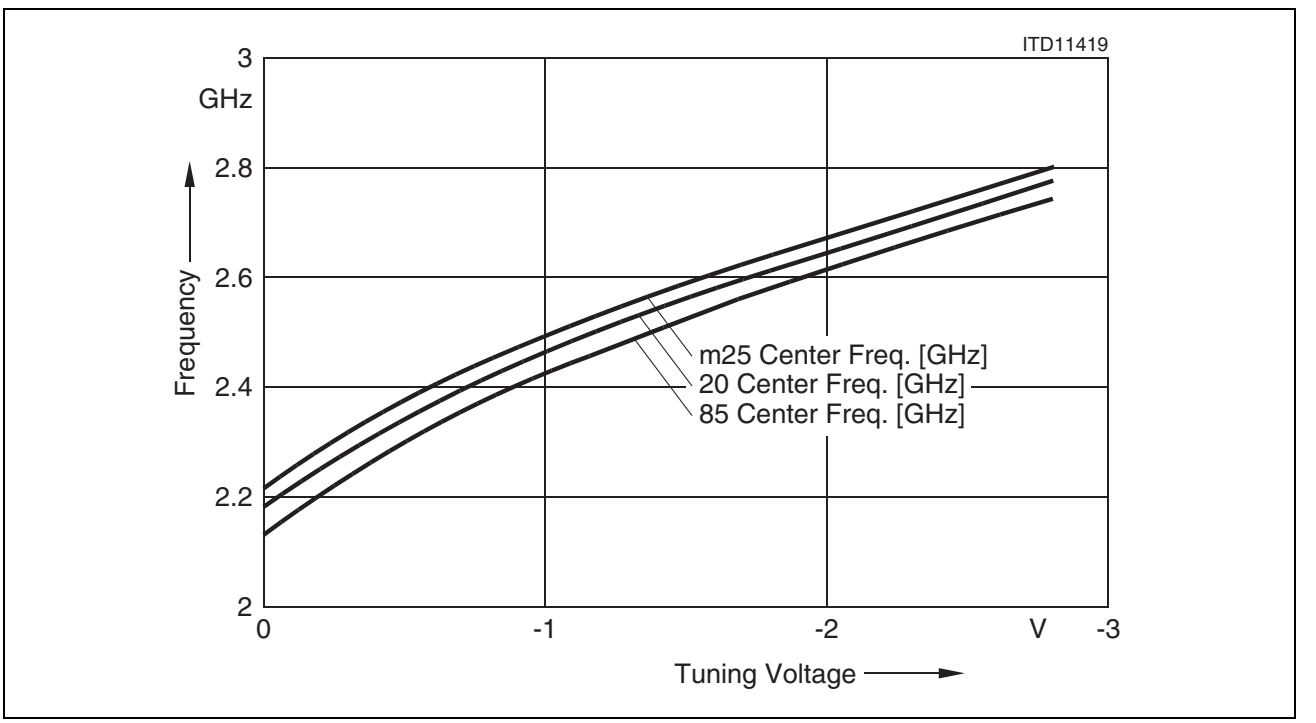


Figure 4 Tuning Range LC VCO

The delay line is programmable in 8 steps of about 50 ps. The clock signal is adjustable over 1 period (400 as) and can be easily adapted to different applications.

3 Operational Description

3.1 Operating States of Delay Line

For clock to data output adjustment a adjustable delay line is available. The clock output signal is adjustable by the signals DELAY0..2.

Table 2 Truth Table Delay Line

DELAY0	DELAY1	DELAY2	Delta
LOW	LOW	LOW	0 ps
LOW	HIGH	LOW	50 ps
LOW	LOW	HIGH	100 ps
LOW	HIGH	HIGH	150 ps
HIGH	LOW	LOW	200 ps
HIGH	HIGH	LOW	250 ps
HIGH	LOW	HIGH	300 ps
HIGH	HIGH	HIGH	350 ps

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
IC supply voltage (V_{CC} - V_{EE})			6	V
Voltage on any pin	V_S	-0.4	V_{DDP} + 0.4	
Maximum junction temperature			125	°C
Storage temperature	T_{stg}	-40	150	
Protection supply voltage	V_{DDP}	V_{EE} - 0.5	V_{CC}	V
ESD robustness HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$		500	
Lead temperature range			Package	

The RF Pin 40, 42 are not ESD protected. The high frequency performance prohibits the use of a adequate protective structure. Pin 33 is only protected to V_{EE}.

4.2 Operating Range

Table 4 Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature	T_A	-40	85	°C
Supply voltage	V_{DD}	3.0	5	V

4.3 DC Characteristics

Table 5 DC Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Control and Test inputs	V_{IL} V_{IH}	V_{CC} - 1	 V_{CC}	V
Output current CML Pin 17, 18, 20, 21	I_{oc}	8	0.45	mA
Supply current	I_{EE} (AV)	200	TBD	mA

4.4 AC Characteristics

Table 6 Electrical Characteristics

Parameter	Condition	Limit Values			Unit
		min.	typ.	max.	
Quantisizer					
DC Characteristics[1)]	Pin or Nin	V_{EE} +2.5		V_{CC}	V
Input Voltage Range[2)]	Pin-Nin, BER < 10^{-12}		10		mV
Input Sensitivity, V_{sense}	Pin-Nin, BER < 10^{-12}				V
Input Overdrive, V_{od}			2		mV
Input Offset Voltage				10	µA
Input Current					
Input RMS Noise	BER < 10^{-12}		TBD		µV
Input Pk-Pk Noise	BER < 10^{-12}		TBD		
Quantisizer					
AC Characteristics			2.5		GHz
Upper -3 dB Bandwidth extern)			50		Ω
Input Resistance	Package			0.8	pF
Input Capacitance					
Pulse Width Distortion					
VSWR				2.5	

Table 6 Electrical Characteristics (cont'd)

Parameter	Condition	Limit Values			Unit
		min.	typ.	max.	
Level Detect					
Response Time	AC coupled			95	µs
Hysteresis (Electrical)[3]		1		3	db
ALM Output Logic High[4]	$V_{CC\ alarm}$ = 5 V		4.5		V
ALM Output Logic Low	$V_{EE\ alarm}$ = GND		1		
ALM Output Logic High	$V_{CC\ alarm}$ = GND		-0.5		
ALM Output Logic Low	$V_{EE\ alarm}$ = -5 V		-4		
Phase-Locked Loop					
Nominal Center Frequency f_0			2.48832		GHz
Capture Range[5]		-0.2% x f_0		+0.2% x f_0	GHz
Tracking Range		-0.2% x f_0		+0.2% x f_0	
Static Phase Error[6]		-3.6		+3.6	deg.
Phase drift[7]		100			Bit
Jitter	SONET STS-48 Frame (with Scrambler 2E7-1) and 2E23-1 PRN Sequence ITU-T G958 and Gr-253-Core objective < 0.005 UIrms (2ps)				
Jitter Tolerance	SONET STS-48 Frame (with Scrambler 2E7-1) and 2E23-1 PRN Sequence ITU-T G958 and Gr-253-Core				
Jitter Transfer	SONET STS-48 Frame (with Scrambler 2E7-1) and 2E23-1 PRN Sequence ITU-T G958 and Gr-253-Core				
Open collector output	Referenced to V_{CC}				
Voltage levels					
Output logic High, V_{oh}			0		V
Output logic Low, V_{ol}			400		V
Symmetry (Duty Cycle)					
Recovered Clock Output		46		54	

Table 6 Electrical Characteristics (cont'd)

Parameter	Condition	Limit Values			Unit
		min.	typ.	max.	
Output Rise/Fall Times					
Clock Output					
Rise Time	20% - 80%, 50 Ω		100		ps
Fall Time	20% - 80%, 50 Ω		100		ps
Data Output					
Rise Time	20% - 80%, 50 Ω		120		ps
Fall Time	20% - 80%, 50 Ω		120		ps
Control and test inputs[8]	Referenced to V_{CC}				
Input logic High, V_{ih}			0		V
Input logic Low, V_{il}			-1		V
Control and test outputs	Referenced to V_{CC}				
Output logic High, V_{ih}			0		V
Output logic Low, V_{il}			-1		V
Power Supply Voltage		3	5	5.8	V
Power Supply Current[9]			210		mA
Operating Temperature					
Package Ambient		-40		+85	°C
Bare Chip Ambient		-40		+100	°C
Bare Chip Size		< 3.0 mm x 3.0 mm			

1) Min value Pin, Nin: V_{CC}-Pin, Nin < 800 mV
2) Voltage (Pin-Nin) = 4 mVpp @Pin = -23 dBm
3) Hysteresis can be installed by a combination of Signal LOS and LLOS.
4) Open Collector Output type, I = 2 mA. Datarate depends on output load. Termination with pullup resistor > 4.7 kΩ
5) No skipping clock cycles allowed down to < 10^{-3} BER External adjustable.
6) Clock drift with no input 25 MHz
7) The alarm shall be asserted before 500 ns of phase shift on the RX clock is realized.
8) Consecutive identical bits 72 bits.
9) Supply current = I_{EE} (current without ECL output current).

5 External Components

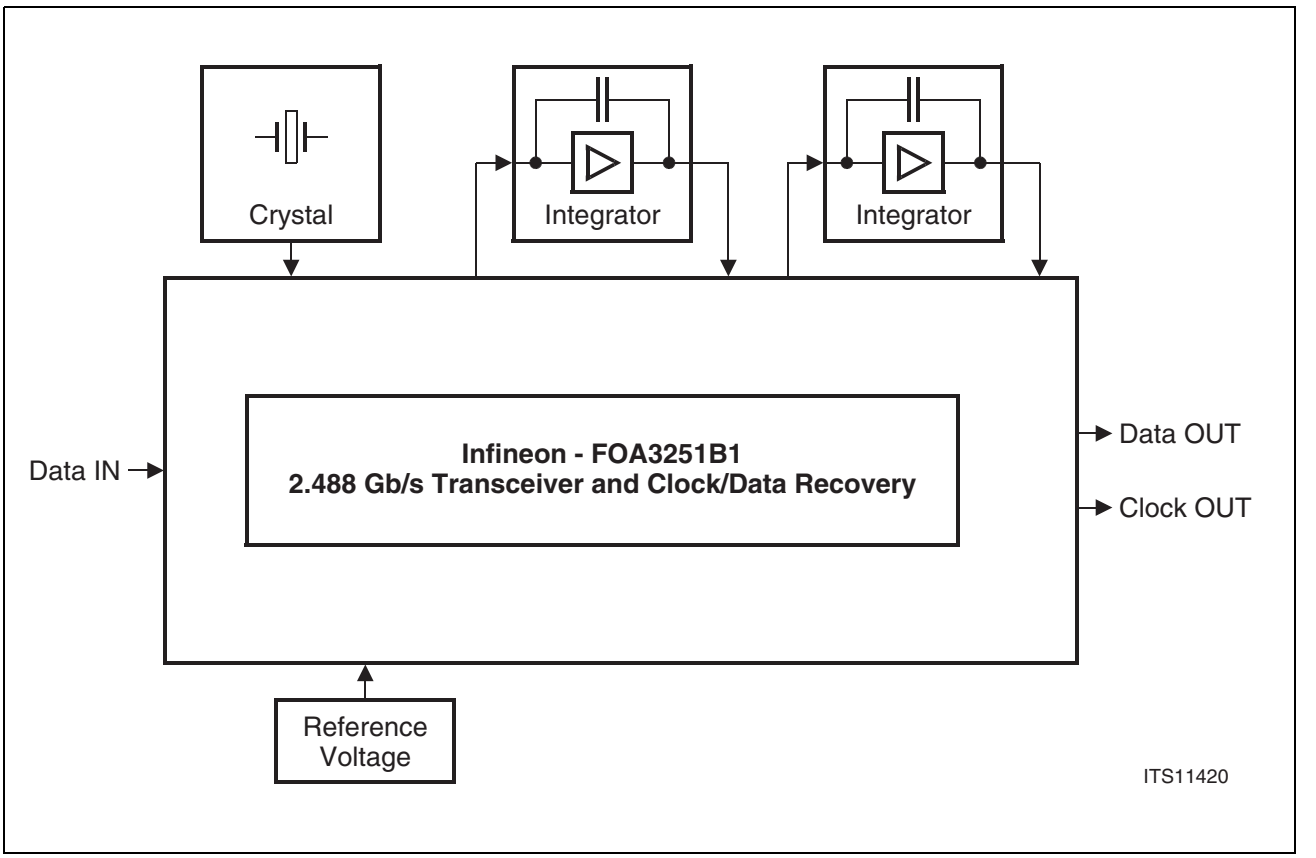


Figure 5 External Components Required for Operation of FOA3251B1

Table 7 External Devices

Device	Number	Recommended Types	Remark
Reference Voltage	1 - 2	TL 431	2.5 V VCO Supply
Operational Amplifier	1	Burr Brown OPA2353 Burr Brown OPA2350	Integrator
Capacitor	10 5		Integrator, Blocking
Resistor	14		Integrator, Reference voltage
Crystal Oscillator	1	Toyocom TSX-2	19.44 MHz
Ferrite Bead Inductor	2	muRata BLM11B601S	V_{EE} blocking to GND (V_{CC})

The external circuits are shown in **Figure 6**, **Figure 7**, **Figure 8** and **Figure 9**.

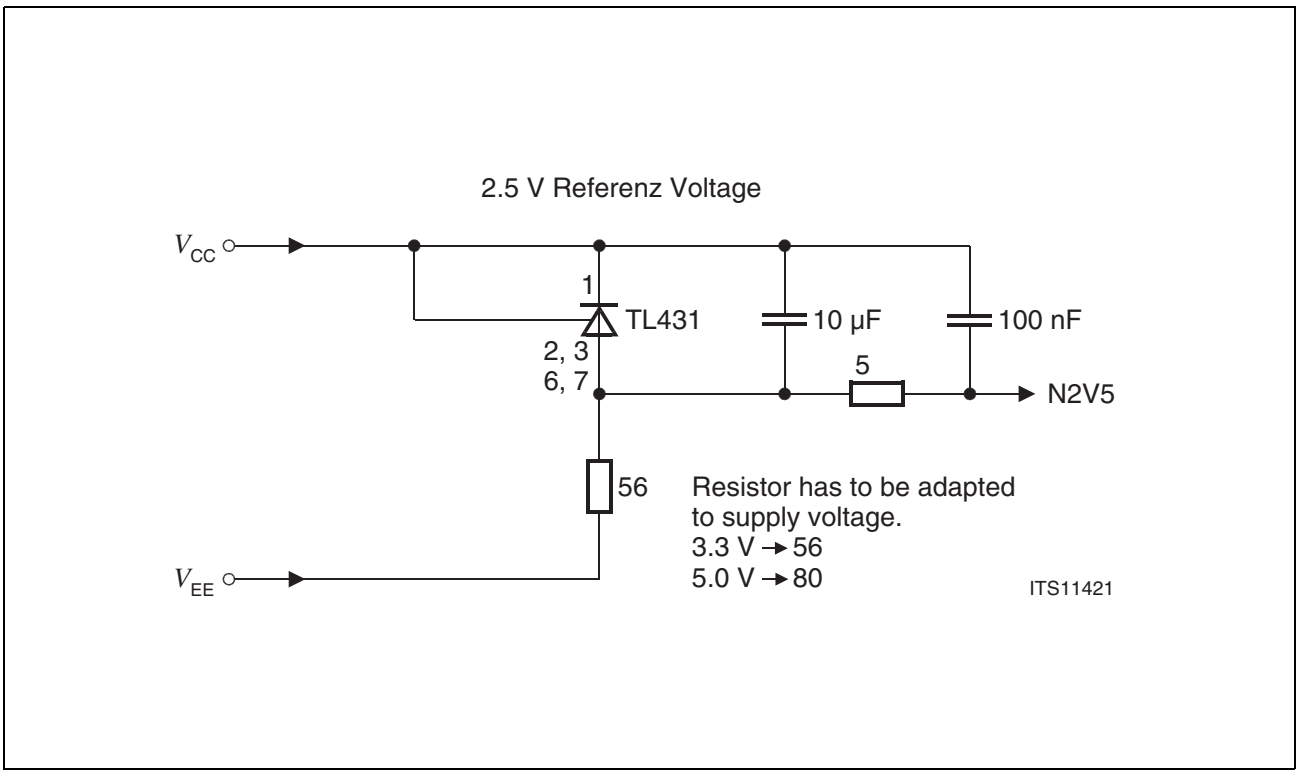


Figure 6 Reference Voltage for VCO (Ring Oscillator).

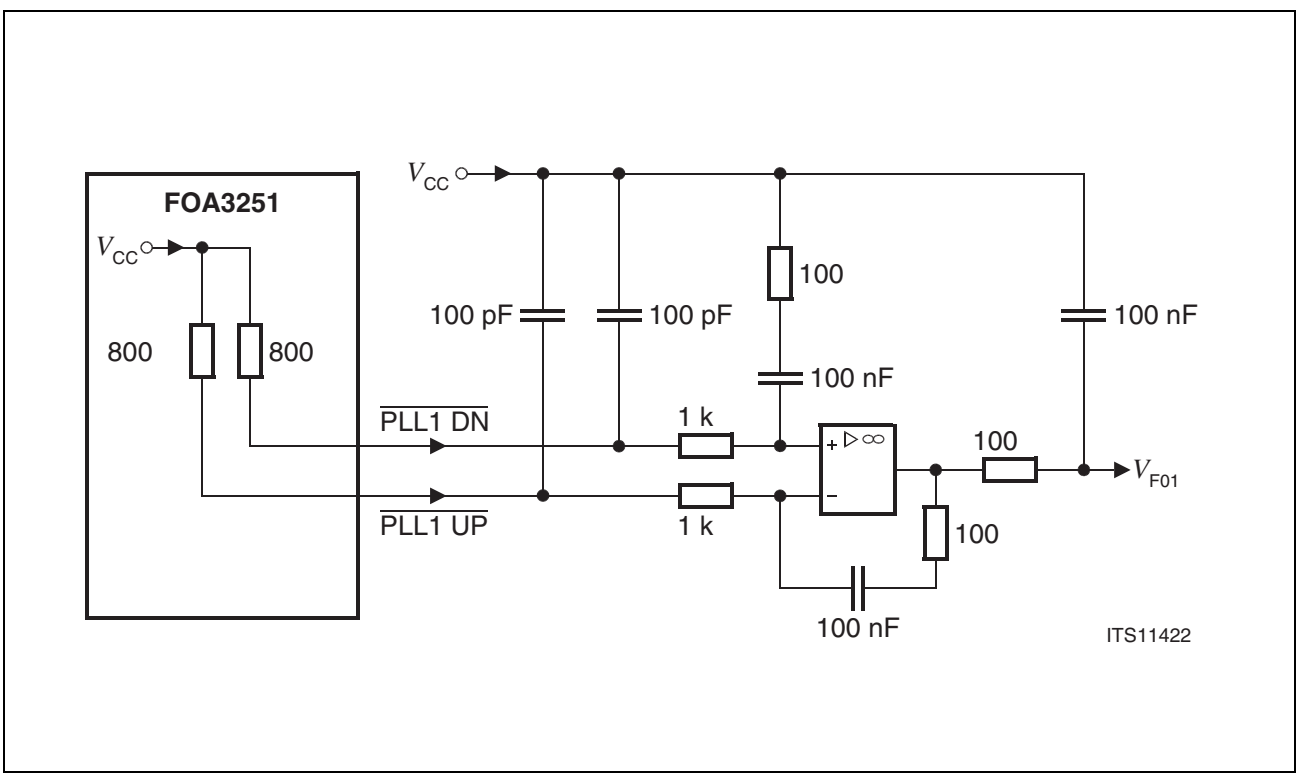


Figure 7 Loop Filter PLL1 (CDR)

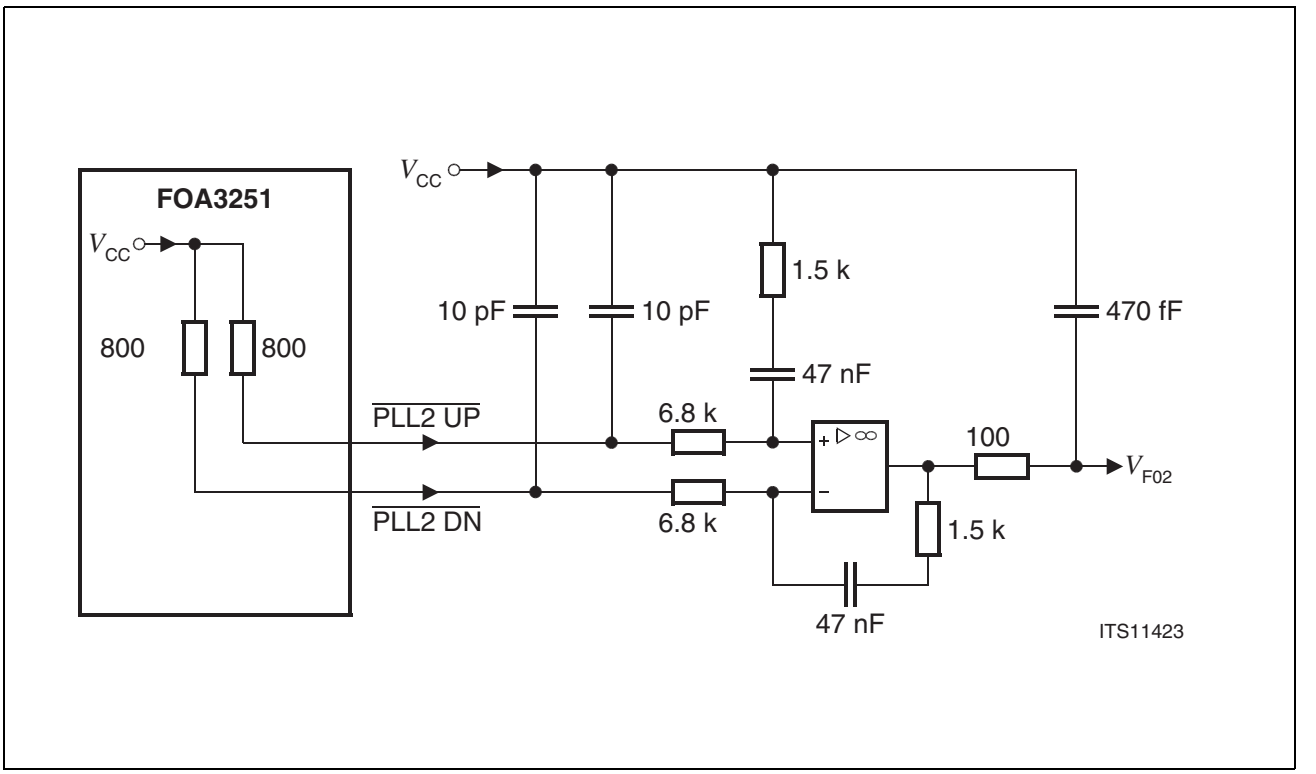


Figure 8 Loop Filter PLL2 (CMU)

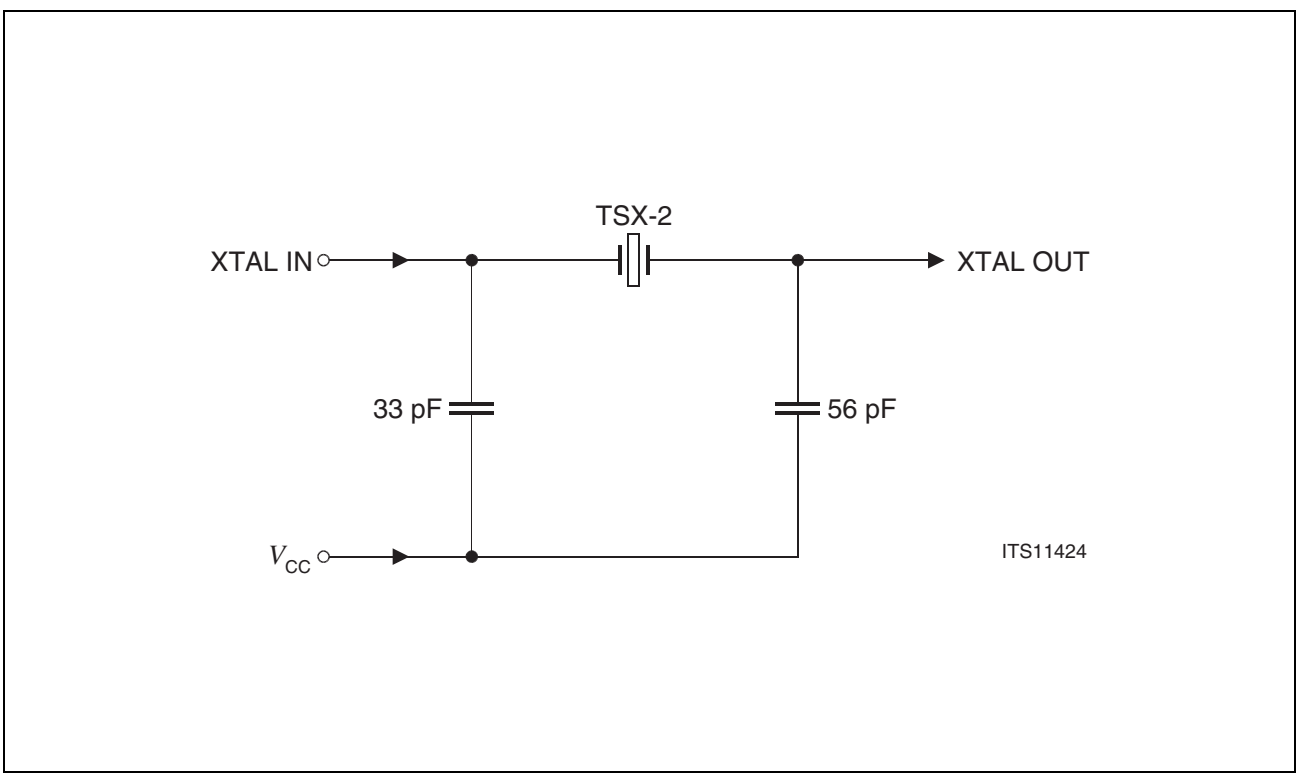


Figure 9 Crystal Oscillator

6 Measurement Results

All measurements were done with 50 mVpp input swing and a 2E23 bit sequence.
Temperature was 25°C, supply voltage was 3.3 V.

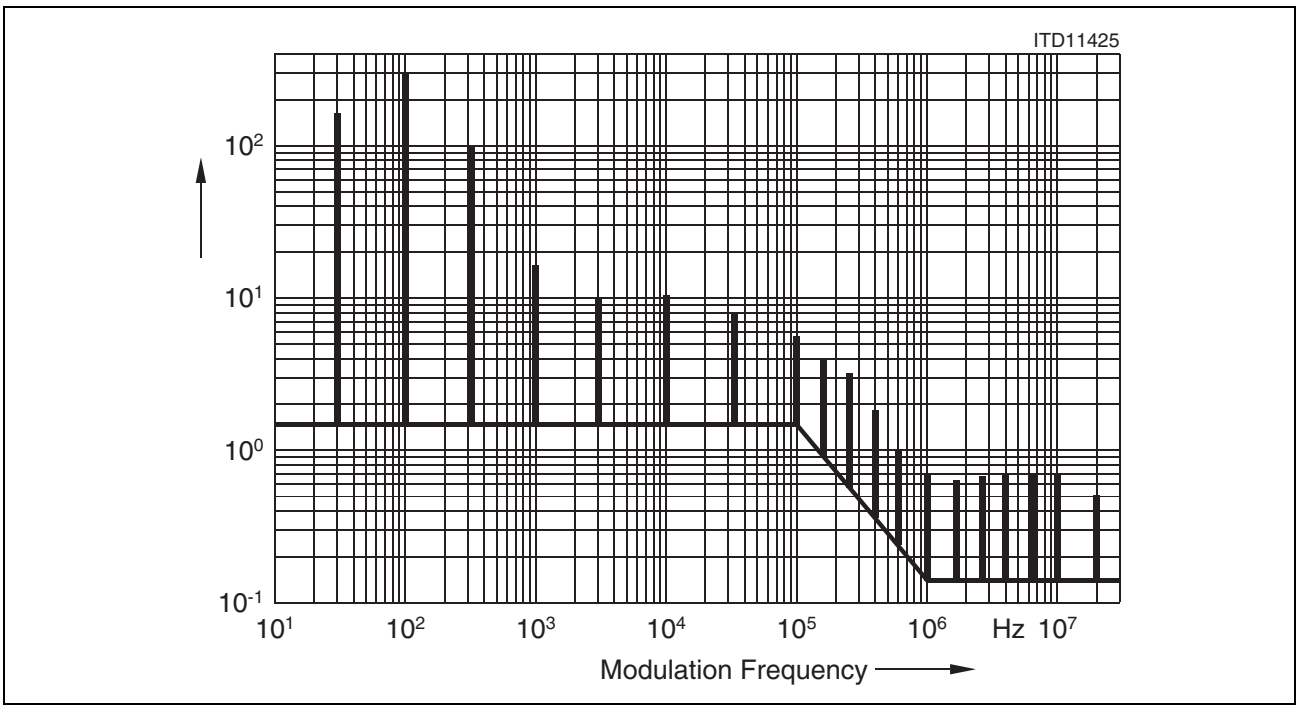


Figure 10 STM 16 Jitter Tolerance

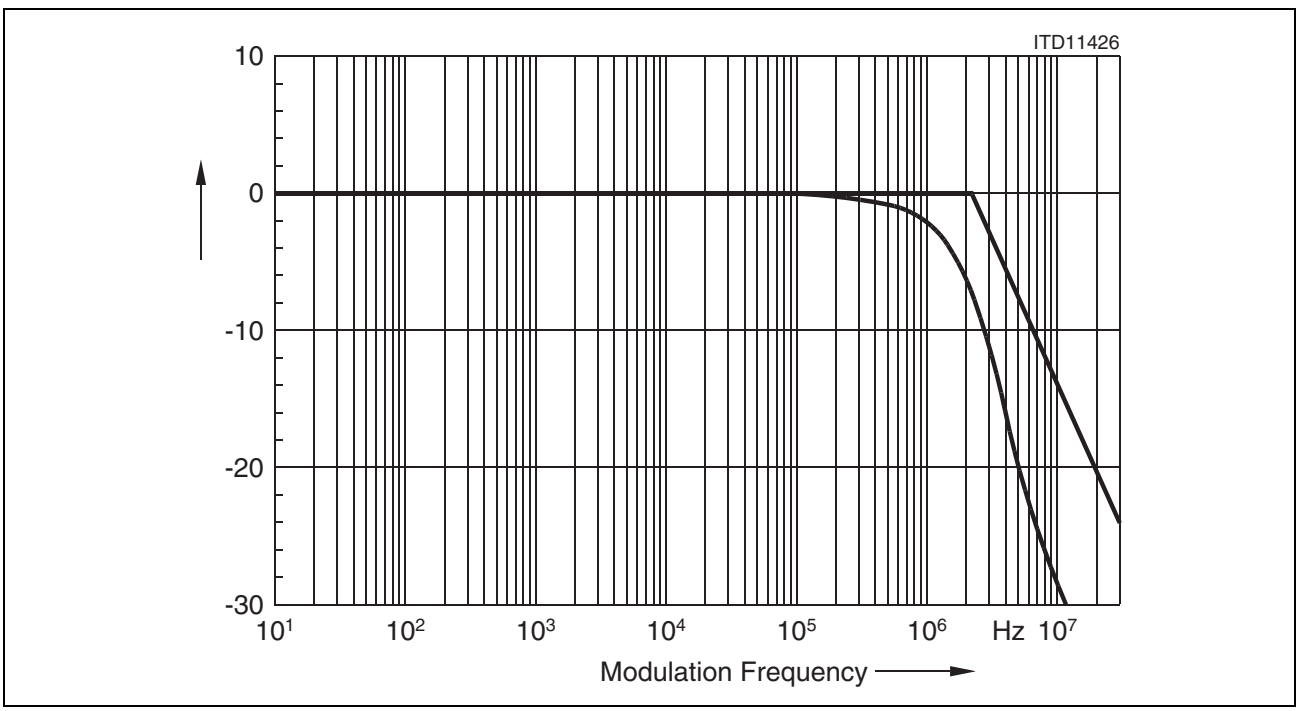
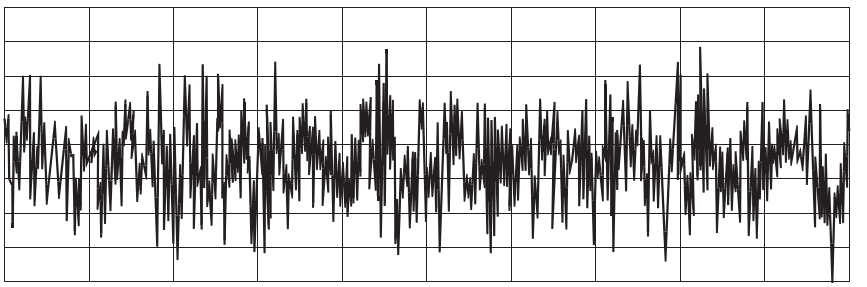


Figure 11 STM 16 Jitter Transfer



Jitter Generation Results

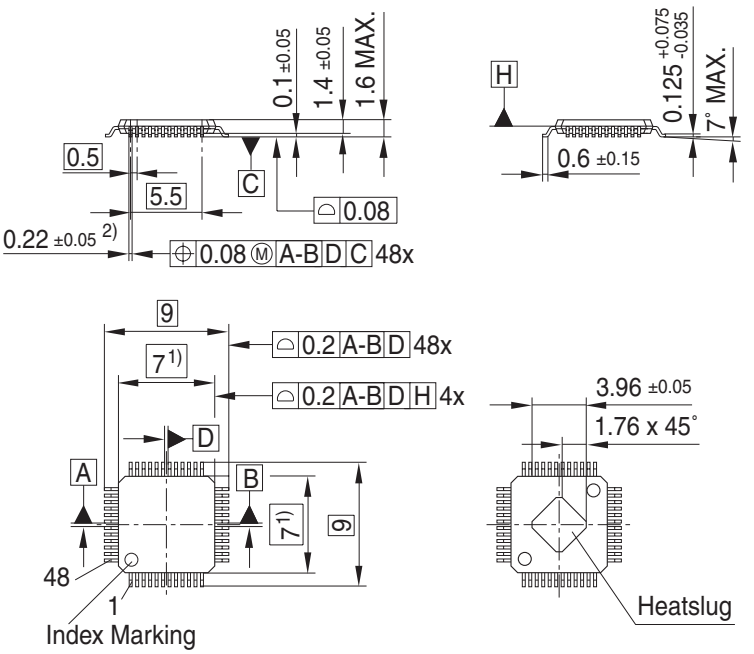
Cutoff Frequency = 12.000 kHz
16.281 mUI p-p
2.516 mUI rms

ITD11427

Figure 12 Gitter Generation Results

7 Package Outlines

P-LQFP-48-1
(Plastic Low Profile Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPP09269

Figure 13

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

Dimensions in mm

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.

Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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Variables Target Specification

Variable Name	Variable Definition	Description
Business Unit	ICs for Communications	
Dev_NameLong1	High Speed Clock and Data Recovery for Fiber Optic Applications	Long product name
Dev_NameLong2		
Dev_NameLong3		
Dev_NameLong4	<Dev_NameLong4>	
Dev_NameShort1	FOA3251B1	Short product name
Dev_NameShort2	<Dev_NameShort2>	
Dev_NameShort3	<Dev_NameShort3>	
Dev_NameShort4	<Dev_NameShort4>	
Dev_Package1	P-LQFP-48-1	Package type
Dev_Package2	<Dev_Package2>	
Dev_Package3	<Dev_Package3>	
Dev_Package4	<Dev_Package4>	
Dev_Version1	<Dev_Version1>	Device version
Dev_Version2	<Dev_Version2>	
Dev_Version3	<Dev_Version3>	
Dev_Version4	<Dev_Version4>	
Device1	FOA3251B1	Marketing/sales name
Device2	<Device2>	
Device3	<Device3>	
Device4	<Device4>	
Doc_Author	<Author>	Author of the document
Doc_ConfidentialStatus		„CONFIDENTIAL“, “PRELIMINARY” or left blank

Variable Name	Variable Definition	Description
Doc_Distribution		"Distribution with NDA" or "Distribution by marketing only" or "Distribution with NDA by marketing only" or left blank
Doc_IssueDate	1999-08	Complete date of releasing the document
Doc_State	V1.0	Revision state of the document
Doc_TopRight1	FOA3251B1	Defines the expression appearing on the top right of the page layout Document type
Doc_TopRight2	S1028C1	
Doc_Type	Data Sheet	Document type
Doc_Type_Cover	Data Sheet	Document type
Modification Date Short		
Status		
Technologie	BIPOLAR	
Title_IssueDate	Aug. 1999	Issue date of the document appearing on the upper right corner of the 1st cover page

Instructions

Defining all variables

1. Double-Click on the Variable Definiton that you want to define.
2. Choose **“Edit Definition”**
3. In the variable dialog box redefine the user variable in the **“Definition”** box. If this variable should not be defined, enter a blank.
4. Click on **“Change”**.
5. Click **“Done”** to return to the variable dialog box.
6. Click **“Done”** again.

Importing the variables into the FrameMaker document/book

1. Make certain that both documents (your FrameMaker file/book and file variables.fm) are open.
2. From the **“File”** menu, click on **“Import”**.
3. Select **“Format”**.
4. From the **“Import from File” (document)** pop-up list, choose **“variables.fm”.**
5. From the **“Import and Update”** box, make sure that *only* the **“Variable Definition”** check box is selected.

Click on **“Import”** to finish.