

Process C0810

CMOS 0.8 μ m

High-Resistance Poly for Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{TN}	0.6	0.8	1.0	V	100x0.8 μ m
Body Factor	γ_N		0.74		$V^{1/2}$	100x0.8 μ m
Conduction Factor	β_N	75	94	115	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{effN}		0.8		μ m	100x0.8 μ m
Width Encroachment	ΔW_N		0.3		μ m	Per side
Punch Through Voltage	$BVDSS_N$	7	13		V	
Poly Field Threshold	$VTF_{P(N)}$	10	17		V	

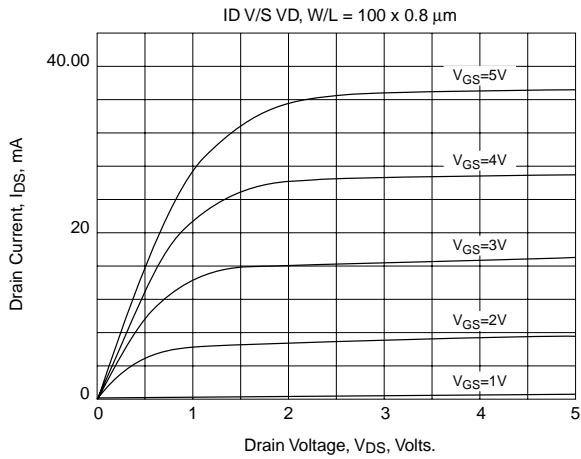
P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{TP}	-0.7	-0.9	-1.1	V	100x0.8 μ m
Body Factor	γ_P		0.57		$V^{1/2}$	100x0.8 μ m
Conduction Factor	β_P	25	31	37	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{effP}		0.85		μ m	100x0.8 μ m
Width Encroachment	ΔW_P		0.4		μ m	Per side
Punch Through Voltage	$BVDSS_P$	-7	-12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-10	-17		V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N-well(f)}$	0.50	0.65	0.80	$K\Omega/\square$	n-well
N+ Sheet Resistance	ρ_{N+}	45	60	75	Ω/\square	
N+ Junction Depth	x_{jN+}		0.25		μ m	
P+ Sheet Resistance	ρ_{P+}	68	90	112	Ω/\square	
P+ Junction Depth	x_{jP+}		0.4		μ m	
Gate Oxide Thickness	T_{GOX}		17.5		nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Bottom Poly Sheet Res.	ρ_{POLY1}	15	23	32	Ω/\square	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	23	32	Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}	40	60	80	$m\Omega/\square$	
Metal-2 Sheet Resistance	ρ_{M2}	20	30	40	$m\Omega/\square$	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.
High Resistance Poly	$\rho_{HI-POLY}$	1.5	2.0	2.5	$K\Omega/\square$	

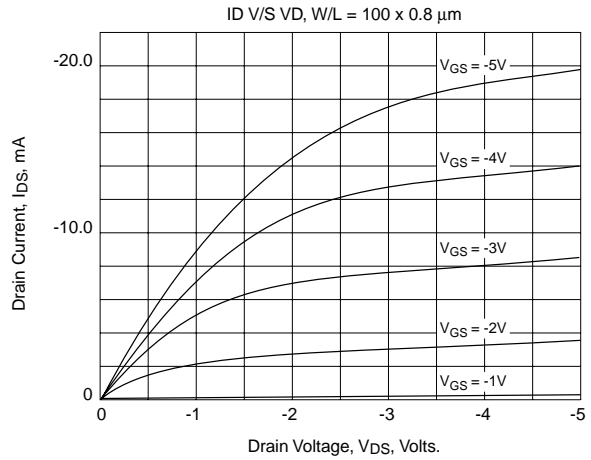
Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.97		fF/ μ m ²	
Metal-1 to Poly1	C_{M1P}		0.046		fF/ μ m ²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/ μ m ²	
Metal-2 to Metal-1	C_{MM}		0.038		fF/ μ m ²	
Poly-1 to Poly-2	C_{PP}	0.69	0.822	1.015	fF/ μ m ²	

Physical Characteristics

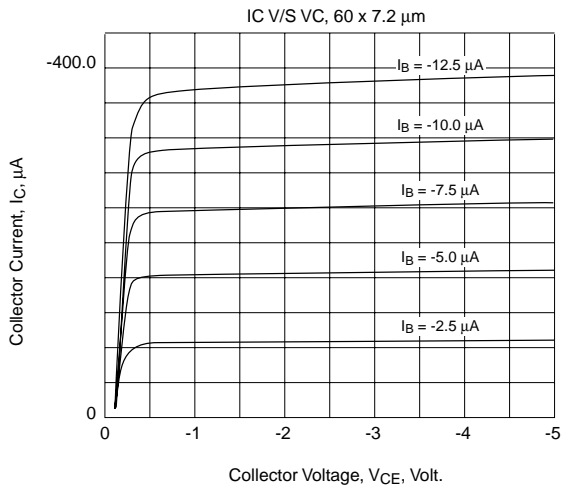
Starting Material	P <100>	N+/P+ Width/Space	1.4 / 1.6 μ m
Starting Mat. Resistivity	25 - 50 Ω -cm	N+ To P+ Space	5.9 μ m
Typ. Operating Voltage	5V	Contact To Poly Space	0.8 μ m
Well Type	N-well	Contact Overlap Of Diffusion	0.7 μ m
Metal Layers	2	Contact Overlap Of Poly	0.7 μ m
Poly Layers	2	Metal-1 Overlap Of Contact	0.7 μ m
Contact Size	0.8x0.8 μ m	Metal-1 Overlap Of Via	0.7 μ m
Via Size	0.8x0.8 μ m	Metal-2 Overlap Of Via	0.7 μ m
Metal-1 Width/Space	1.4 / 1.0 μ m	Minimum Pad Opening	65x65 μ m
Metal-2 Width/Space	1.4 / 1.1 μ m	Minimum Pad-to-Pad Spacing	5.0 μ m
Gate Poly Width/Space	0.8 / 1.0 μ m	Minimum Pad Pitch	80.0 μ m



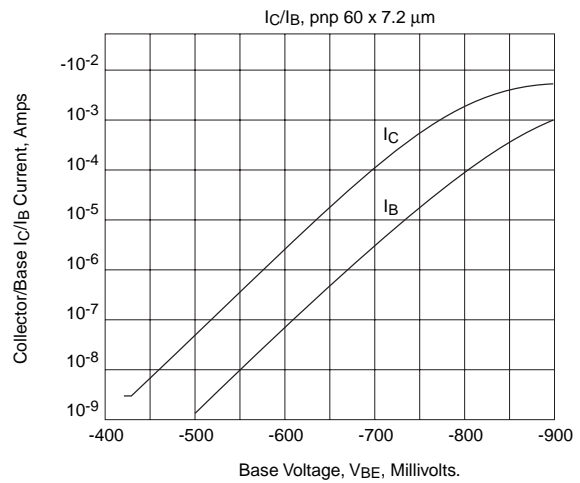
C0810 - n - Channel Transistor Characteristics



C0810 - P - Channel Transistor Characteristics



C0810 Vertical pnp Transistor Characteristics



C0810 Vertical pnp Transistor Characteristics