

**IN74ACT299**

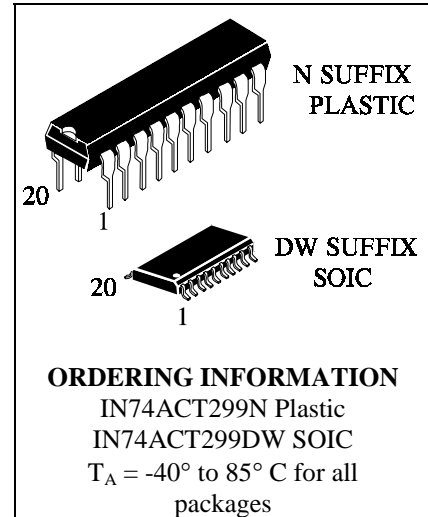
**8-Bit Bidirectional Universal  
Shift Register with Parallel I/O  
High-Speed Silicon-Gate CMOS**

The IN74ACT299 is identical in pinout to the LS/ALS299, HC/HCT299. The IN74ACT299 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT299 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S<sub>1</sub> and S<sub>2</sub>, high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other inputs.

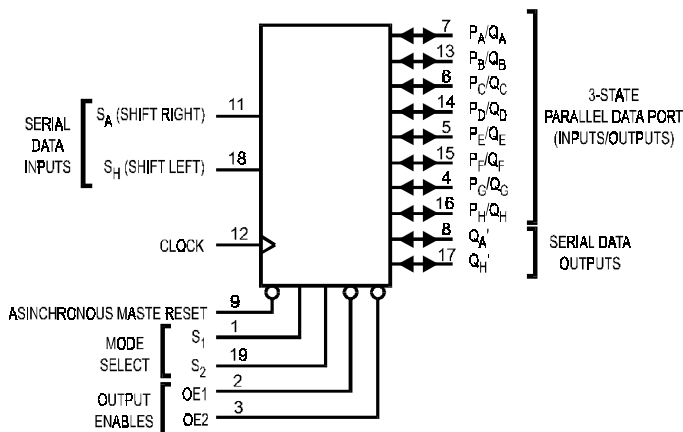
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA; 0.1 μA @ 25°C
- Outputs Source/Sink 24 mA



**PIN ASSIGNMENT**

S1	1 ●	20	V <sub>CC</sub>
OE1	2	19	S2
OE2	3	18	S <sub>H</sub>
P <sub>G</sub> /Q <sub>G</sub>	4	17	Q <sub>H</sub> '
P <sub>E</sub> /Q <sub>E</sub>	5	16	P <sub>H</sub> /Q <sub>H</sub>
P <sub>C</sub> /Q <sub>C</sub>	6	15	P <sub>F</sub> /Q <sub>F</sub>
P <sub>A</sub> /Q <sub>A</sub>	7	14	P <sub>D</sub> /Q <sub>D</sub>
Q <sub>A</sub> '	8	13	P <sub>B</sub> /Q <sub>B</sub>
RESET	9	12	CLOCK
GND	10	11	S <sub>A</sub>

**LOGIC DIAGRAM**



PIN 20 = V<sub>CC</sub>  
 PIN 10 = GND

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Sink/Source Current, per Pin	±50	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>J</sub>	Junction Temperature (PDIP)		140	°C
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
I <sub>OH</sub>	Output Current - High		-24	mA
I <sub>OL</sub>	Output Current - Low		24	mA
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time * (except Schmitt Inputs)	V <sub>CC</sub> =4.5 V V <sub>CC</sub> =5.5 V	0 10 8.0	ns/V

\* V<sub>IN</sub> from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>).  
Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> -0.1 V	4.5 5.5	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> -0.1 V	4.5 5.5	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	I <sub>OUT</sub> ≤ -50 μA	4.5 5.5	4.4 5.4	4.4 5.4	V
		*V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> =-24 mA	4.5	3.86	3.76	
		I <sub>OH</sub> =-24 mA	5.5	4.86	4.76	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	I <sub>OUT</sub> ≤ 50 μA	4.5 5.5	0.1 0.1	0.1 0.1	V
		*V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> =24 mA	4.5	0.36	0.44	
		I <sub>OL</sub> =24 mA	5.5	0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	±0.1	±1.0	μA
ΔI <sub>CCCT</sub>	Additional Max. I <sub>CC</sub> /Input	V <sub>IN</sub> =V <sub>CC</sub> - 2.1 V	5.5		1.5	mA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	V <sub>IN</sub> (OE)= V <sub>IH</sub> or V <sub>IL</sub> V <sub>IN</sub> =V <sub>CC</sub> or GND V <sub>OUT</sub> =V <sub>CC</sub> or GND	5.5	±0.6	±6.0	μA
I <sub>OLD</sub>	+Minimum Dynamic Output Current	V <sub>OLD</sub> =1.65 V Max	5.5		75	mA
I <sub>OHD</sub>	+Minimum Dynamic Output Current	V <sub>OHD</sub> =3.85 V Min	5.5		-75	mA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	8.0	80	μA

\* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

**AC ELECTRICAL CHARACTERISTICS**( $V_{CC}=5.0\text{ V} \pm 10\%$ ,  $C_L=50\text{pF}$ , Input  $t_r=t_f=3.0\text{ ns}$ )








Symbol	Parameter	Guaranteed Limits				Unit
		25 °C		-40°C to 85°C		
		Min	Max	Min	Max	
$f_{\max}$	Maximum Clock Frequency (Figure 1)	120		110		MHz
$t_{PLH}$	Propagation Delay, Clock to $Q_A'$ or $Q_H'$ (Figure 1)	4.0	12.5	3.0	14.0	ns
$t_{PHL}$	Propagation Delay, Clock to $Q_A'$ or $Q_H'$ (Figure 1)	4.0	13.5	3.5	15.0	ns
$t_{PLH}$	Propagation Delay, Clock to $Q_A$ thru $Q_H$ (Figure 1)	4.5	12.5	4.5	13.5	ns
$t_{PHL}$	Propagation Delay, Clock to $Q_A$ thru $Q_H$ (Figure 1)	5.0	15.0	4.5	16.5	ns
$t_{PHL}$	Propagation Delay, Reset to $Q_A'$ or $Q_H'$ (Figure 2)	4.0	15.0	4.0	18.0	ns
$t_{PHL}$	Propagation Delay, Reset to $Q_A$ thru $Q_H$ (Figure 2)	4.0	14.5	3.5	17.5	ns
$t_{PZH}$	Propagation Delay , OE1, OE2 to $Q_A$ thru $Q_H$ (Figure 3)	2.5	12.0	1.5	13.0	ns
$t_{PZL}$	Propagation Delay , OE1, OE2 to $Q_A$ thru $Q_H$ (Figure 3)	2.0	12.0	1.5	13.5	ns
$t_{PHZ}$	Propagation Delay , OE1, OE2 to $Q_A$ thru $Q_H$ (Figure 3)	2.0	12.5	2.0	13.5	ns
$t_{PLZ}$	Propagation Delay , OE1, OE2 to $Q_A$ thru $Q_H$ (Figure 3)	2.5	11.5	2.0	12.5	ns
$C_{IN}$	Maximum Input Capacitance	4.5		4.5		pF

$C_{PD}$	Power Dissipation Capacitance	Typical @25°C, $V_{CC}=5.0\text{ V}$		pF
		170		

**TIMING REQUIREMENTS**( $V_{CC}=5.0\text{ V} \pm 10\%$ ,  $C_L=50\text{pF}$ , Input  $t_r=t_f=3.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limits		Unit
		25 °C	-40°C to 85°C	
$t_{su}$	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	5.0	5.5	ns
$t_{su}$	Minimum Setup Time, Data Inputs $P_A$ thru $P_H$ to Clock (Figure 4)	4.0	4.5	ns
$t_{su}$	Minimum Setup Time, Data Inputs $S_A$ , $S_H$ to Clock (Figure 4)	4.5	5.0	ns
$t_h$	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	1.0	1.0	ns
$t_h$	Minimum Hold Time, Clock to Data Inputs $P_A$ thru $P_H$ (Figure 4)	1.0	1.0	ns
$t_h$	Minimum Hold Time, Clock to Data Inputs $S_A$ , $S_H$ (Figure 4)	1.0	1.0	ns
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	1.5	1.5	ns
$t_w$	Minimum Pulse Width, Clock (Figure 1)	4.0	4.5	ns
$t_w$	Minimum Pulse Width, Reset (Figure 2)	3.5	3.5	ns

FUNCTION TABLE

Inputs									Response									
Mode	Reset	Mode Select		Output Enables		Clock	Serial Inputs		P <sub>A</sub> / Q <sub>A</sub>	P <sub>B</sub> / Q <sub>B</sub>	P <sub>C</sub> / Q <sub>C</sub>	P <sub>D</sub> / Q <sub>D</sub>	P <sub>E</sub> / Q <sub>E</sub>	P <sub>F</sub> / Q <sub>F</sub>	P <sub>G</sub> / Q <sub>G</sub>	P <sub>H</sub> / Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
		S <sub>2</sub>	S <sub>1</sub>	OE1↑	OE2↑		D <sub>A</sub>	D <sub>H</sub>										
Reset	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	Q <sub>A</sub> through Q <sub>H</sub> =Z							L	L	
Shift Right	H	L	H	H	X		D	X	Shift Right: Q <sub>A</sub> through Q <sub>H</sub> =Z; D <sub>A</sub> →F <sub>A</sub> ; F <sub>A</sub> →F <sub>B</sub> ; etc							D	Q <sub>G</sub>	
	H	L	H	X	H		D	X	Shift Right: Q <sub>A</sub> through Q <sub>H</sub> =Z; D <sub>A</sub> →F <sub>A</sub> ; F <sub>A</sub> →F <sub>B</sub> ; etc							D	Q <sub>G</sub>	
	H	L	H	L	L		D	X	Shift Right: D <sub>A</sub> →F <sub>A</sub> =Q <sub>A</sub> ; F <sub>A</sub> →F <sub>B</sub> =Q <sub>B</sub> ; etc							D	Q <sub>G</sub>	
Shift Left	H	H	L	H	X		X	D	Shift Left: Q <sub>A</sub> through Q <sub>H</sub> =Z; D <sub>H</sub> →F <sub>H</sub> ; F <sub>H</sub> →F <sub>G</sub> ; etc							Q <sub>B</sub>	D	
	H	H	L	X	H		X	D	Shift Left: Q <sub>A</sub> through Q <sub>H</sub> =Z; D <sub>H</sub> →F <sub>H</sub> ; F <sub>H</sub> →F <sub>G</sub> ; etc							Q <sub>B</sub>	D	
	H	H	L	L	L		X	D	Shift Left: D <sub>H</sub> →F <sub>H</sub> =Q <sub>H</sub> ; F <sub>H</sub> →F <sub>G</sub> =Q <sub>G</sub> ; etc							Q <sub>B</sub>	D	
Parallel Load	H	H	H	X	X		X	X	Parallel Load: P <sub>N</sub> →F <sub>N</sub>							P <sub>A</sub>	P <sub>H</sub>	
Hold	H	L	L	H	X	X	X	X	Hold: Q <sub>A</sub> through Q <sub>H</sub> =Z; F <sub>N</sub> =F <sub>N</sub>							P <sub>A</sub>	P <sub>H</sub>	
	H	L	L	X	H	X	X	X	Hold: Q <sub>A</sub> through Q <sub>H</sub> =Z; F <sub>N</sub> =F <sub>N</sub>							P <sub>A</sub>	P <sub>H</sub>	
	H	L	L	L	L	X	X	X	Hold: Q <sub>N</sub> =Q <sub>H</sub>							P <sub>A</sub>	P <sub>H</sub>	

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

↑ When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

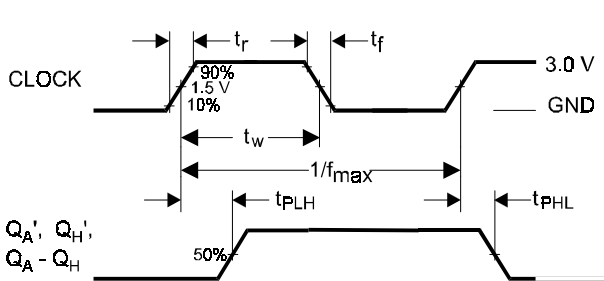


Figure 1. Switching Waveform

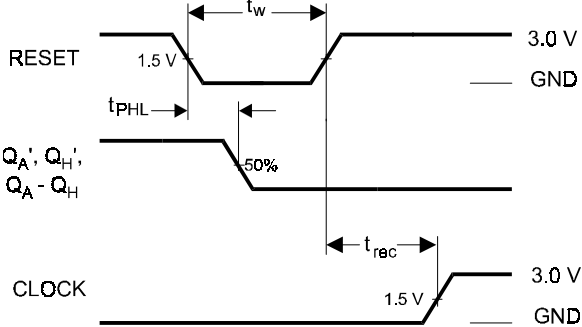


Figure 2. Switching Waveform

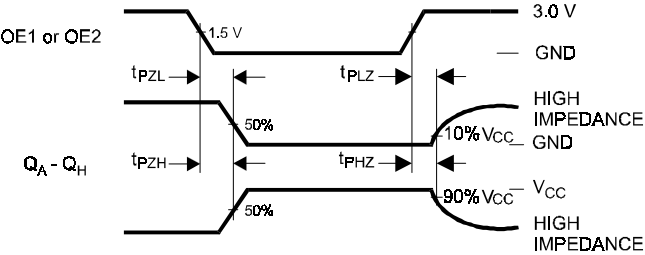


Figure 3. Switching Waveform

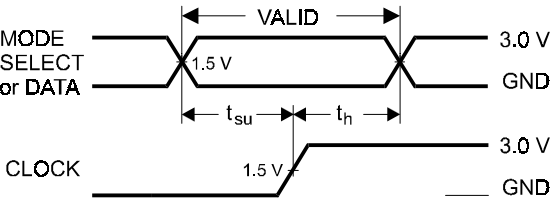


Figure 4. Switching Waveform

EXPANDED LOGIC DIAGRAM

