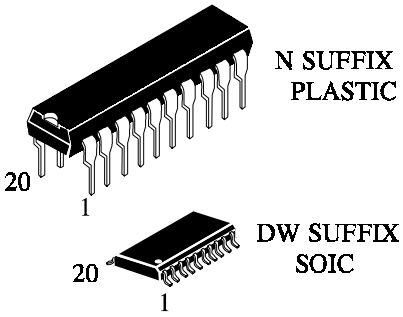
IN472-3

Liquid Crystal Display Controller

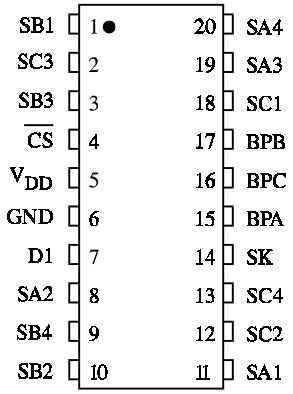


ORDERING INFORMATION
IN472-3N Plastic
IN472-3DW SOIC
T_A = 0° to 70° C
for all packages

The IN472-3-3 Liquid Crystal Display (LDC) Controller is a perpheral member of the COPS™ family, fabricated using CMOS technology. The IN472-3 drives a multiplexed liquid crystal directly. Data is loaded serially and is held in internal latches. The In472-3 contains an on-chip oscillator and generates all the multi-level waveforms for back-planes and segment outputs on a triplex display. One IN472-3 can drive 36 segments multiplexed as 3 x 12 ($4^1/_2$ digit display). Two IN472-3 devices can be used together to drive 72 segments (3 x 24) which could be an $8^1/_2$ digit display.

- Direct interface to TRIPLEX LCD
- Low power dissipation (100 µW typ.)
- Low cost
- Compatible with all COP400 processors
- Needs no refresh from processor
- On-chip oscillator and latches
- Expandable to longer displays
- Software compatible with COP470 V.F.Display Driver Chip
- Operates from display voltage
- MICROWIRE™ compatible serial I/O
- 20-pin Dual-In-Line package

PIN ASSIGNMENT



Pin Description

Pin	Description
CS	Chip select
V_{DD}	Power supply (display voltage)
GND	Ground
DI	Serial data input
SK	Serial clock input
BP_A	Display backplane A (or oscillator in)
BP_B	Display backplane B
BP_C	Display backplane C (or oscillator out)
SA1~SA4	12 multiplexed outputs

DC ELECTRICAL CHARACTERISTICS (GND=0 V, V_{DD}=3.0 V to 5.5 V, T_A= 0°C to 70°C (depends on display characteristics)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V_{DD}	Power Supply Voltage		3.0	5.5	V
I_{DD}	Power Supply Current (Note 1)	V_{DD} =5.5 V		250	µA
V_{IL}	Input Levels DI, SK, CS			0.8	V
V_{IH}			0.7 V_{DD}	V_{DD}	
V_{IL}	BPA (as Osc. in)			0.6	V
V_{IH}			V_{DD}-0.6	V_{DD}	
V_{OL}	Output Levels, BPC (as Osc. Out)			0.4	V
V_{OH}			V_{DD}-0.4	V_{DD}	
$V_{BPA,BPB,BPC}$ ON	Backplane Outputs (BPA,BPB,BPC)	During BP + Time	V_{DD} -ΔV	V_{DD}	V
$V_{BPA,BPB,BPC}$ OFF			1/3V_{DD} -ΔV	1/3V_{DD} +ΔV	
$V_{BPA,BPB,BPC}$ ON	Backplane Outputs (BPA,BPB,BPC)	During BP - Time	0	ΔV	V
$V_{BPA,BPB,BPC}$ OFF			2/3V_{DD} -ΔV	2/3V_{DD} +ΔV	
V_{SEG} ON	Segment Outputs (SA_1 ~ SA_4)	During BP + Time	0	ΔV	V
V_{SEG} OFF			2/3V_{DD} -ΔV	2/3V_{DD} +ΔV	
V_{SEG} ON	Segment Outputs (SA_1 ~ SA_4)	During BP - Time	V_{DD} -ΔV	V_{DD}	V
V_{SEG} OFF			1/3V_{DD} -ΔV	1/3V_{DD} +ΔV	
	Internal Oscillator Frequency		15	80	kHz
	Frame Time (Int. Osc. ÷ 192)		2.4	12.8	ms
$1/T_{SCAN}$	Scan Frequency		39	208	Hz
	SK Clock Frequency		4	250	kHz
	SK Width		1.7		µs
t_{SETUP}	DI Data Stup		1.0		µs
t_{HOLD}	DI Data Hold		100		ns
t_{SETUP}	$\overline{CS}$		1.0		µs
t_{HOLD}			1.0		
	Output Loading Capacitance			100	pF

Note 1: Power supply current as measured in stand-alone mode with all outputs open and all inputs at V_{DD}.

Note 2: ΔV - 0.05V_{DD}.

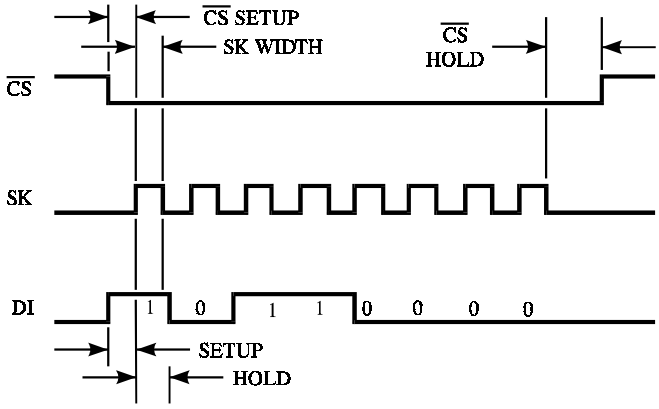


Figure 1. Serial Load Timing Diagram

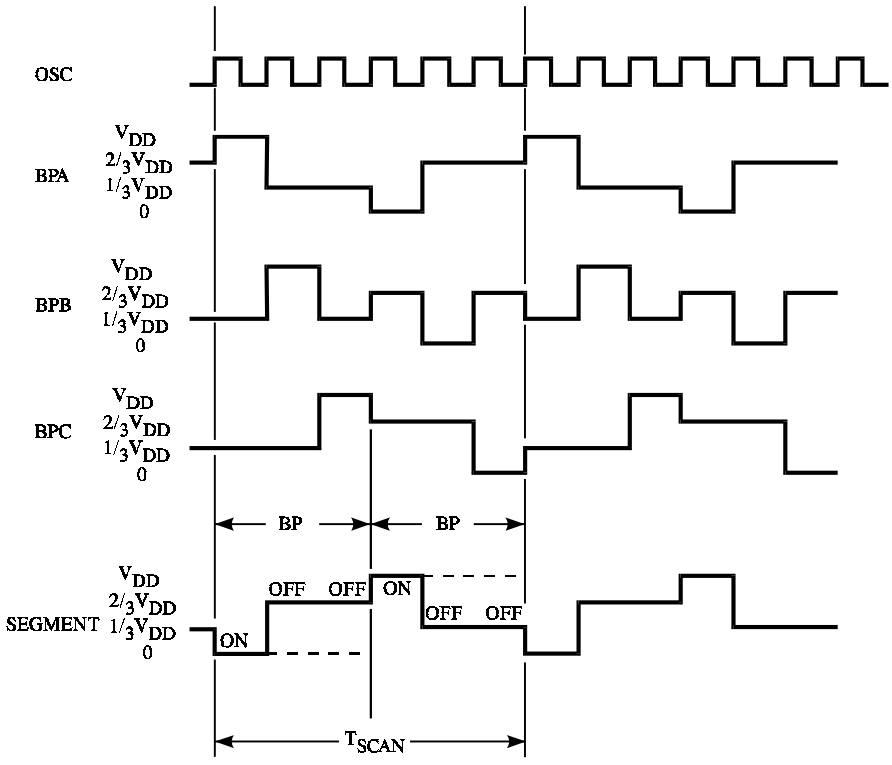


Figure 2. Backplane and Segment Waveforms