

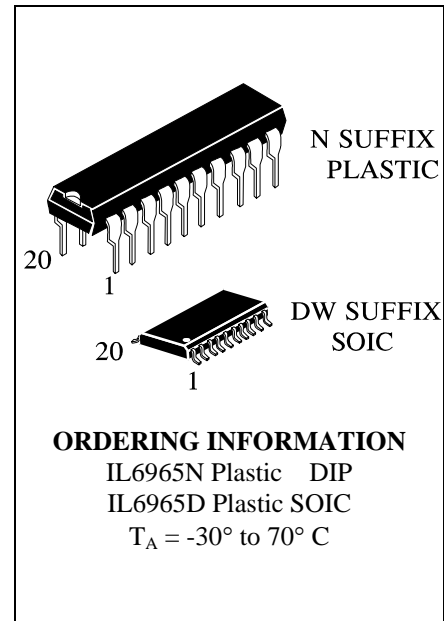
**IL6965**

# Telephone Speech Network with Dialer Interface

The IL6965 is a bipolar integrated circuit for use in electronic telephones.

The IL6965 has low operating voltage, it provides an excellent branch performance.

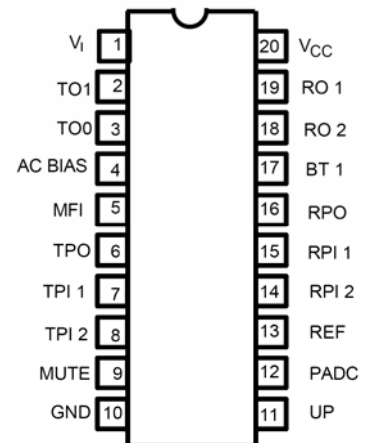
It has line voltage increasing circuit by the external terminal. Transmitting and receiving gains automatically vary according to the line current.



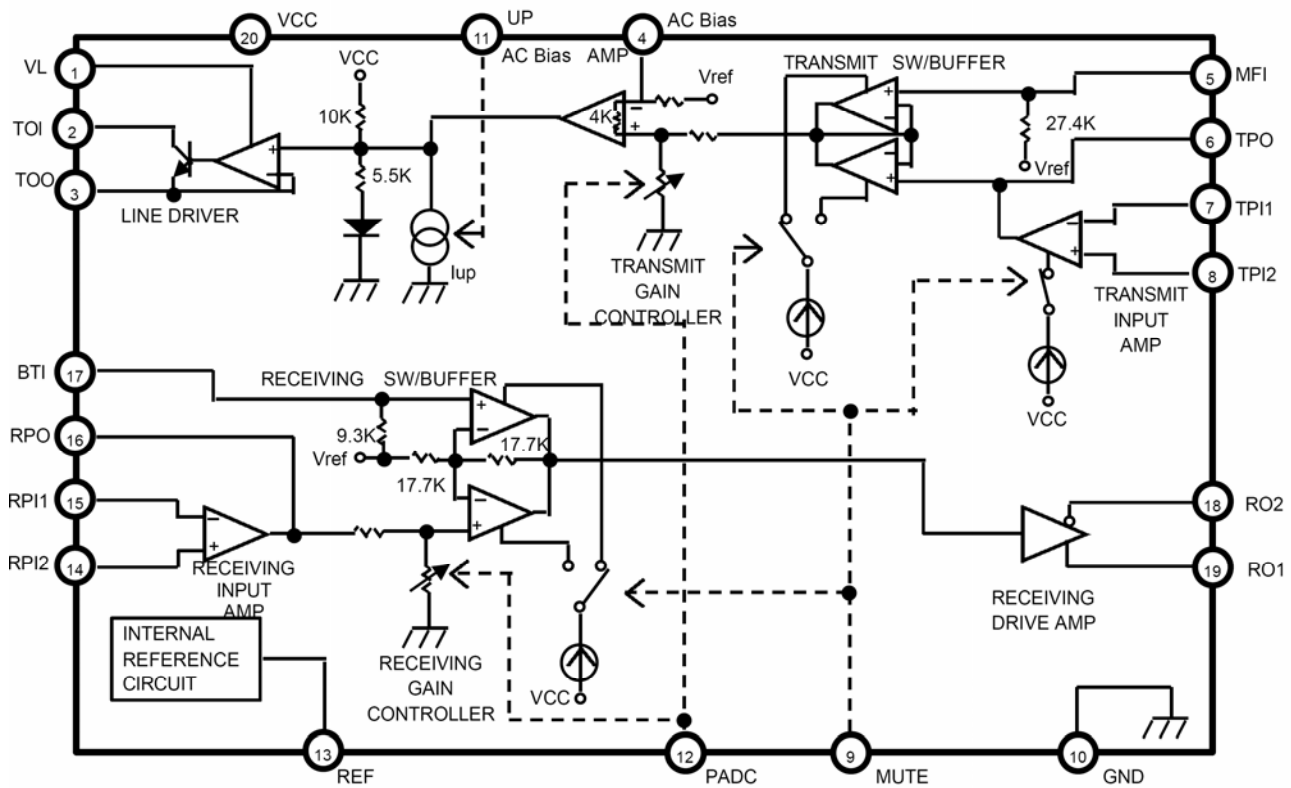
## FEATURES

- Externally adjustable transmitting, receiving and sidetone gains.
- Switching between transmitting output and DTMF output is possible.
- Direct interface with light and compact ceramic transmitter-receiver is possible.
- Receiver follow impedance type can also be used.
- Gain is automatically controlled according to the line current. (Auto-PAD function)
- The line voltage can be increased by the external terminal (Up function).
- PKG is 20pin DIP & SOP

## PIN ASSIGNMENT



**BLOCK DIAGRAM**



**Absolute Maximum Ratings (Ta = 25°C)**

Parameter	Symbol	Value	Unit
Line Voltage	$V_L$	15	V
Line Current	$I_L$	150	mA
Power Dissipation	$P_D$	1300	mW
Operating Temperature	$T_{opr}$	-30 ~ 70	°C
Storage Temperature	$T_{stg}$	-55 ~ 150	°C

**Electrical Characteristics (Ta = 25°C)**

Parameter	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Line Voltage	$V_L$	1	IL=20mA	2.9	3.2	3.6	V
			IL=120mA	9	11	14	V
Internal Power Supply Voltage	$V_{CC}$	1	IL=20mA	1.75	1.90	2.20	V
			IL=120mA	5.8	6.1	6.6	V

Parameter	Sym-bol	Test Circuit	Test Conditon	Min.,	Typ.	Max.	Unit	
Line Voltage Rise up Amount	$\Delta V_L$	2	IL=20mA	1.1	1.5	2.1	V	
Transmit Gain	$G_T$	4	IL=20mA	$f = 1\text{KHz}$ $V_{in} = -55\text{dBV}$	43	46	48	dB
			IL=120mA		40	43.2	45	dB
Receiving Gain	$G_R$	5	IL=20mA	$f = 1\text{KHz}$ $V_{in} = -55\text{dBV}$	40	43.5	46	dB
			IL=120mA		34.5	38	40.5	dB
MF Gain	$G_{MF}$	6	IL=20mA	$f = 1\text{KHz}$ $V_{in} = -30\text{dBV}$	24	26.8	28	dB
			IL=120mA		21.5	24	25.5	dB
Beep Gain	$G_{BP}$	8	IL=20mA	$f = 1\text{KHz}$ $V_{in} = -30\text{dBV}$	21	24	27	dB
			IL=120mA		21.5	24.5	27.5	dB
Transmit Dynamic Range	$D_{RT}$	4	IL=20mA	Distortion Ratio 4%	2.0	—	—	$V_{p,p}$
			IL=120mA		4.0	—	—	$V_{p,p}$
Receiving Dynamic Range	$D_{RR}$	5	IL=20mA	Distortion Ratio 10%	3.0	—	—	$V_{p,p}$
			IL=120mA		6.0	—	—	$V_{p,p}$
MFI Input Resistance	ZI(MF)	—		21	30	—	k $\Omega$	
BTI Input Resistance	ZI(BP)	—		7	10	—	k $\Omega$	
AC BIAS Input Resistance	ZI(AB)	—		21	30	—	k $\Omega$	
MUTE Terminal High Level Input Voltage	$V_{IH}(MU)$	—	IL=20mA-120mA	$V_{CC} - 0.5$	—	$V_{CC}$	V	
MUTE Terminal Low Level Input Voltage	$V_{IL}(MU)$	—	IL=20mA-120mA	0	—	0.2	V	

**Reference data**

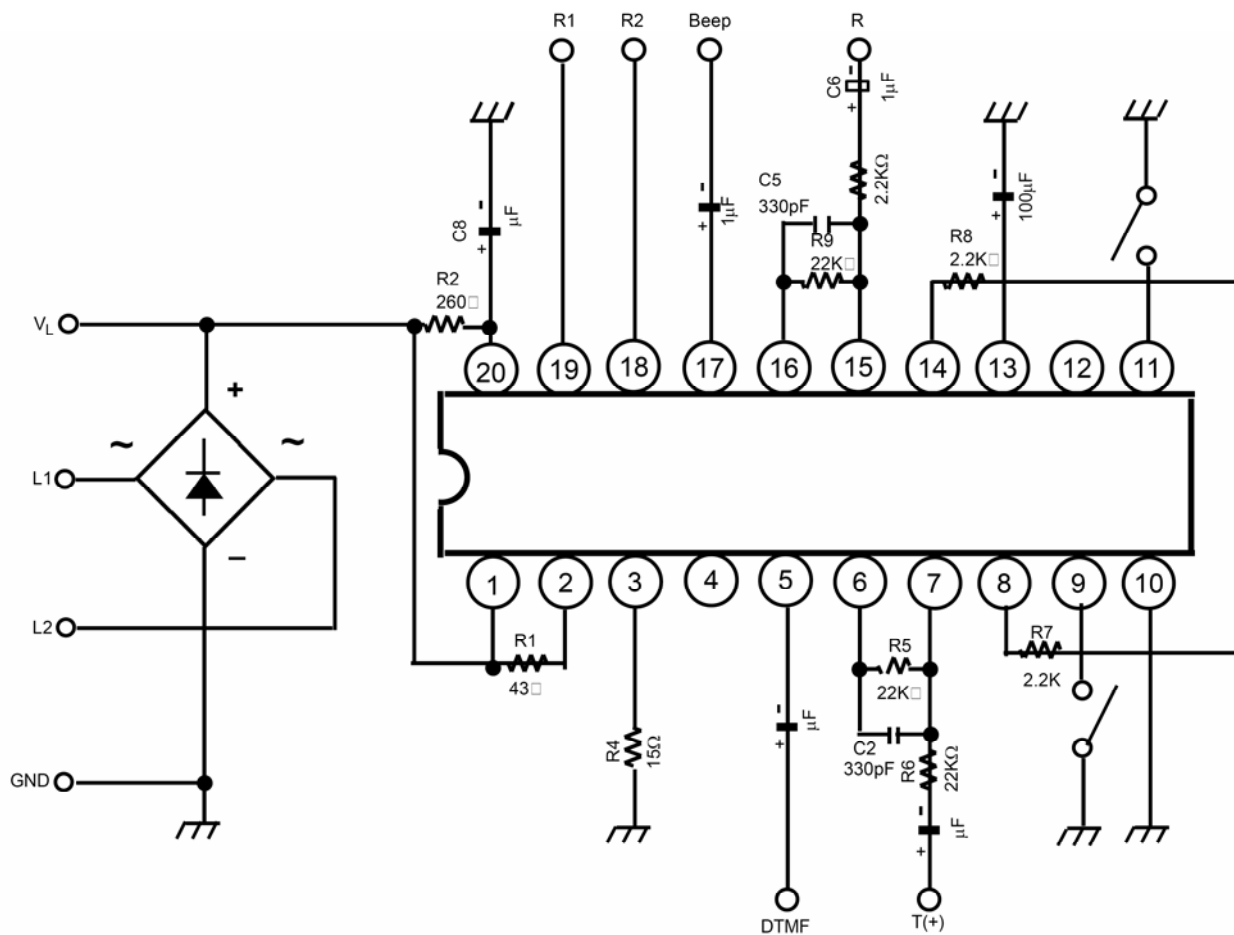
Parameter	Symbol	Test Circuit	Test Condition	Typ	Unit	
Internal Reference Voltage	$V_{REF}$	3	IL=20mA	0.66	V	
			IL=120mA	2.8	V	
RO1, RO2 Output Impedance	$Z_{RO}$	—	IL=30mA $f=1\text{KHz}$	200	$\square$	
Total Receiving Gain	$G_R$ (Total)	11	IL=20mA	(Balancing Network circuit included.)	14.5	dB
			IL=120mA		9.0	dB
MUTE Terminal Input Current	$I_{IL}(MU)$	9	IL=20mA $V_{IL}=0.2\text{V}$	-50	$\mu\text{A}$	
UP Terminal Input Current	$I_{IL}(MP)$	10	IL=20mA at GND connection	-35	$\mu\text{A}$	
AC Impedance	Z TEL	—	IL=50mA $f=1\text{KHz}$	580	$\square$	
Phase	$\theta$	—	IL=50mA $f=1\text{KHz}$	3	DEG	

## Pin Descriptions

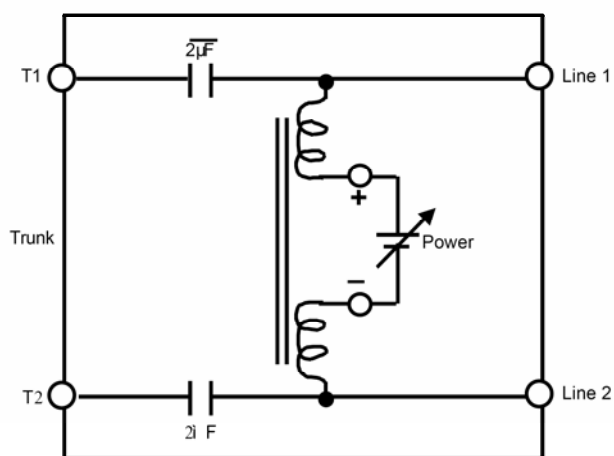
Pin No.	Symbol	Function	Explanation
1	VL	Line Current flow-in and Line Voltage terminal	Connected to positive output of diode bridge circuit. DC potential of this terminal determines line voltage and if AC signal is not input, the highest DC potential appears. Transmit output signal and output signal of opposite transfer side are intermingled and output at this terminal in actual use.
2	TOI	Current flow-in terminal of transmit output	Connected to VL terminal (① pin) through $43\ \Omega$ . Since almost all the line currents flow in from this terminal, set allowable power of resistance $43\ \Omega$ to be connected to VL terminal from this terminal considering the maximum line current expected to be used.
3	TOO	Current output terminal of transmit output	Connected to GND terminal (⑩ pin) through $15\ \Omega$ . Since almost all the line currents flow out from this terminal, set allowable power of resistance $15\ \Omega$ to be connected to GND terminal from this terminal considering the maximum line current expected to be used. Transmit signal is sent from this terminal. Signal of this terminal varies current which is input from line through connected resistance $15\ \Omega$ , and makes it be output at VL terminal (① pin)
4	AC Bias	AC signal reference Voltage terminal	When AC signal is input to this terminal through capacitor (for blocking DC), signal is sent to line, Input from this terminal is output to line without any relation to gain control (PAD) or MUTE since this input does not pass through gain control circuit or MUTE function
5	MFI	Input terminal of DTMF or external input signal	Signal which is input to this terminal is output at VL terminal (① pin) only when MUTE terminal (⑨ pin) is in "L" state. Since this terminal is biased to almost the same potential as REF terminal (⑬ pin), avoid direct impressing external DC potential by using capacitor at inputting external terminal.
6	TPO	Output terminal of transmit input Amp.	Makes negative feedback to TPI1 terminal (⑦ pin)
7	TPI1	Inversion input terminal of transmit input Amp.	Receives negative feedback from TPO terminal (⑥ pin)
8	TPI2	Non-inversion input terminal of transmit input Amp.	Applies DC bias to this terminal from REF terminal (⑬ pin) through resistance

Pin No.	Symbol	Function	Explanation
9	MUTE	MUTE terminal	Switching terminal of transmit signal with MFI input signal in transmitting system. Switching terminal of receiving signal with BTI input signal in receiving system. “L” State—Signal which is input from MFI is output to VL terminal (① pin) Signal which is input from BTI is output to terminals RO1 and RO2. “H” or “OPEN” state Transmitting input signal is output to VL terminal (① pin). Receiving input signal is output to terminals RO1 and RO2 (⑨ pin (⑩ pin)) This terminal is pulled up by constant-current circuit
10	GND	Ground terminal	Connected to negative output of diode bridge circuit.
11	UP	DC impedance control terminal	When this terminal is connected to GND terminal (⑩ pin) directly or through resistance. DC potential of VL terminal (① pin) can be in-creased up to max. 1.5V (TYP.) in the same line current. This function has no relation to the state of MUTE terminal.
12	PADC	Pad control terminal	When this terminal is connected to GND terminal (⑩ pin) or V <sub>CC</sub> terminal (⑳ pin) through resistance, operation current of gain control (Auto-PAD) performed by line current can be controlled.
13	REF	Internal reference voltage Output terminal	Voltage of this terminal is used as a reference voltage of internal amplifiers. Never used this terminal for an external power supply.
14	RPI2	Non-inversion input terminal of receiving Input Amp.	Apply DC bias to this terminal from REF terminal (⑬ pin) through resistance.
15	RPI1	Inversion Input terminal of receiving input Amp.	Receives negative feedback from RPO terminal (⑯ pin).
16	RPO	Output terminal of Receiving input Amp.	Makes negative feedback to RPI1 terminal (⑮ pin).
17	BTI	Dial confirmation sound (Beep Tone, DTMF), monitor sound input terminal	Signal which is input to this terminal is output to terminals RO1 and RO2 (⑰ pin and ⑱ pin) only when MUTE terminal (⑨ pin) is in “L” state. Since this terminal is biased to about the same potential as REF terminal (③ pin), avoid direct impressing external DC voltage through capacitor at in-putting external signal
18	RO2	Receiving output terminal Inversion output	Output terminal to receiver. Signal of which phase is negative to RO1 terminal (⑰ pin), is output.
19	RO1	Receiving output terminal Non-inversion output	Output terminal to receiver, Signal of which phase is negative to RO2 terminal (⑱ pin), is output
20	V <sub>CC</sub>	Internal power supply voltage terminal	Power supply of internal amplifiers

Test Circuit

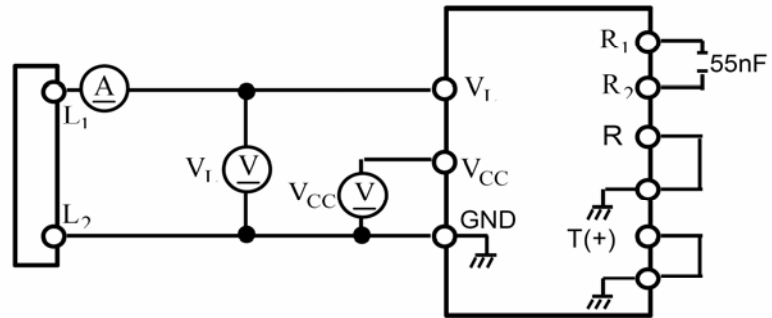


Telephone line Simulation Equivalent circuit

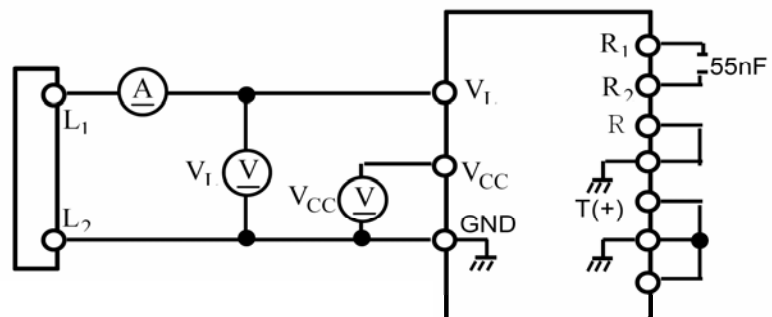


Test Circuit (continued)

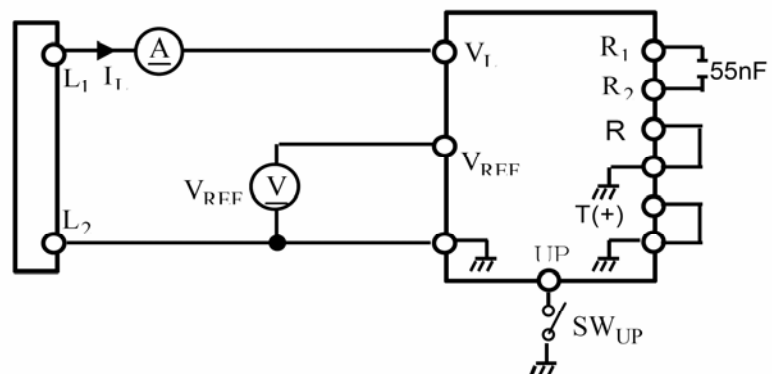
1.  $V_L, V_{CC}$



2.  $V_L, V_{CC}$  (UP)

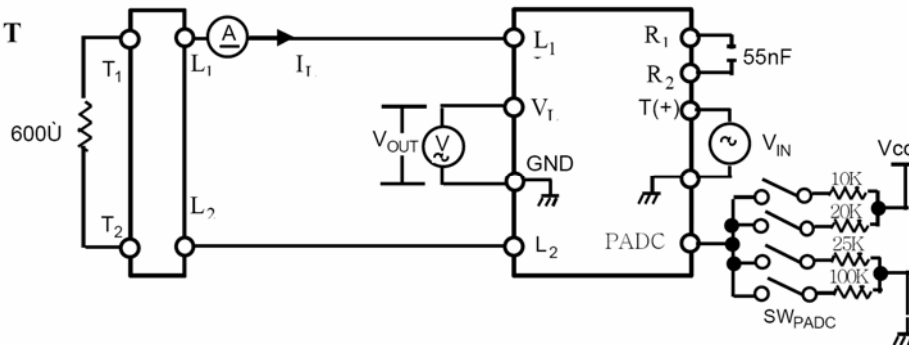


3.  $V_{REF}$



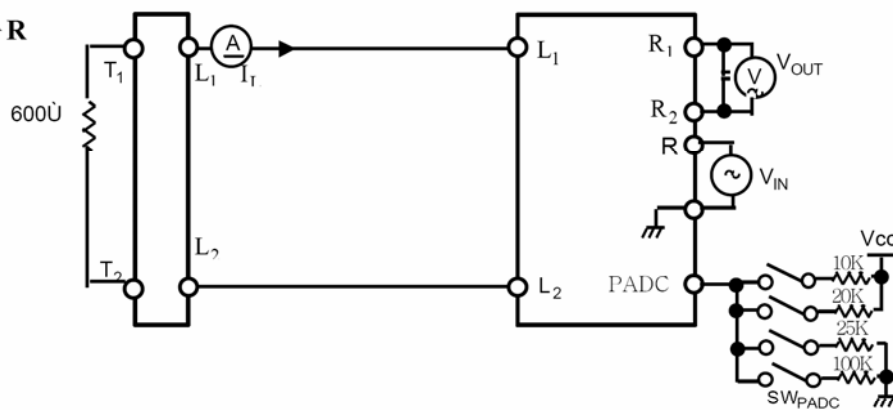
Test Circuit (continued)

4.  $G_T, DR_T$



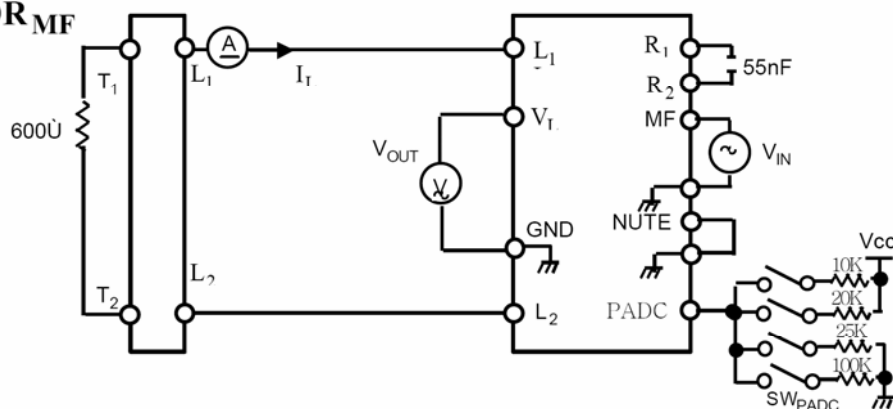
- Transmit Gain,  $G_T = 20 \log |V_{OUT} / V_{IN}|$  (dB)
- Transmit Dynamic Range:  $DR_T = V_{OUT}$  (Vp-p) at  $V_{OUT} : DIST = 4\%$

5.  $G_R, DR_R$



- Receiving Gain,  $G_R = 20 \log |V_{OUT} / V_{IN}|$  (dB)
- Receiving Dynamic Range:  $DR_R = V_{OUT}$  (Vp-p) at  $V_{OUT} : DIST = 10\%$

6.  $G_{MF}, DR_{MF}$

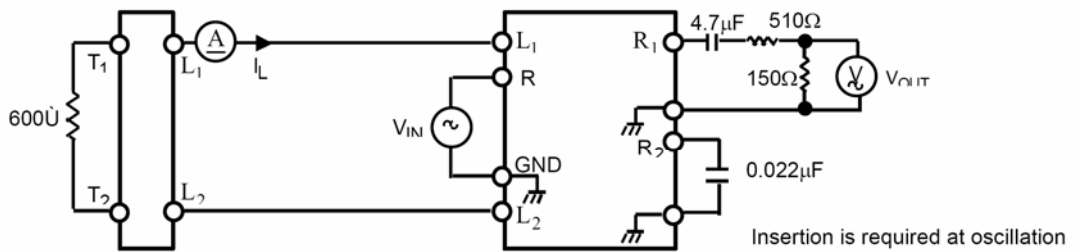


- MF Gain,  $G_{MF} = 20 \log |V_{OUT} / V_{IN}|$  (dB)
- MF Dynamic Range:  $DR_{MF} = V_{OUT}$  (Vp-p) at  $V_{OUT} : DIST = 4\%$



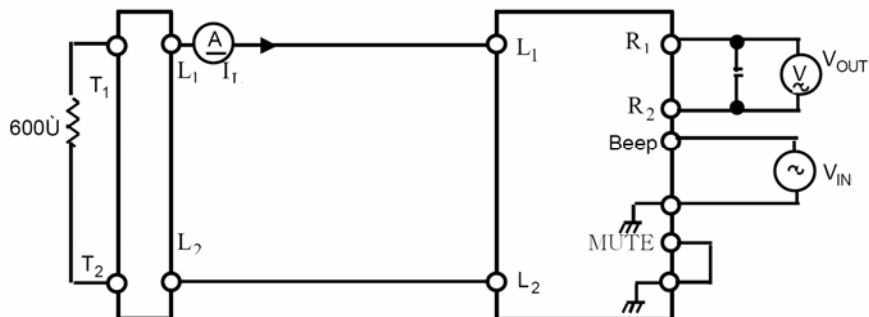
Test Circuit (continued)

7.  $G_R$ ,  $DR_R$  (at  $R_L=150\Omega$ ; Low Impedance Type Receiver)



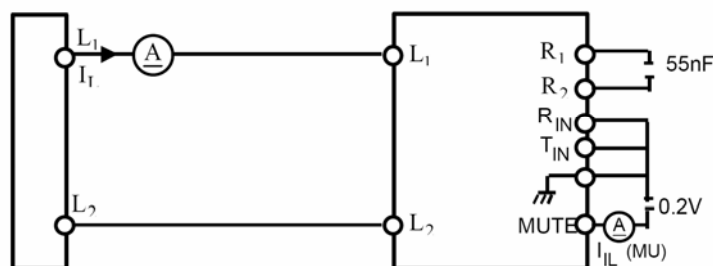
- Receiving Gain, (dB)
- Receiving Dynamic Range: -p)  
at  $V_{OUT}$ : DIST= 10%

8.  $G_{BP}$ ,  $DR_{BP}$



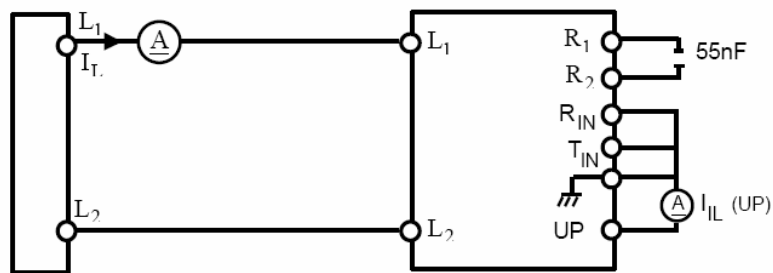
- Beep Gain,  $G_{BP} = 20 \log |V_{OUT} / V_{IN}|$  (dB)
- Beep Dynamic Range:  $DR_{BP} = V_{OUT}$  (Vp-p)  
at  $V_{OUT}$ : DIST= 10%

9.  $G_{IL}$  (MU)

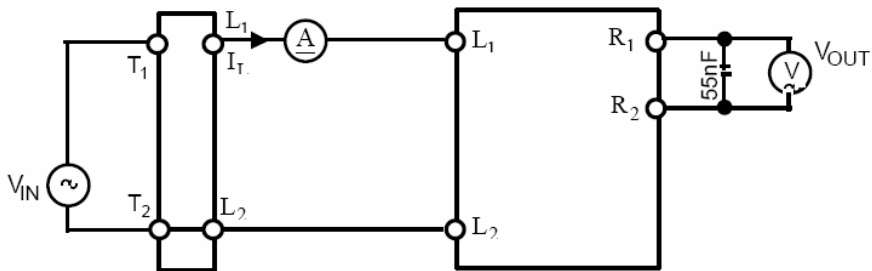


Test Circuit (continued)

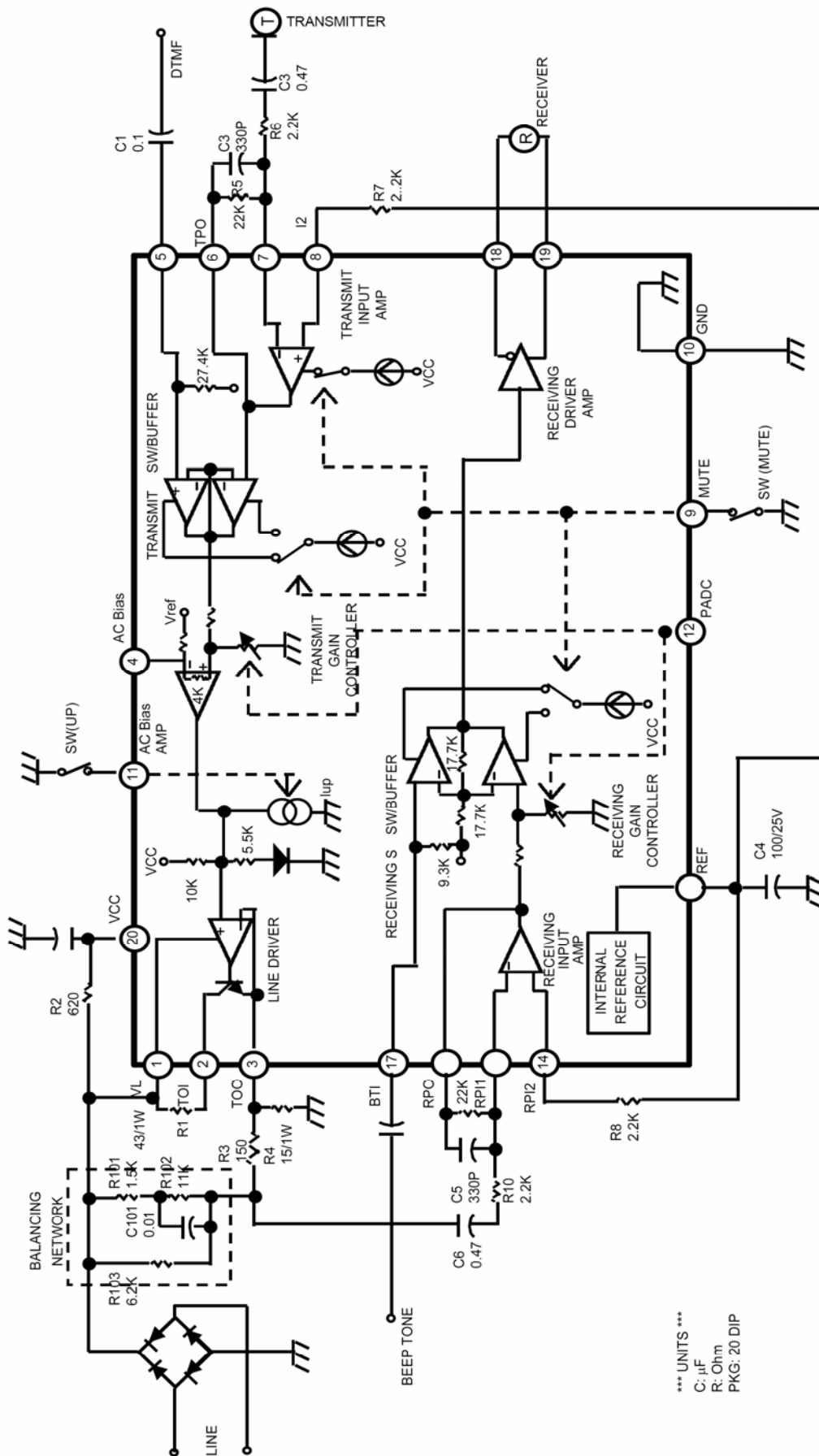
10.  $I_{IL}$  (UP)



11.  $G_R$  (Total)

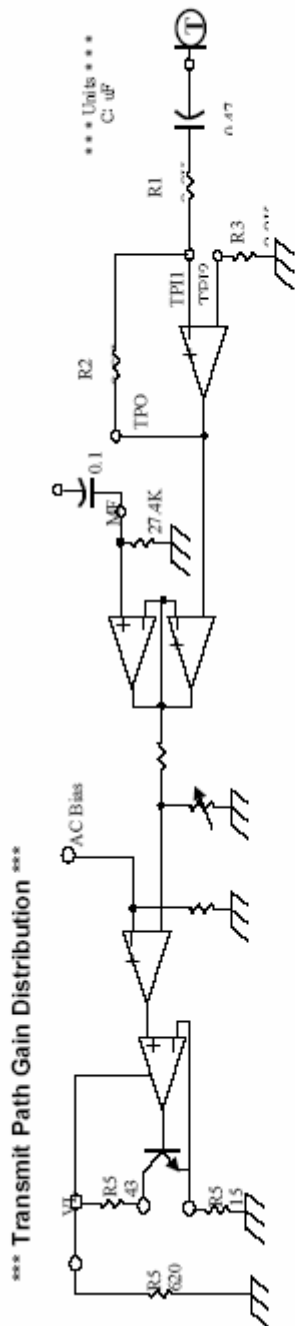


- Total Receiving Gain,  $G_R(\text{Total}) = 20 \log |V_{OUT} / V_{IN}|$  (dB)  
 \*Balancing circuit included



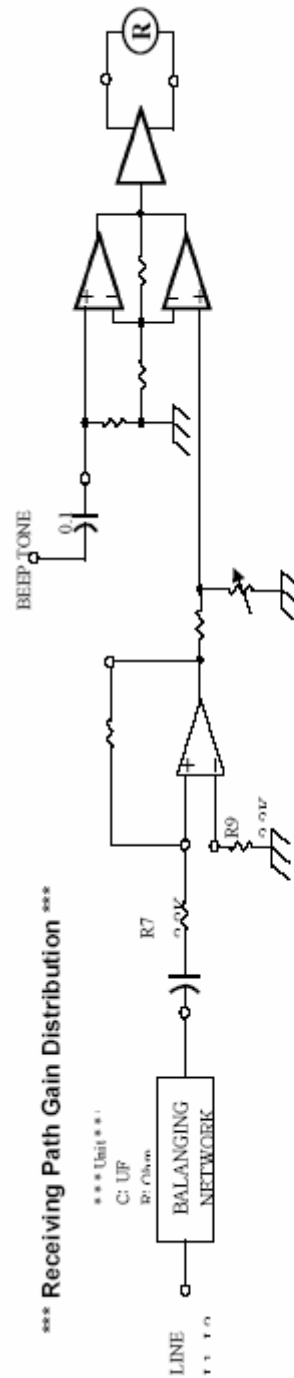
\*\*\* UNITS \*\*\*  
 C: µF  
 R: Ohm  
 PKG: 20 DIP

Gain Distribution



The Gain value is the one roughly determined

Line Drive Amp.	AC Bias Amp.	Transmit PAD	Transmit SW/Buffer	Transmit Input Amp.
IL=20mA IL=120mA	26 dB (At line 600 Ohm termination)	0 dB -3 dB	0 dB	20 dB (Externally Adjustable)



The Gain value is the one roughly determined

Balancing Network	Receiving Input Amp.	Receiving PAD	Receiving SW/Buffer	Receiving Input Amp.
IL=20mA IL=120mA	-29 dB (Externally Adjustable)	0 dB -5.5 dB	0 dB	20 dB (Externally Adjustable)

**Description Functions**

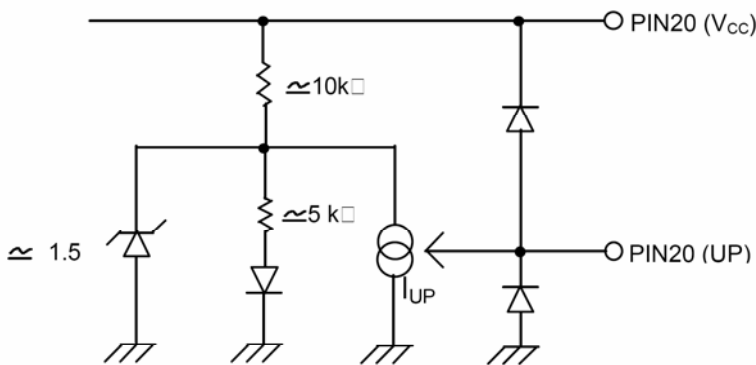
**1. Line voltage increasing circuit (up)**

The voltage of  $V_L$ ,  $V_{CC}$  or  $V_{REF}$  can be increased by connecting UP terminal to GND directly or through the resistance.

The internal equivalent circuit is as shown in the figure.

- (1) The voltage increased most up to about 1.5V in  $V_L$  when UP terminal is directly connected to GND. when the resistance is inserted the voltage increases according to the resistance value. (See graph)
- (2) In case of usage with MUTE terminal connected, the line voltage can be increased only at muting.
- (3) Avoid impressing the voltage over  $V_{CC}$  or under GND.
- (4) When not in use, make the circuit opened or connected to  $V_{CC}$ .

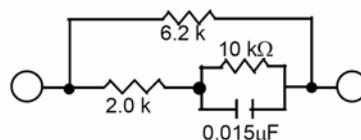
Internal equivalent circuit



**2. Side tone protection circuit (Balancing circuit)**

The time constant (hereafter referred to as BN constant) of the side tone protection circuit in the example of application circuit is adjusted nearly to  $0.4\phi$  7dB. Since the side tone characteristic varies according to this BN time constant, adjust the time constant confirming to the function of the telephone set.

EXAMPLE OF BN TIME CONSTANT

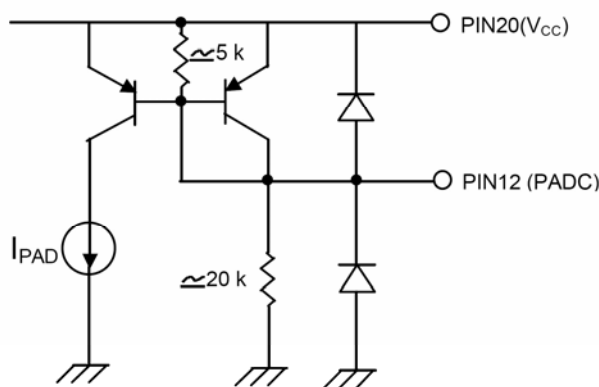


In case of  $0.5\phi$  7dB is determined to be the center.

### 3. Gain control circuit (PADC)

- 1) PADC terminal open state. Transmitting and receiving gains vary automatically according to the line current amount (Auto-PAD). With the increase of line current amount; the gain attenuates by about - 3dB at transmitting and about - 5.5dB at receiving.
- 2) In case PADC terminal is connected to GND by resistance. The gain begins to attenuate with the line current amount less than that when PADC terminal is open. Set the value of resistance to be connected at 25k or over.
- 3) In case PADC terminal is connected to VCC by resistance. The gain begins to attenuate with the line current amount more than that when PADC terminal is open. Set the value of resistance to be connected at 10k or over.

\* Internal equivalent circuit.

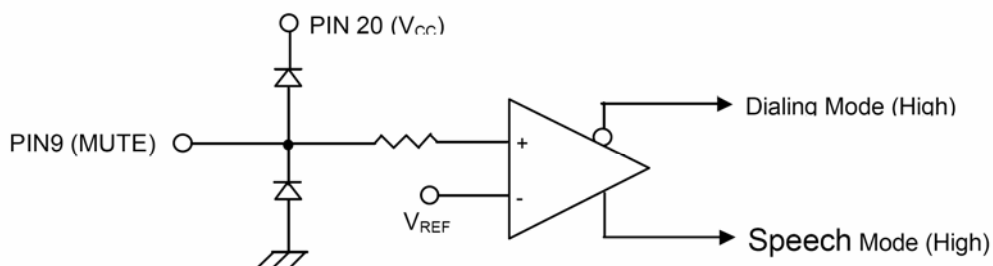


### 4. MUTE circuit (MUTE)

The internal equivalent circuit in the MUTE terminal is shown in the figure below. Since the protective diode is connected between  $V_{CC}$  and GND, avoid impressing the voltage over that of  $V_{CC}$  or below GND.

This is most suitable for input from the output of open drain or open collector type.

\* Internal equivalent circuit.



**Application**

**1. Transmitter**

As the transmitter, the condenser microphone, the ceramic type and the dynamic type (speaker type) are available. However, since and of FET or transistor built-in require the bias circuit. Externally provide the bias circuit. For example, refer to the example of the application circuit.

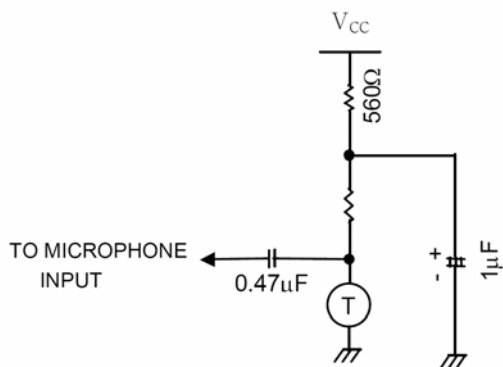
**2. Receiver**

As the receiver, the ceramic type the low-impedance (dynamic type) are available.

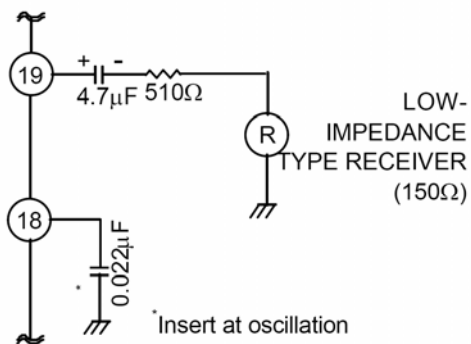
- (1) Ceramic type; The receiver of equivalent capacity of about 55nF is assumed. In case of the ceramic type, since the large voltage amplitude is generally required at driving, make the receiver function in BTL mode.
- (2) Low-impedance type; The receiver of equivalent resistance of about 150 is assumed. For the connections, refer to the example of application circuit.

**3. Example of Application circuit.**

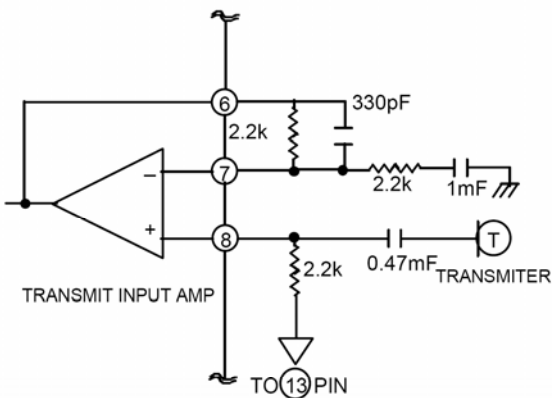
(1) EXAMPLE OF POWER SUPPLY CIRCUIT FOR CONDENSER MICROPHONE



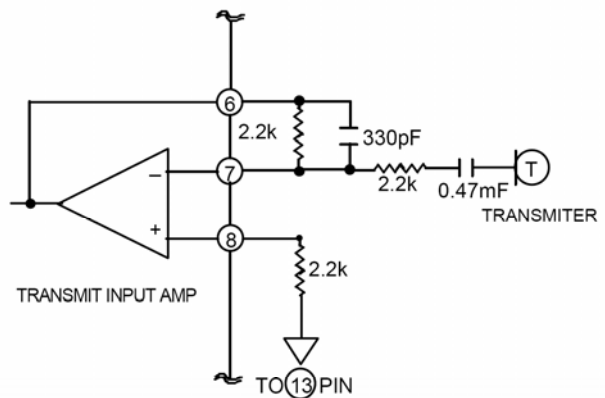
(2) EXAMPLE OF CONNECTION CIRCUIT OF LOW-IMPEDANCE TYPE RECEIVER.



(3) In case of using transmit input amplifier as non-inversion input.



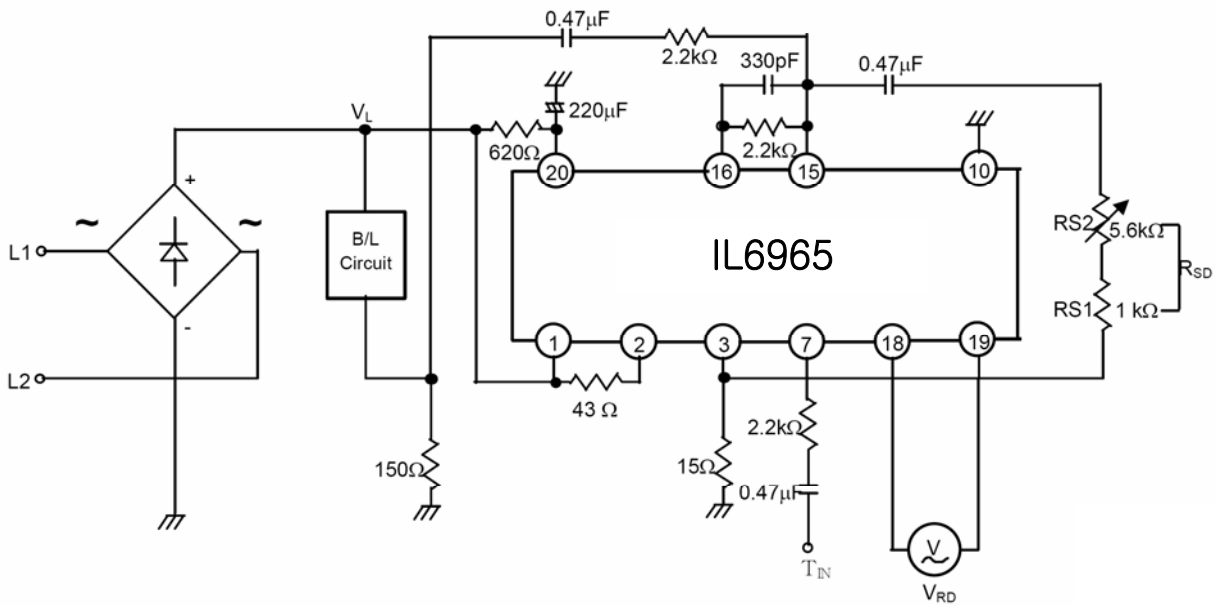
(4) In case of using transmit input amplifier as inversion input.



Note : In test circuit and application circuit, transmit input amplifier is set at inversion input.

4. Side Tone Gain Control.

(1) Alternative application for side tone gain control



- The side tone gain is externally controlled by the resistor  $R_{SD}$  ( $R_{S1}+R_{S2}$ )
- The maximum available control range of side tone gain is 0dB to 14 dB.

(2) Side tone gain,  $G_{SD}$  to Resistor,  $R_{SD}$

$R_{SD}$ ( $R_{S1}+R_{S2}$ )	$G_{SD}$
1k	14.2dB
2k	11.1dB
3k	2.5dB
3.5k	0.2dB
4k	1.6 dB
5k	5.4 dB
6k	7.5 dB

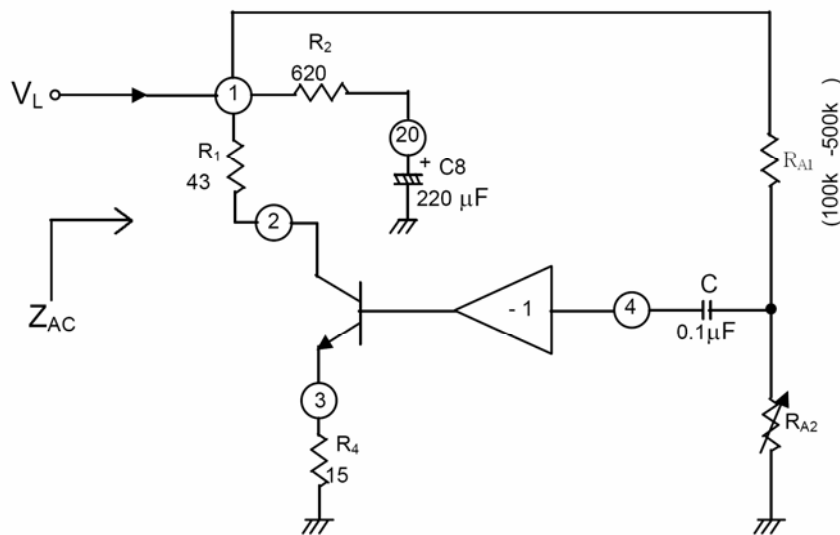
(3) The side tone gain is

$$G_{SD} = 20 \log\left(\frac{V_{RO}}{V_L}\right) \text{ (dB)}$$



**5. AC Impedance UP control.**

(1) Application for AC impedance up control



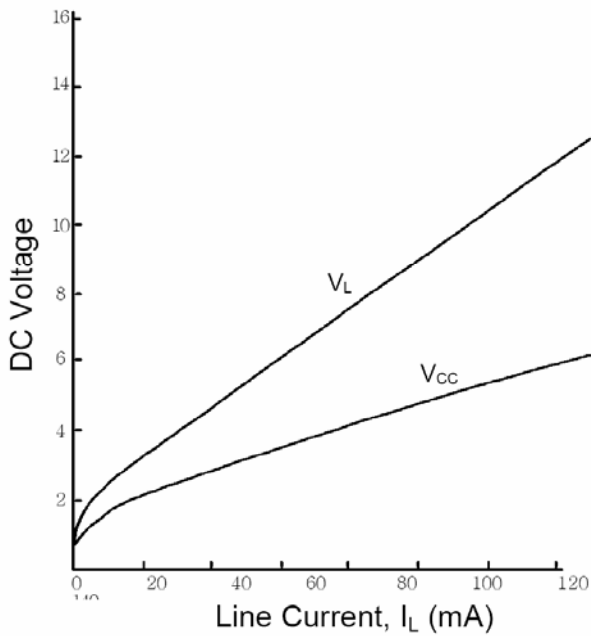
- The AC Impedance (\$Z\_{AC}\$) can be increased by using AC Bias terminal (Pin ).
- The AC Impedance up amount is determined by the external resistors \$R\_1\$, \$R\_2\$ value. :

(2) The AC impedance is

$$Z_{AC} = \frac{V_L}{I_L} = \frac{1}{\frac{1}{R_2} + \frac{1}{R_4 + \left(\frac{R_{A2}}{R_{A1} + R_{A2}}\right)}}$$

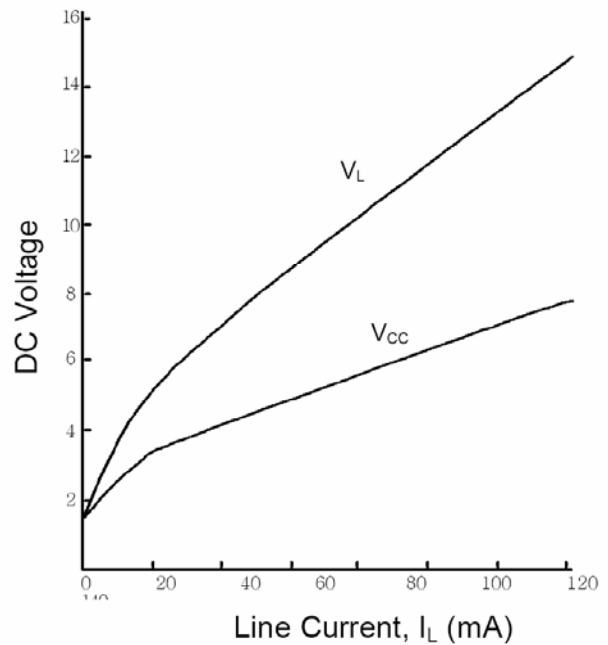
**DC Characteristic (Normal)**

Test Circuit 1



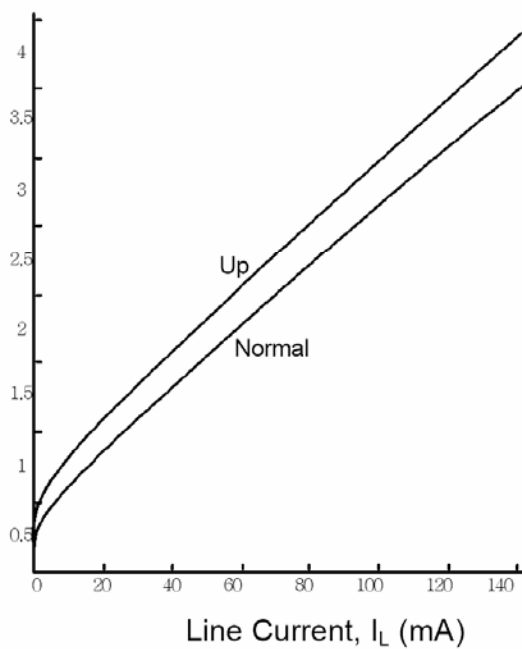
**DC Characteristic (UP)**

Test Circuit 2



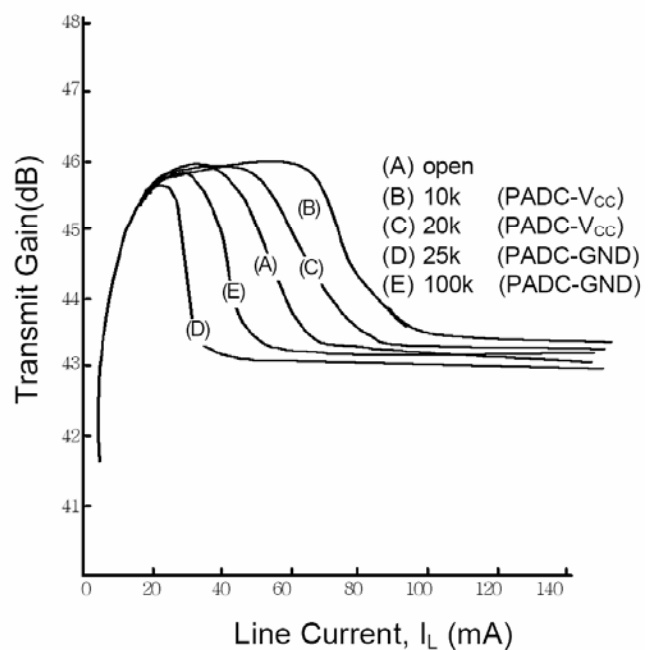
**V<sub>REF</sub> Voltage to Current Characteristic**

Test Circuit 3



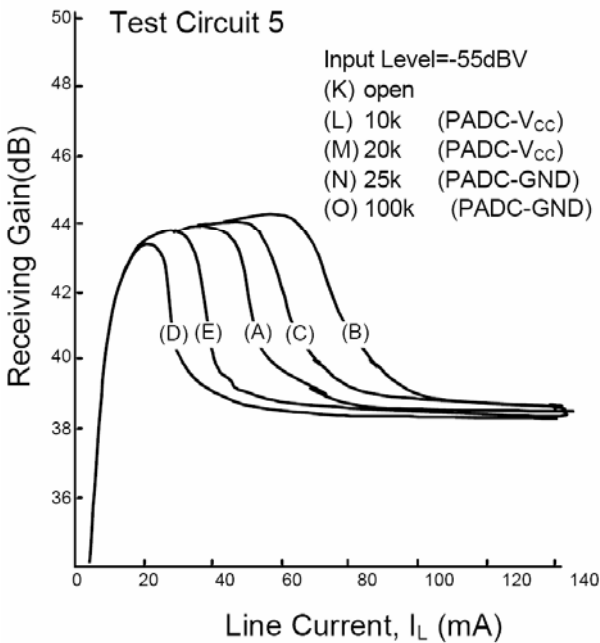
**Transmit Gain to Current Characteristic**

Test Circuit 4



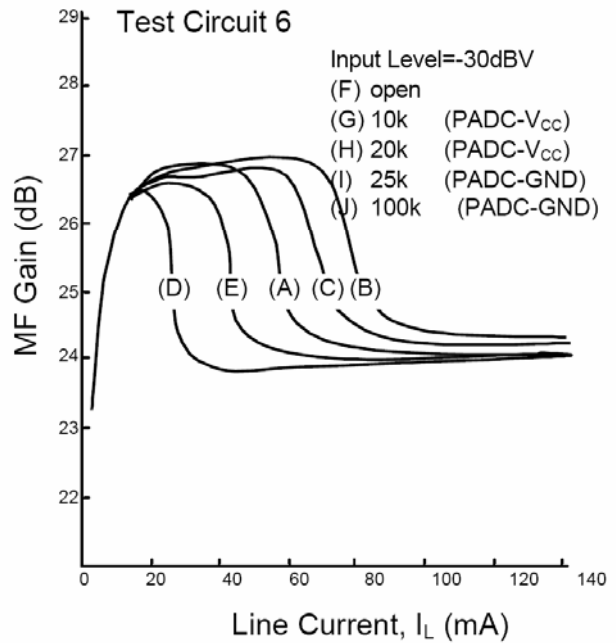
**Receiving Gain to Current Characteristic**

Input=pin 15, -55dBV  
Output=pin 18, pin 19



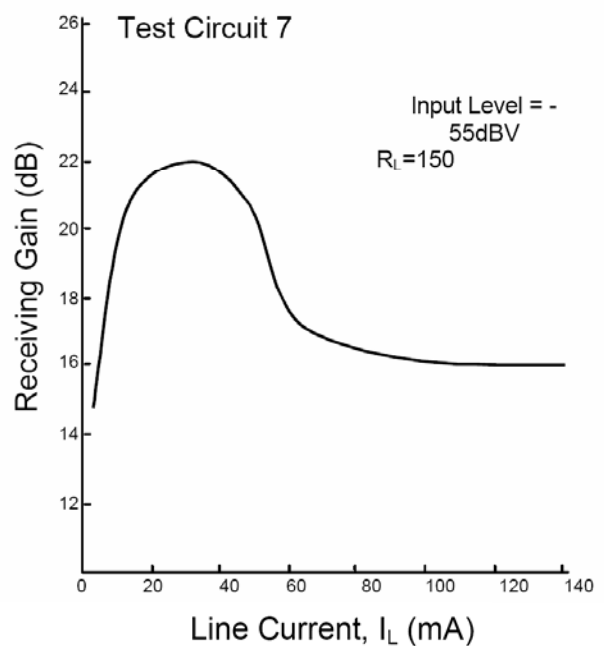
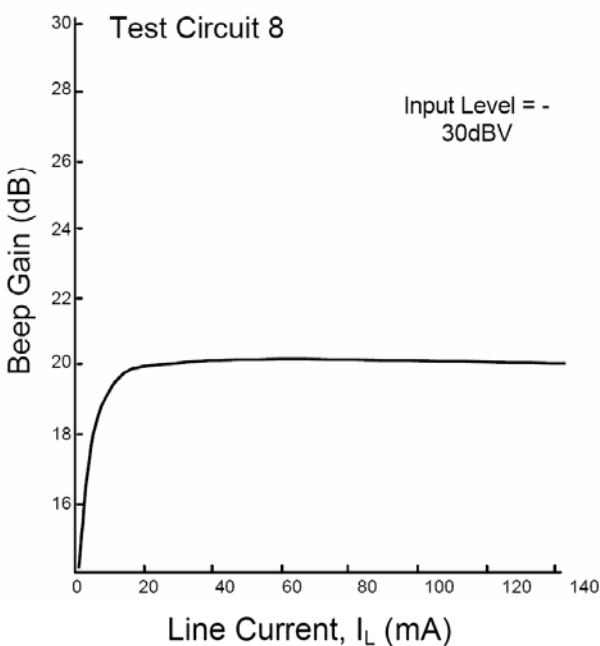
**MF Gain to Current Characteristic**

Input=pin 15, -30dBVrms  
Output=pin 1

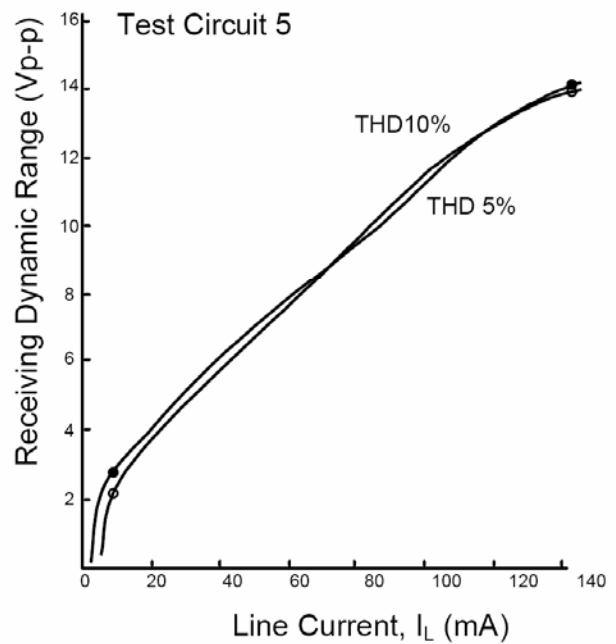
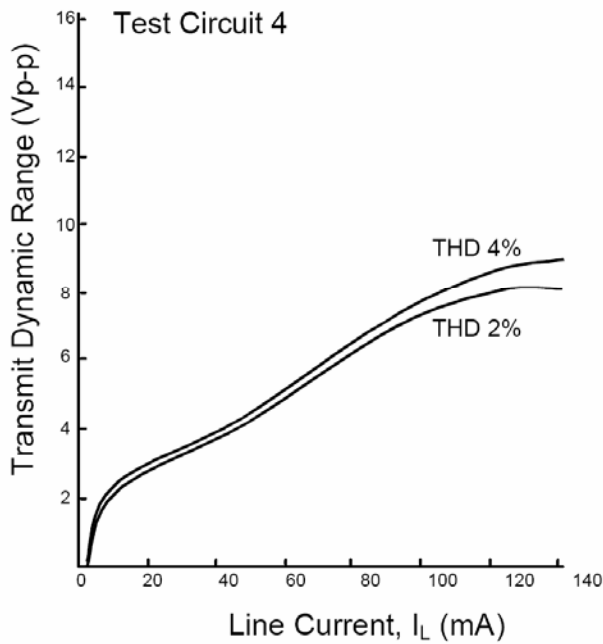


**Beep Gain to Current Characteristic**

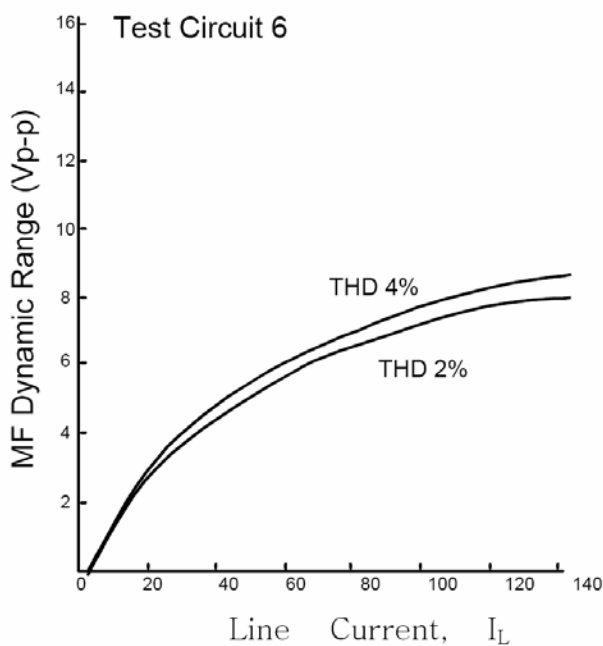
**Receiving Gain to Current Characteristic**  
(at using Low-impedance type receiver ;  
R<sub>L</sub>=150 Ω)



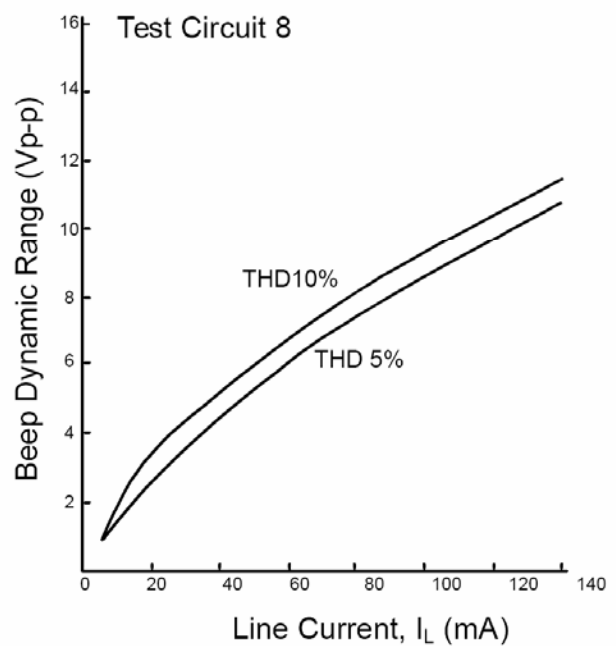
Transmit Dynamic Range to Current Characteristic Receiving Range to Current Characteristic



DTMF Dynamic Range to Current Characteristic

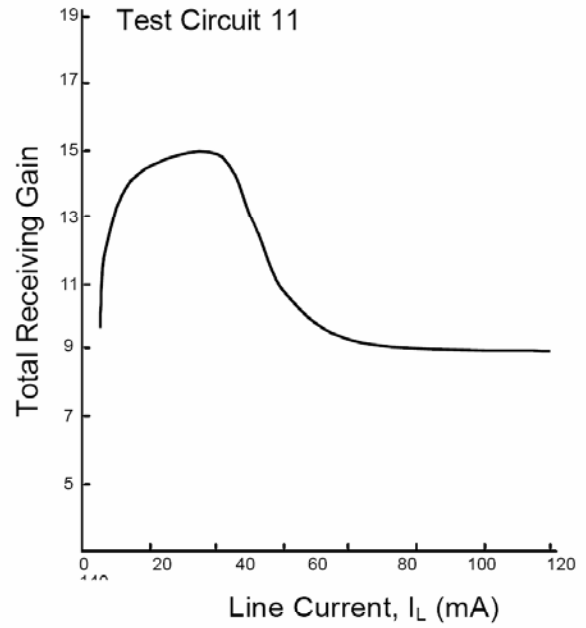
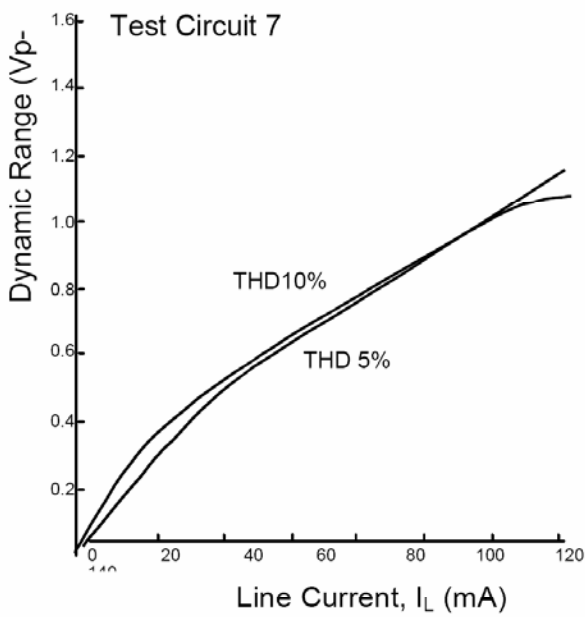


Beep Dynamic Range to Current Characteristic

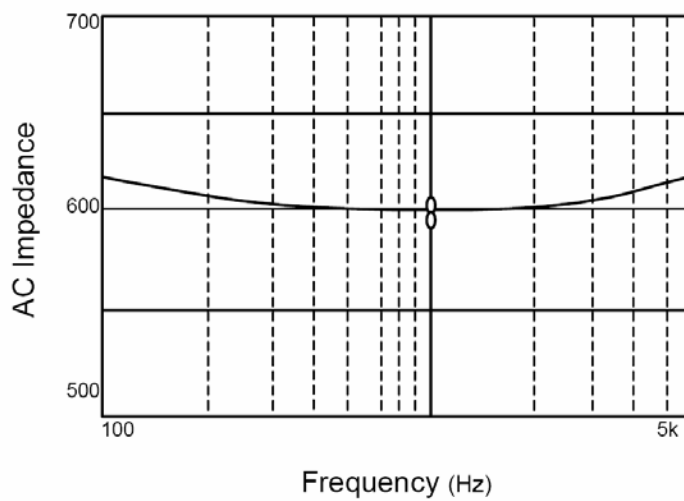


**Receiving Dynamic Range to Current Characteristic  
At using Low-Impedance type Receiver ;  $R_L=150$**

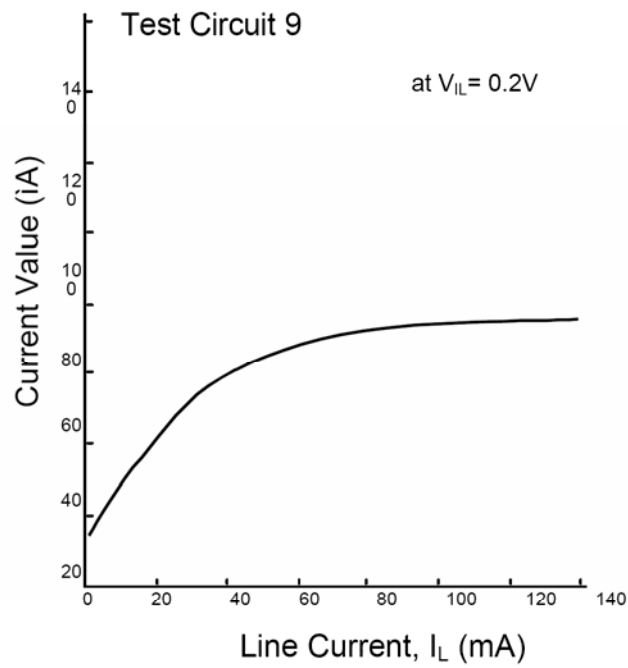
**Total Receiving Gain to Current Characteristic  
(Balancing circuit included)**



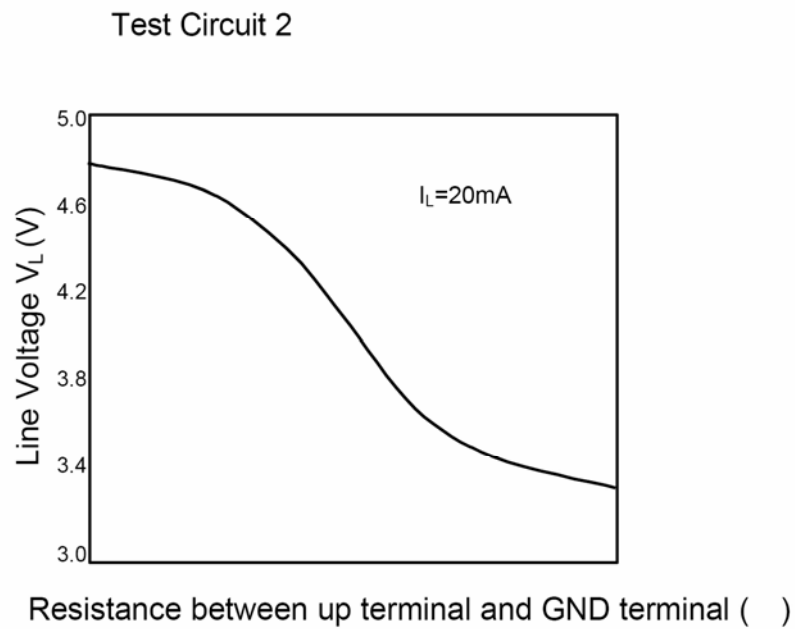
**AC Impedance to Frequency Characteristic ( $I_L = 120$  mA)**



Mute Terminal pull-up current characteristic

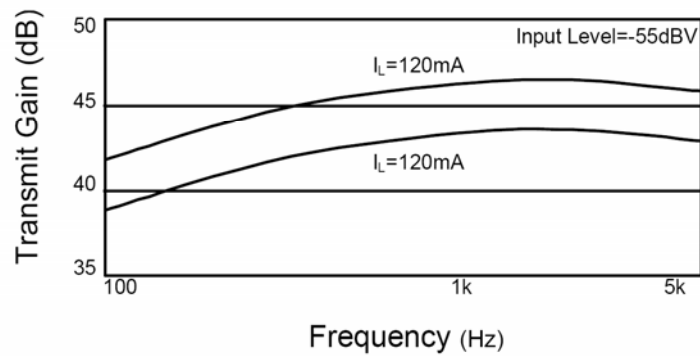


Line Voltage Rise up Characteristic



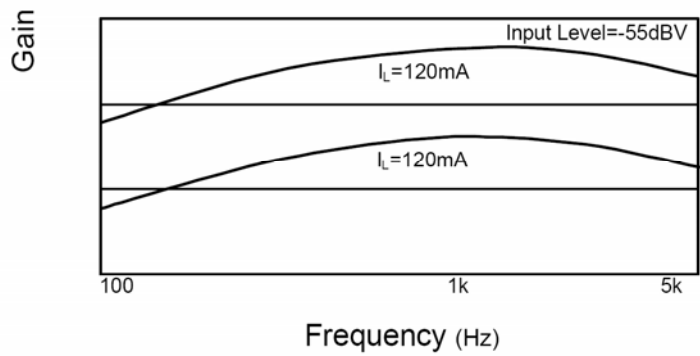
**Transmit Gain to Frequency Characteristic**

**Test Circuit 4**



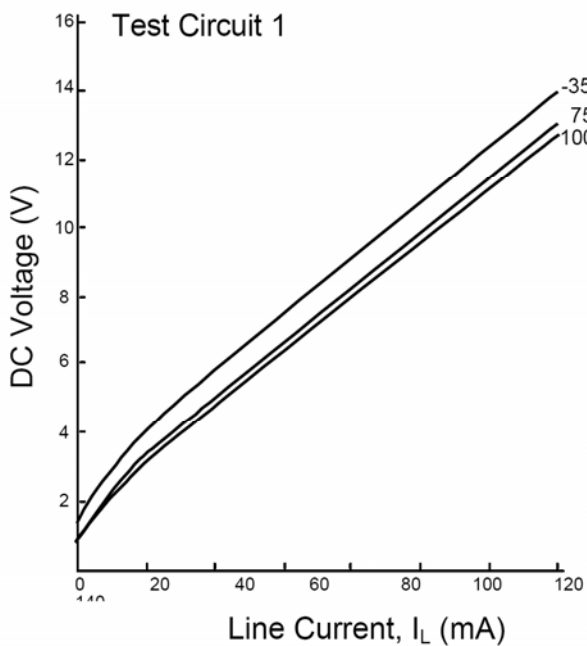
**Receiving gain to Frequency Characteristic**

**Test Circuit 5**



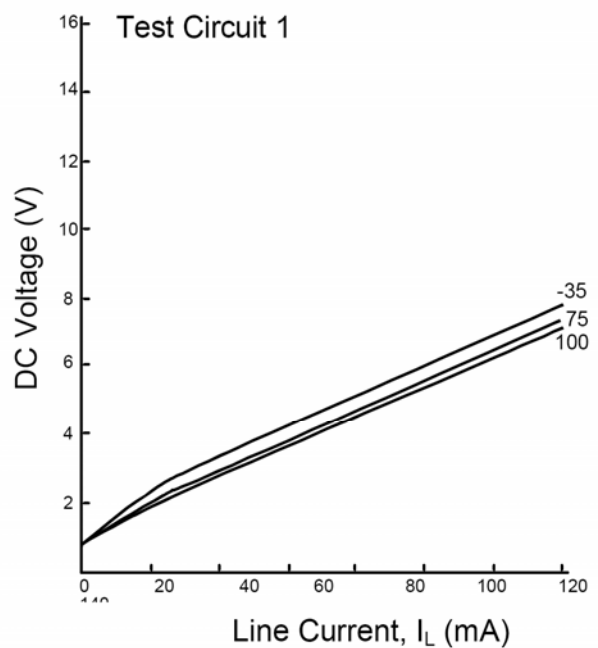
**Line Voltage to Temperature Characteristic**

**Test Circuit 1**

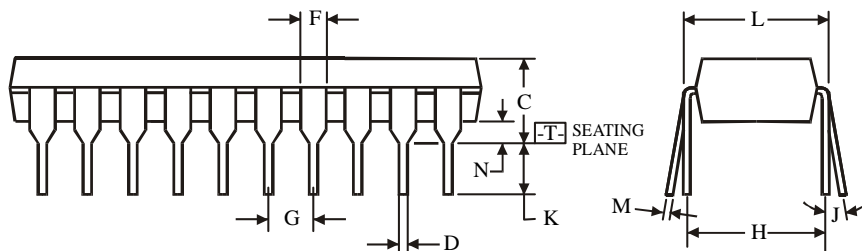
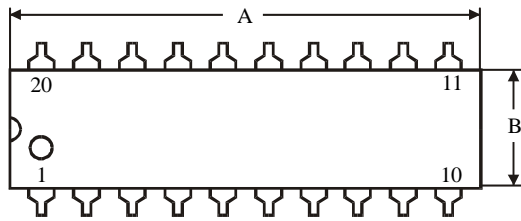
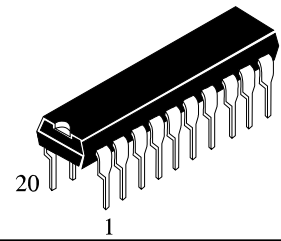


**Internal Power Supply Voltage to Temperature Characteristic**

**Test Circuit 1**



**N SUFFIX PLASTIC DIP  
(MS - 001AD)**



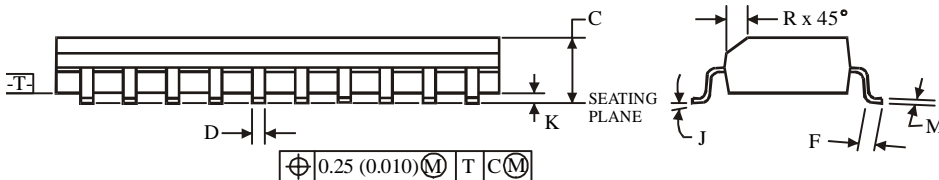
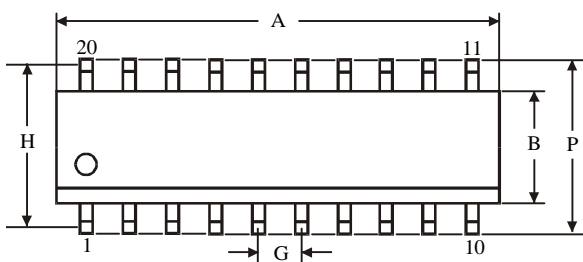
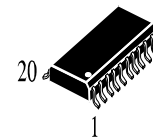
$\oplus 0.25 (0.010) \text{ (M) } \text{ (T)}$

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	24.89	26.92
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

**D SUFFIX SOIC  
(MS - 013AC)**



$\oplus 0.25 (0.010) \text{ (M) } \text{ (T) } \text{ (C) } \text{ (M)}$

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	12.60	13.00
B	7.40	7.60
C	2.35	2.65
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.10	0.30
M	0.23	0.32
P	10.00	10.65
R	0.25	0.75