



# 3.3V CMOS 16-BIT REGISTER WITH CLOCK ENABLE AND 5 VOLT TOLERANT I/O

**IDT74LVC2X377**  
**ADVANCE**  
**INFORMATION**

## FEATURES:

- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,  
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- Rail-to-Rail output swing for increased noise margin

### Drive Features for LVC2X377:

- High Output Drivers: ±24mA
- Reduced system switching noise

## DESCRIPTION:

This 16-bit register with clock enable is built using advanced dual metal CMOS technology. This high-speed, low power device is a 16-bit register with a buffered clock, buffered output drive, and synchronous clock enable, that is ideal for driving high capacitance loads such as memory address and data buses.

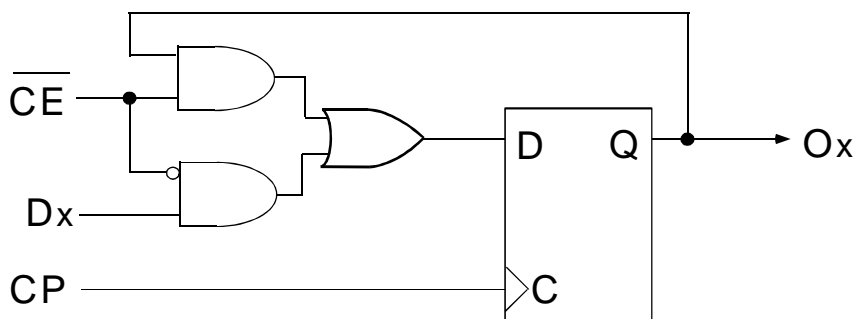
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

The LVC2X377 16-bit device is configured for flexibility as two 8-bit slices, each with individual Clock and Enable inputs.

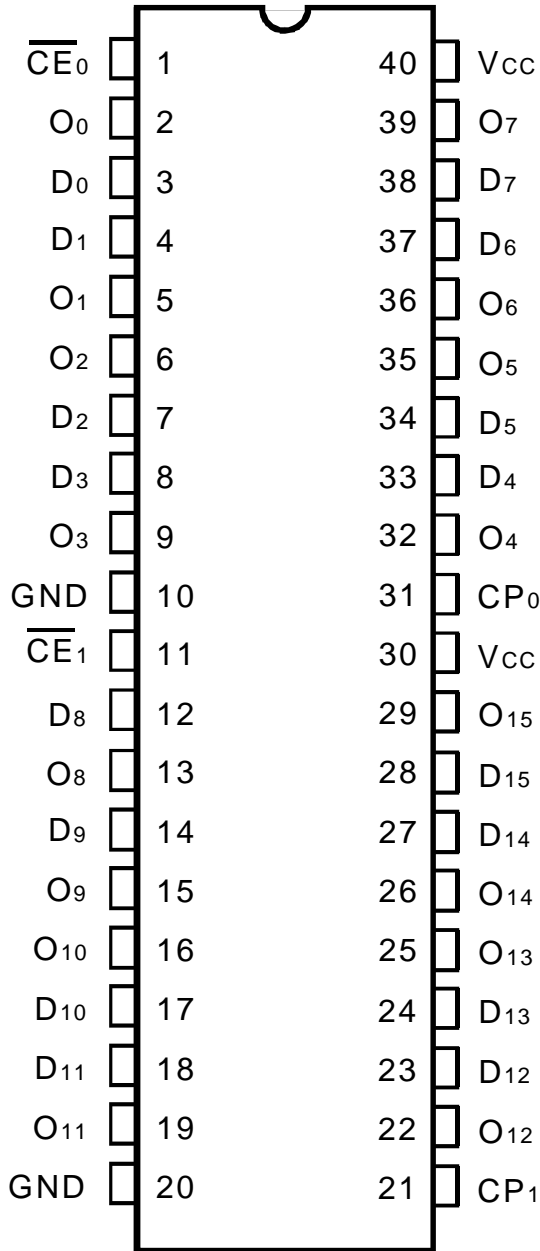
## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION



QVSOP  
TOP VIEW

### ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current	- 50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

**NOTE:**

1. As applicable to the device type.

### PIN DESCRIPTION

Pin Names	Description
CE <sub>0,1</sub>	Clock Enable Input (Active LOW)
CP <sub>0,1</sub>	Clock Input
O <sub>x</sub>	Data Outputs
D <sub>x</sub>	Data Inputs

### FUNCTION TABLE (1)

Inputs			Internal Q Value	Outputs O <sub>x</sub>	Function
CE	CP	D <sub>x</sub>			
H	↑	X	NC	NC	Hold Value
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	

**NOTE:**

- 1. H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care
- ↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  To  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = 0 to 5.5V	—	—	±10	μA
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 5.5V		—	—	±50	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>	—	—	20	μA
			3.6 ≤ V <sub>IN</sub> ≤ 5.5V <sup>(2)</sup>	—	—	20	
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND V <sub>CC</sub> = 3.0 – 3.6V		—	—	500	μA

### NOTES:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -24mA	2.2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	

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### NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range.  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

**OPERATING CHARACTERISTICS,  $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 25^\circ C$**

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	$C_L = 0pF$ , $f = 10MHz$		pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled			pF

**SWITCHING CHARACTERISTICS <sup>(1)</sup>**

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
$t_{PLH}$	Propagation Delay	1.5	9.5	1	8.5	ns
$t_{PHL}$	CP to Ox					
$t_{SU}$	Data Setup Time, Dx to CP	2.5	—	2.5	—	ns
$t_H$	Data Hold Time, Dx to CP	1.5	—	1.5	—	ns
$t_{SU}$	Clock Enable Data Setup Time, $\overline{CE}$ to CP	3	—	3	—	ns
$t_H$	Clock Enable Data Hold Time, $\overline{CE}$ to CP	1.5	—	1.5	—	ns
$t_w$	CLK Pulse Width HIGH or LOW	3.3	—	3.3	—	ns
$t_{sk(o)}$	Output Skew <sup>(2)</sup>	—	—	—	500	ps

**NOTES:**

1. See test circuits and waveforms.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
2. Skew between any two outputs of the same package and switching in the same direction.

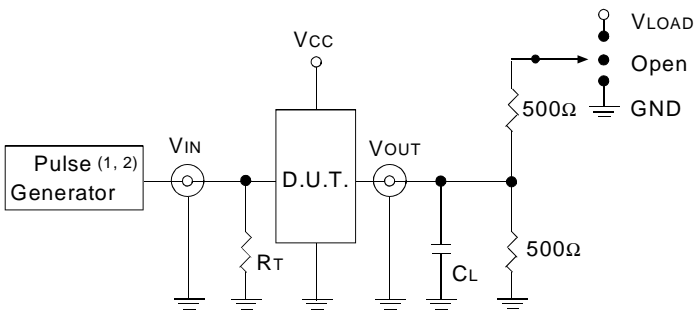
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1) = 3.3V ± 0.3V	V <sub>CC</sub> (1) = 2.7V	V <sub>CC</sub> (2) = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

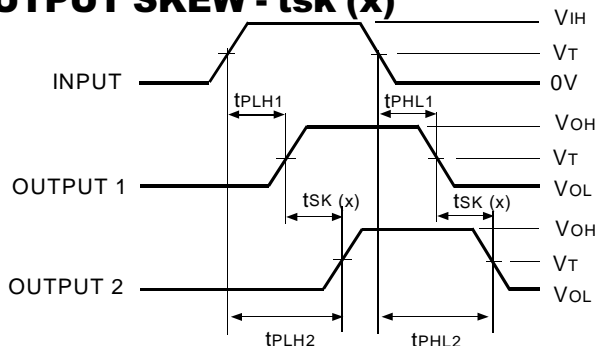
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain	V <sub>LOAD</sub>
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

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### OUTPUT SKEW - t<sub>SK</sub>(x)



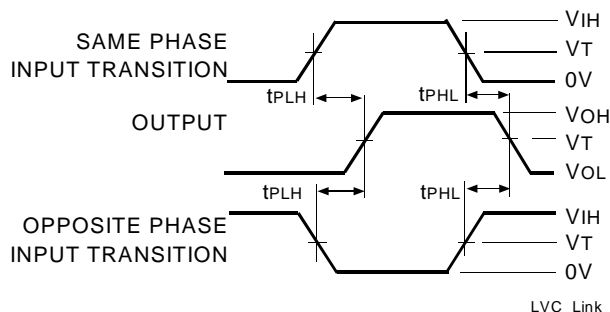
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

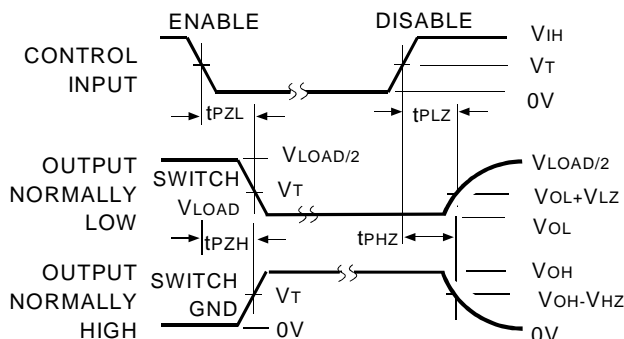
1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

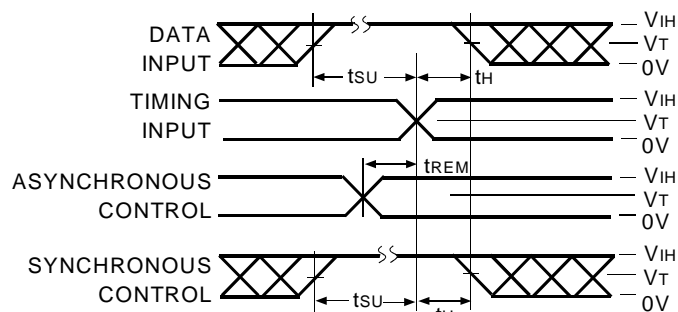


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#### NOTE:

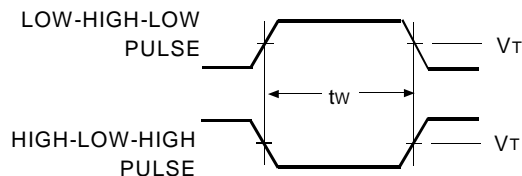
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



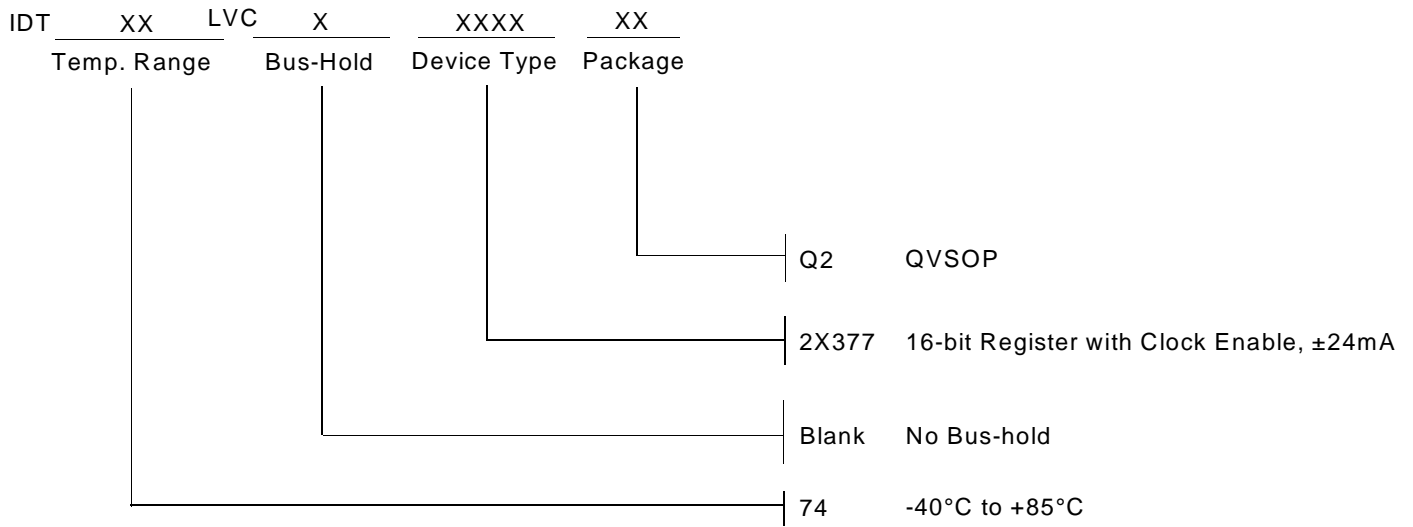
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### PULSE WIDTH



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