



3.3V CMOS DUAL J-K FLIP-FLOP WITH SET AND RESET, POSITIVE-EDGE TRIG- GER, AND 5 VOLT TOLERANT I/O

IDT74LVC109A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs, and I/Os are 5V tolerant
- Supports hot insertion
- Available in QSOP, SOIC, SSOP, and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

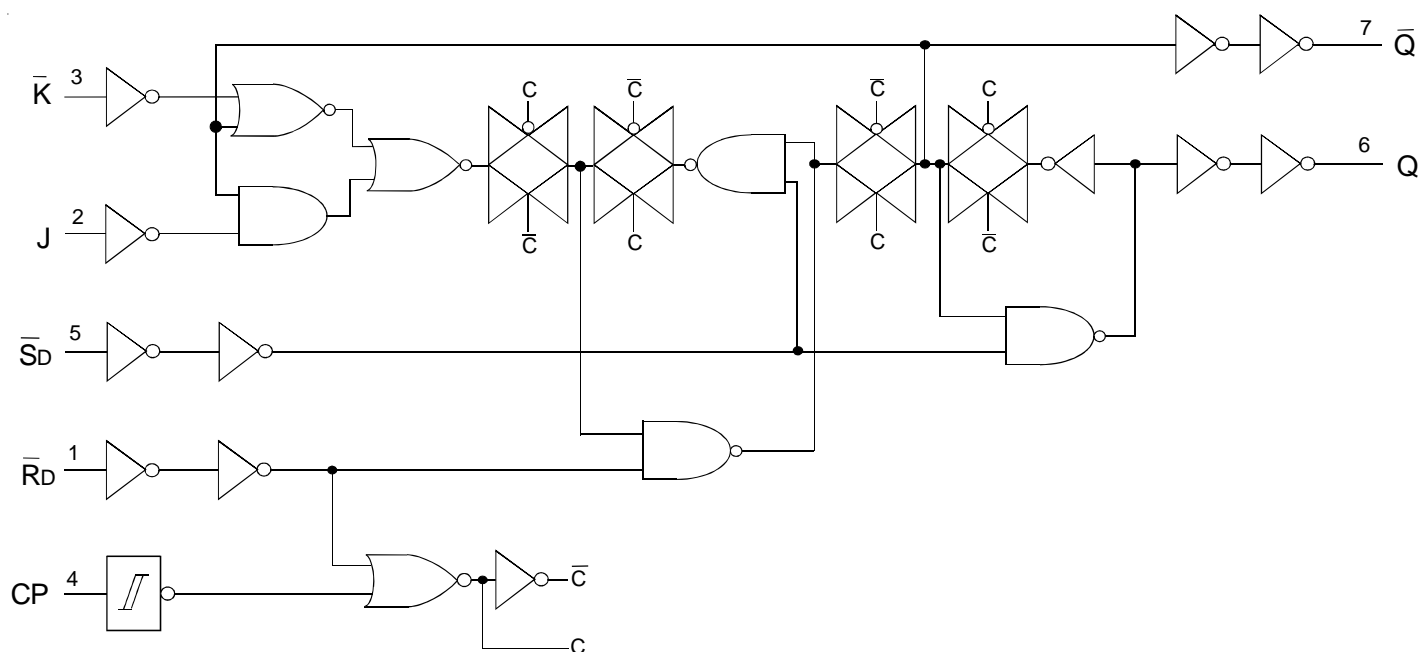
DESCRIPTION:

The LVC109A dual J-K flip-flop with set and reset, positive-edge trigger is built using advanced dual metal CMOS technology. This device features individual J, \bar{K} inputs, clock (CP) inputs, set (\bar{S}_D) and reset (\bar{R}_D) inputs; also complementary Q and \bar{Q} outputs. The set and reset are asynchronous active low inputs and operate independently of the clock input. The J and \bar{K} inputs control the state changes of the flip-flops as described in the function table. The J and \bar{K} inputs must be stable one setup time prior to the low-to-high clock transition for predictable operation. The J-K design allows operation as a D-type flip-flop by tying the J and \bar{K} inputs together.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC109A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

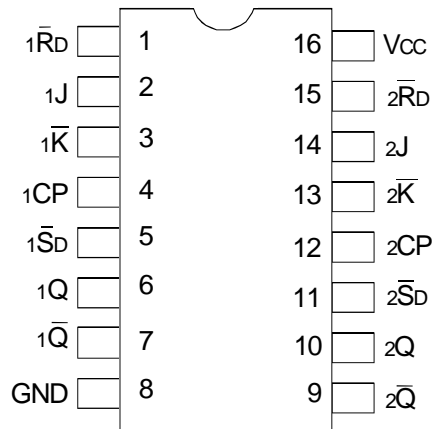
FUNCTIONAL BLOCK DIAGRAM



NOTE:

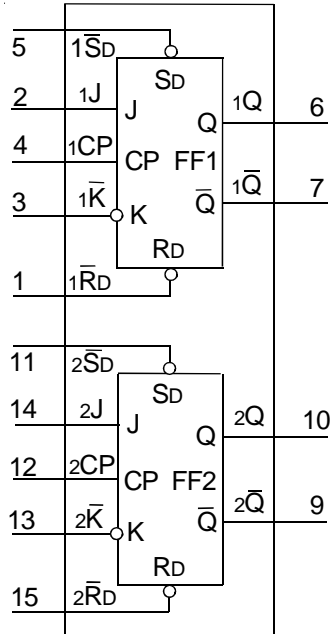
Pin numbers are for section 1. Refer to pin configuration for section 2 pin numbers.

PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xCP	Clock Inputs, LOW-to-HIGH, edge-triggered
xR _D	Asynchronous Reset Input (Active LOW)
xS _D	Asynchronous Set Inputs (Active LOW)
xJ, xK	Synchronous Inputs
xQ	True Flip-Flop Outputs
xQ	Complement Flip-Flop Outputs

FUNCTION TABLE ⁽¹⁾

Operating Modes	Inputs					Outputs	
	xSD	xRD	xCP	xJ	xK	xQ	xQ
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\bar{Q}^{(2)}$	$Q^{(3)}$
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	$Q^{(3)}$	$\bar{Q}^{(2)}$

NOTES:

- H = HIGH Voltage Level
h = HIGH voltage level of input set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level of input set-up time prior to LOW-to-HIGH CP transition
X = Don't Care
↑ = LOW-to-HIGH transition
- Complement of Q or level of \bar{Q} before the indicated steady-state input conditions were established.
- Level of Q before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V, V _{IN} = GND or V _{CC}		—	—	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = - 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V	I _{OH} = - 24mA	2.2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Flip-Flop	C _L = 0pF, f = 10Mhz	—	pF

SWITCHING CHARACTERISTICS⁽¹⁾

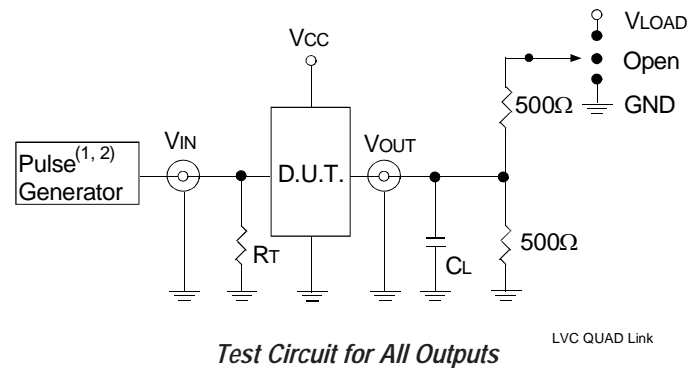
Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCP to xQ or x \bar{Q}	—	9	—	8.5	—	7.5	ns
t _{PLH}	Propagation Delay x \bar{S}_D to xQ or x \bar{R}_D x \bar{Q}	—	11	—	9	—	8	ns
t _{PHL}	Propagation Delay x \bar{S}_D to xQ or x \bar{R}_D x \bar{Q}	—	10	—	10	—	9	ns
t _{SU}	Set-up Time, xJ, x \bar{K} to xCP	2.5	—	2.5	—	2.5	—	ns
t _H	Hold Time, xJ, x \bar{K} to xCP	2	—	2	—	2	—	ns
t _{REM}	Removal Time, x \bar{S}_D , x \bar{R}_D to xCP	3	—	3	—	3	—	ns
t _w	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _w	Set or Reset Pulse Width, HIGH or LOW	3	—	3	—	3	—	ns
t _{sk(0)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ = 2.5V ± 0.2V	V _{CC} ⁽²⁾ = 3.3V ± 0.3V & 2.7V	Unit
V _{LOAD}	2 x V _{CC}	6	V
V _{IH}	V _{CC}	2.7	V
V _T	V _{CC} / 2	1.5	V
V _{LZ}	150	300	mV
V _{HZ}	150	300	mV
C _L	30	50	pF



DEFINITIONS:

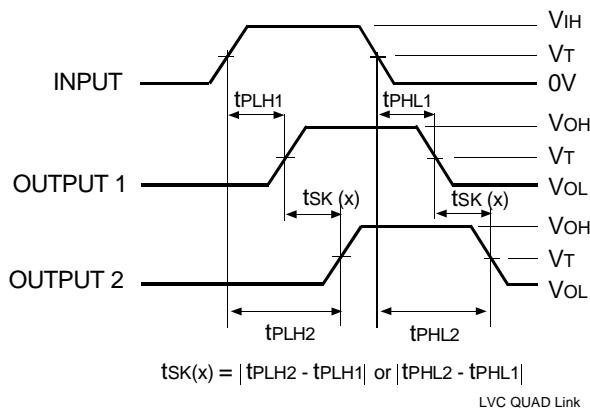
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.

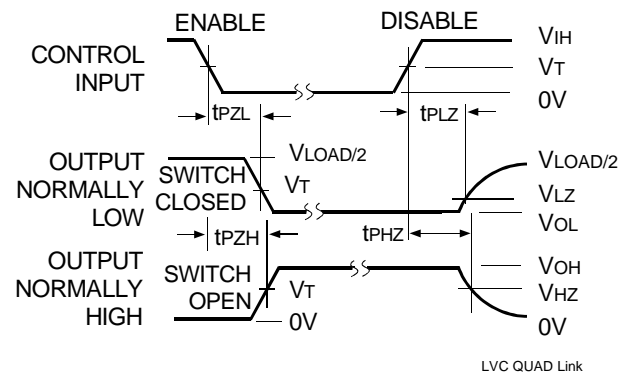
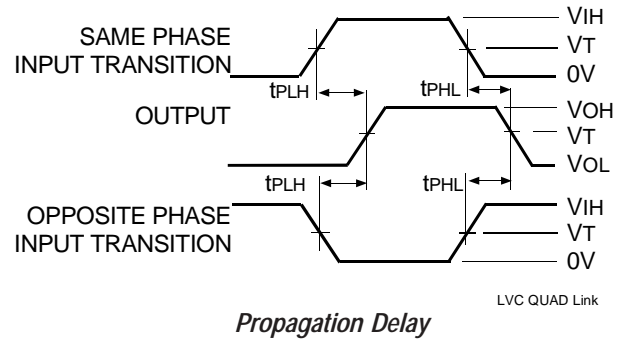
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



NOTES:

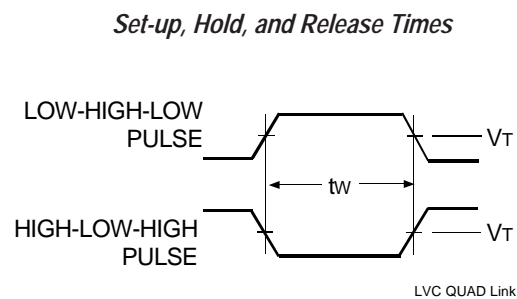
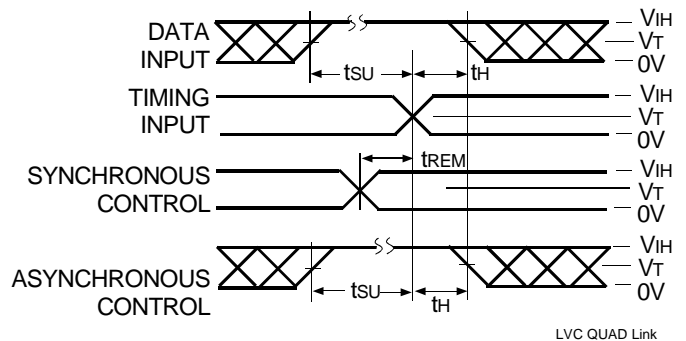
1. For t_{SK}(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



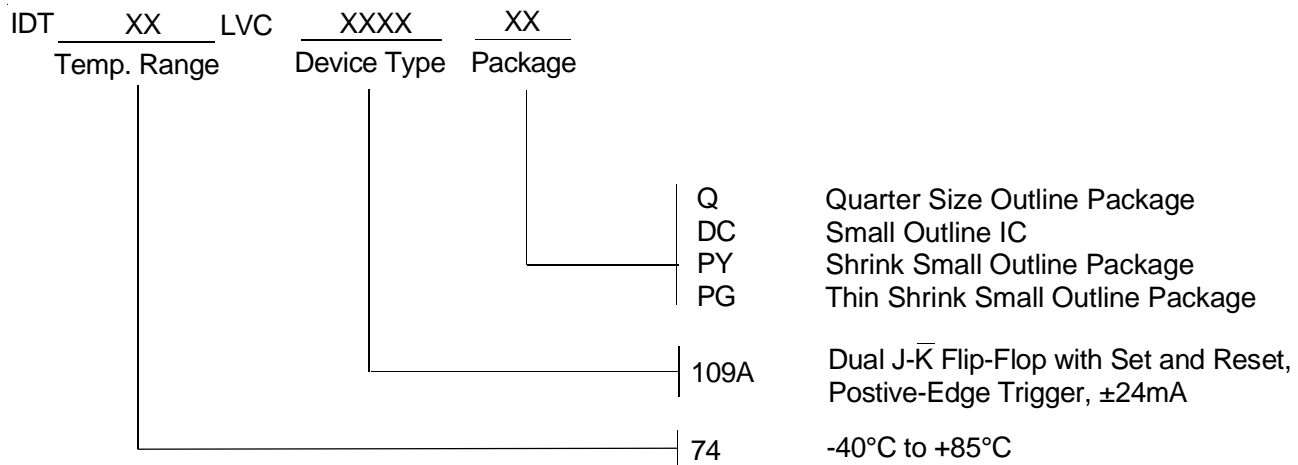
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



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