3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16543

FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 3.3V ± 0.3V, Normal Range**
- **Vcc = 2.7V to 3.6V, Extended Range**
- **Vcc = 2.5V ± 0.2V**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in SSOP, TSSOP, and TVSOP packages**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Suitable for heavy loads**

APPLICATIONS:

- **3.3V high speed systems**
- **3.3V and lower voltage computing systems**

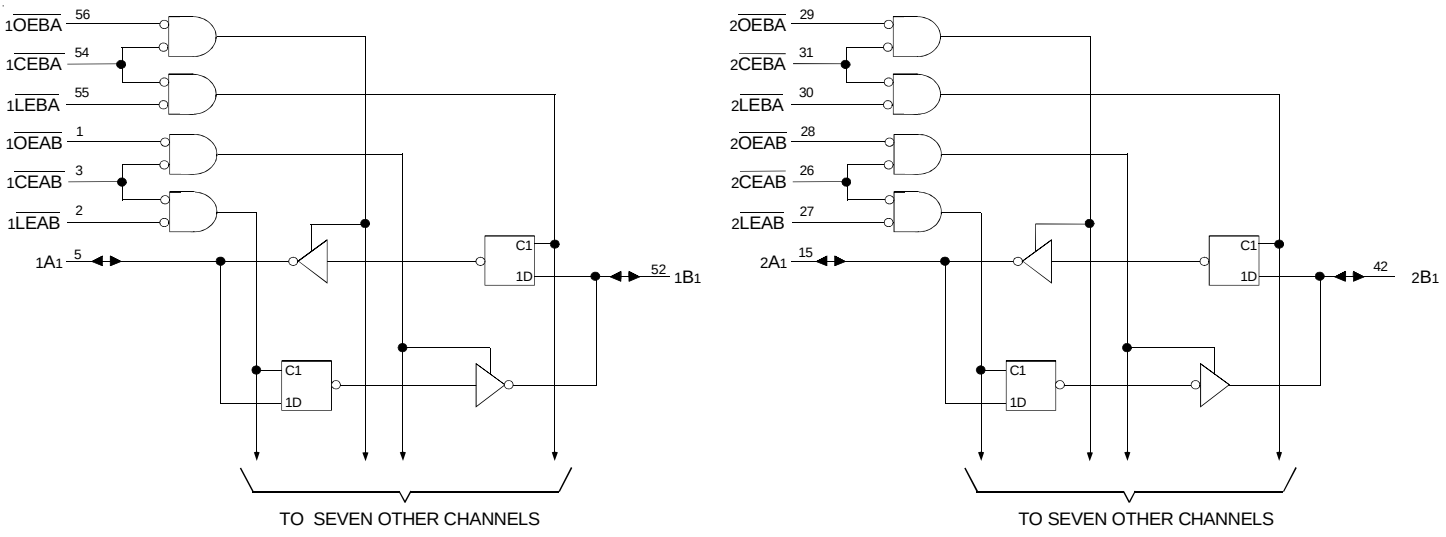
DESCRIPTION:

This 16-bit registered transceiver is built using advanced dual metal CMOS technology. The ALVCH16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

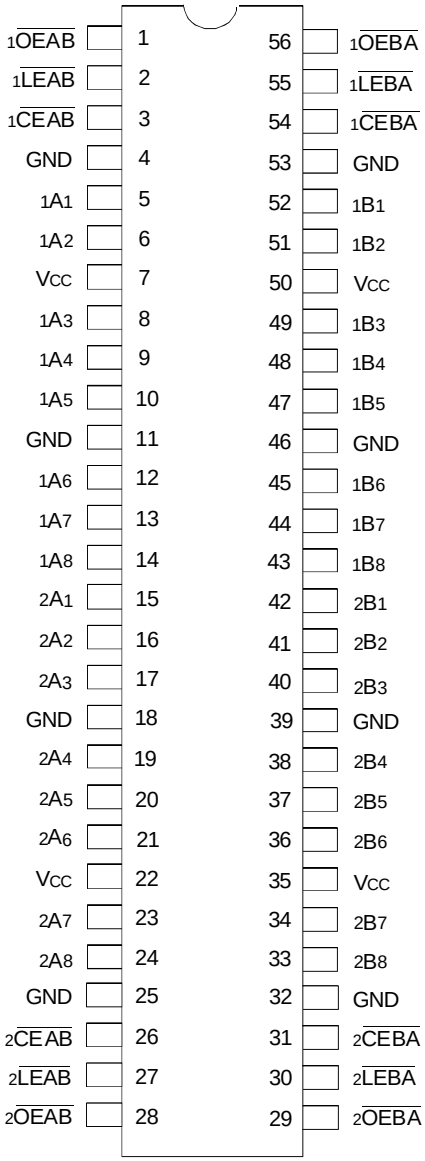
The ALVCH16543 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16543 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
x$\overline{OEAB}$	A-to-B Output Enable Inputs (Active LOW)
x$\overline{OEBA}$	B-to-A Output Enable Inputs (Active LOW)
x$\overline{CEAB}$	A-to-B Enable Inputs (Active LOW)
x$\overline{CEBA}$	B-to-A Enable Inputs (Active LOW)
x$\overline{LEAB}$	A-to-B Latch Enable Inputs (Active LOW)
x$\overline{LEBA}$	B-to-A Latch Enable Inputs (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs[1]
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs[1]

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	±50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

NOTE:
1. As applicable to the device type.

FUNCTION TABLE[1,2]

Inputs				Output
x$\overline{CEAB}$	x$\overline{LEAB}$	x$\overline{OEAB}$	xAx	xBx
X	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B[3]
L	L	L	L	L
L	L	L	H	H

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses x$\overline{CEBA}$, x$\overline{LEBA}$, and x$\overline{OEBA}$.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
3. Level of B before the indicated steady-state inputs were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	–75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	–45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA
I_{BHLO}							

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V Typical	V_{CC} = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	54	64	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		6	7	

SWITCHING CHARACTERISTICS(1)

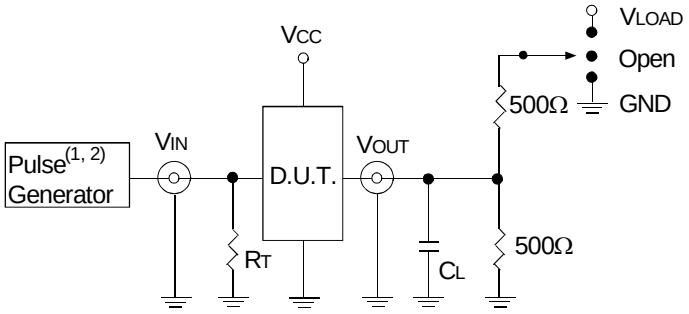
Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	1	5.1	—	4.8	1	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay x$\overline{LEAB}$ to xBx or x$\overline{LEAB}$ to xAx	1	6.5	—	6.2	1.1	5	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{CEAB}$ to xBx or x$\overline{CEAB}$ to xAx	1	7.2	—	6.9	1	5.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{CEAB}$ to xBx or x$\overline{CEAB}$ to xAx	1.3	6.1	—	6.2	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEAB}$ to xBx or x$\overline{OEAB}$ to xAx	1	6.8	—	6.3	1	5.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEAB}$ to xBx or x$\overline{OEAB}$ to xAx	1	5.7	—	4.8	1.1	4.6	ns
t_{SU}	Set-up Time, data before $\overline{CE}\uparrow$	1.2	—	1.5	—	1.2	—	ns
t_{SU}	Set-up Time, data before $\overline{LE}\uparrow$, $\overline{CE}$ LOW	1.2	—	1.5	—	1.2	—	ns
t_H	Hold Time, Ax data after $\overline{CE}\uparrow$	1.2	—	0.8	—	1.3	—	ns
t_H	Hold Time, Bx data after $\overline{LE}\uparrow$, $\overline{CE}$ LOW	1.2	—	0.8	—	1.3	—	ns
t_W	Pulse Duration, $\overline{LE}$ or $\overline{CE}$ LOW	3.3	—	3.3	—	3.3	—	ns
$t_{SK}(o)$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2 Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$=3.3V±0.3V	$V_{CC}^{(1)}$=2.7V	$V_{CC}^{(2)}$=2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

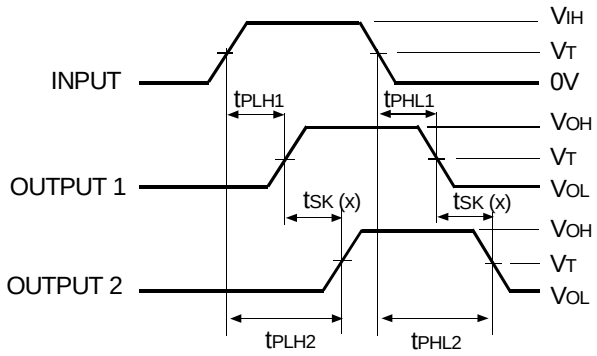
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

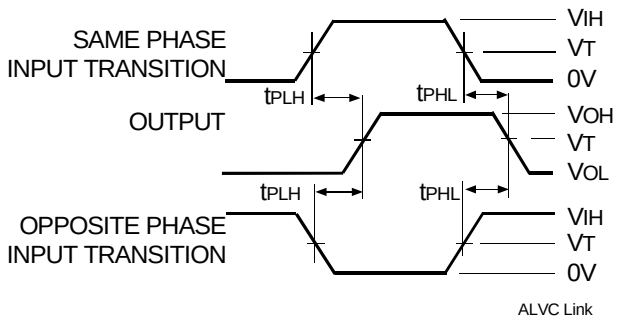


$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

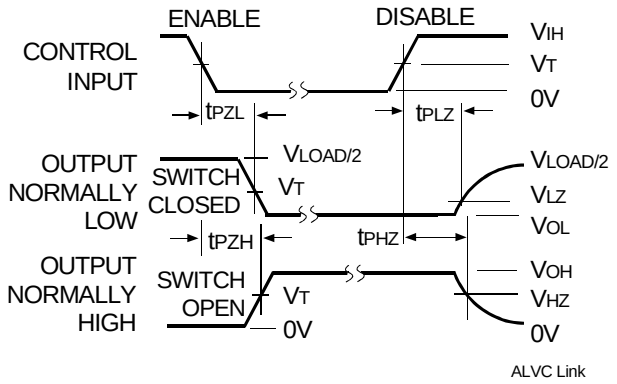
Output Skew - $t_{SK(x)}$

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



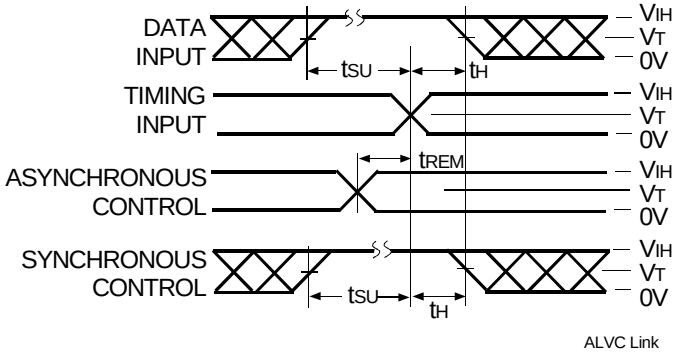
Propagation Delay



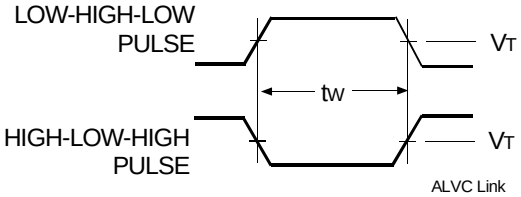
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

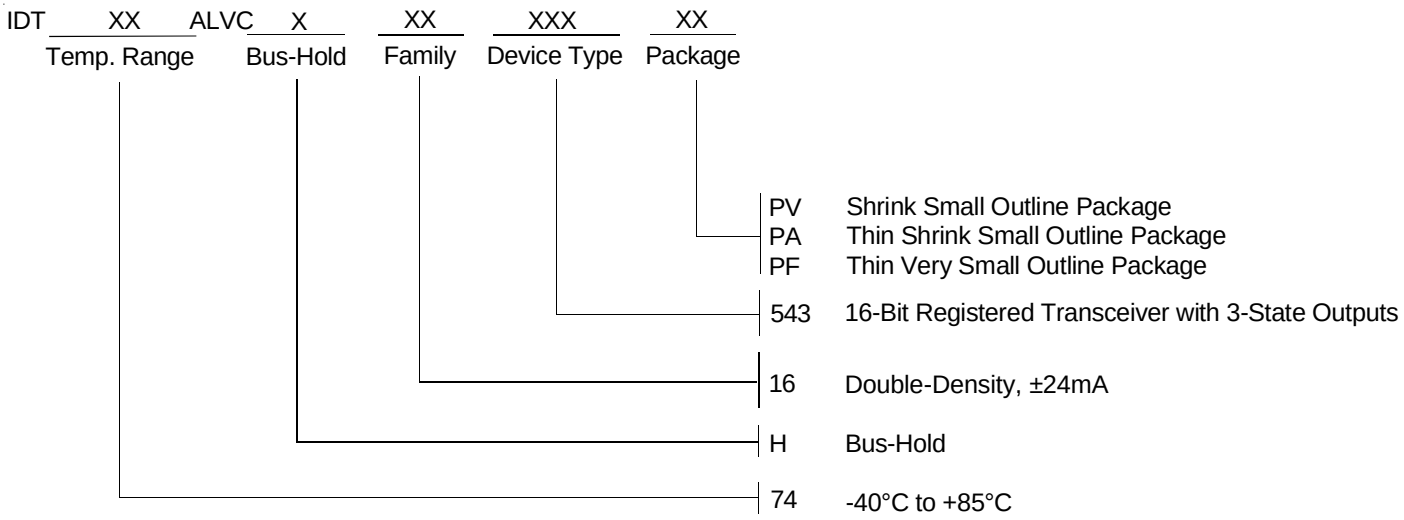


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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