



## 3.3V CMOS 10-BIT FLIP-FLOP WITH DUAL 3-STATE OUTPUTS

IDT74ALVC16820

### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 $\mu$  W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Suitable for heavy loads

### APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

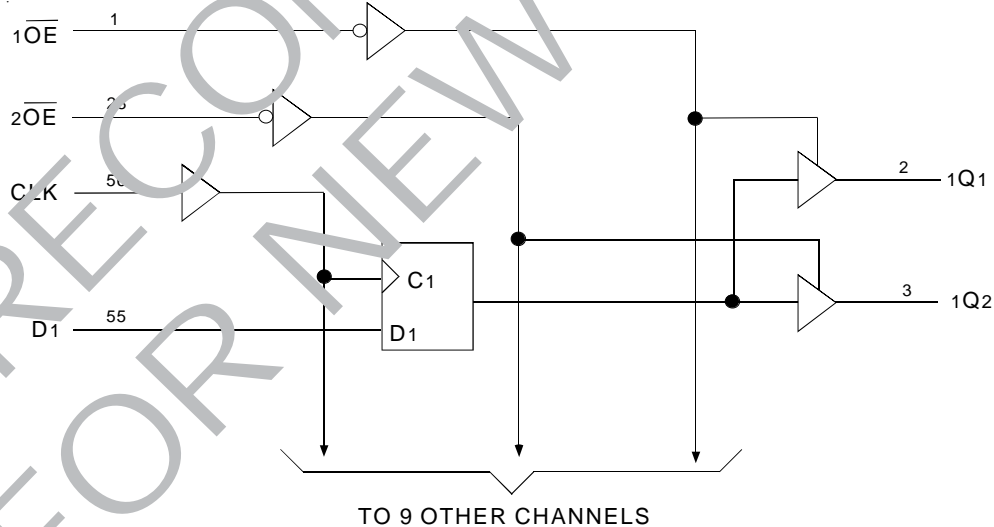
### DESCRIPTION:

This 10-bit flip-flop is built using advanced dual metal CMOS technology. The flip-flops of the ALVC16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

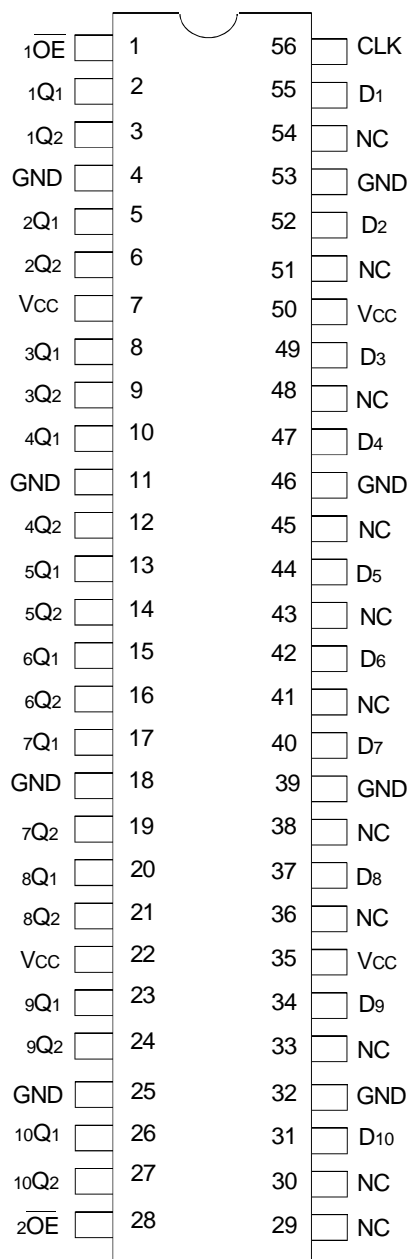
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components.  $\overline{OE}$  input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The ALVC16820 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > Vcc	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each Vcc or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>OUT</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
D <sub>x</sub>	Data Inputs
CLK	Clock Input
xQ <sub>x</sub>	3-State Outputs
$\overline{xOE}$	3-State Output Enable Inputs (Active LOW)

## FUNCTION TABLE (EACH FLIP-FLOP)<sup>(1)</sup>

Inputs			Outputs
$\overline{xOE}$	CLK	D <sub>x</sub>	xQ <sub>x</sub>
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub> <sup>(2)</sup>
H	X	X	Z

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance  
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V		—	—	±10	μA
		V <sub>O</sub> = GND		—	—	±10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	40	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	μA

**NOTE:**

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3V		2.4	—	
		V <sub>CC</sub> = 3V	I <sub>OH</sub> = -24mA	2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 24mA	—	0.55	

**NOTE:**

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range.  
T<sub>A</sub> = -40°C to +85°C.

OPERATING CHARACTERISTICS,  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per Flip-Flop Outputs enabled	$C_L = 0\text{pF}$ , $f = 10\text{MHz}$	60	63	pF
CPD	Power Dissipation Capacitance per Flip-Flop Outputs disabled		38	46	

SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 3.3V \pm 0.15V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLK to xQx	1	5.9	—	5.5	—	4.5	1	4	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}x$ to xQx	1	6.4	—	6.1	—	5.7	1	5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}x$ to xQx	1	5.7	—	5	—	4.5	1.3	4.5	ns
$t_w$	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	3.3	—	ns
$t_{SU}$	Set-up Time HIGH or LOW data before CLK $\uparrow$	1.7	—	1.8	—	1.4	—	1.4	—	ns
$t_H$	Hold Time HIGH or LOW data before CLK $\uparrow$	1.1	—	1.1	—	1	—	1	—	ns
$t_{SK(O)}$	Output Skew <sup>(2)</sup>	—	—	—	—	—	—	—	500	ps

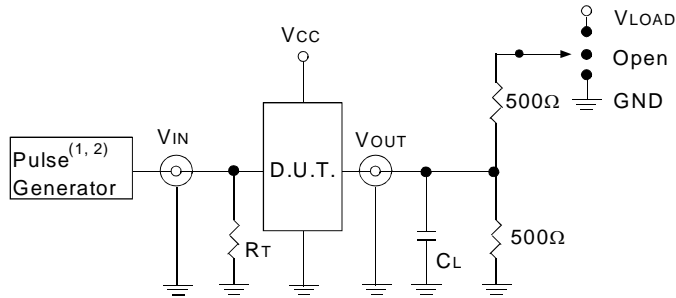
NOTES:

- See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ± 0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

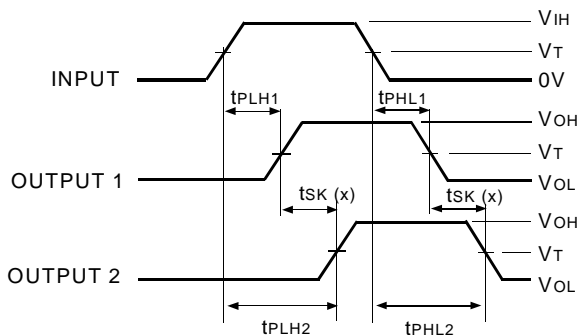
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

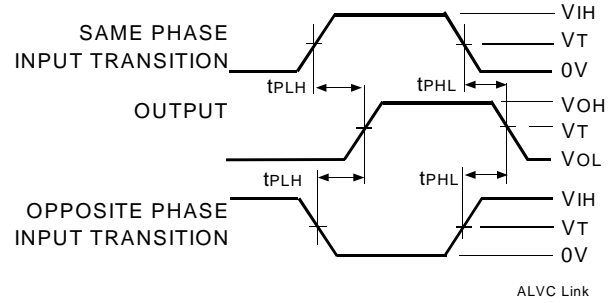


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

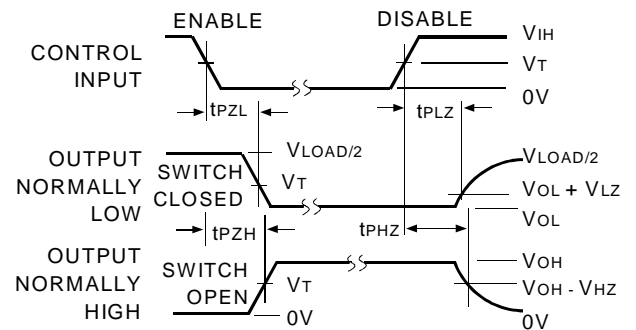
Output Skew - tsk(x)

#### NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



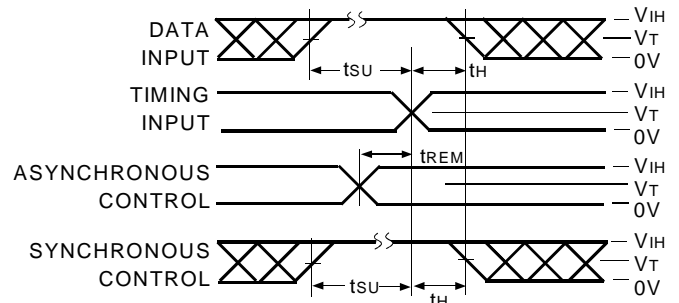
Propagation Delay



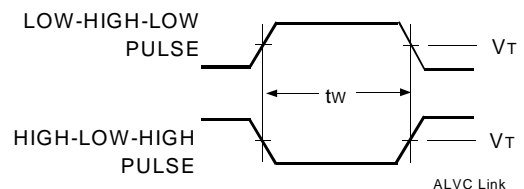
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

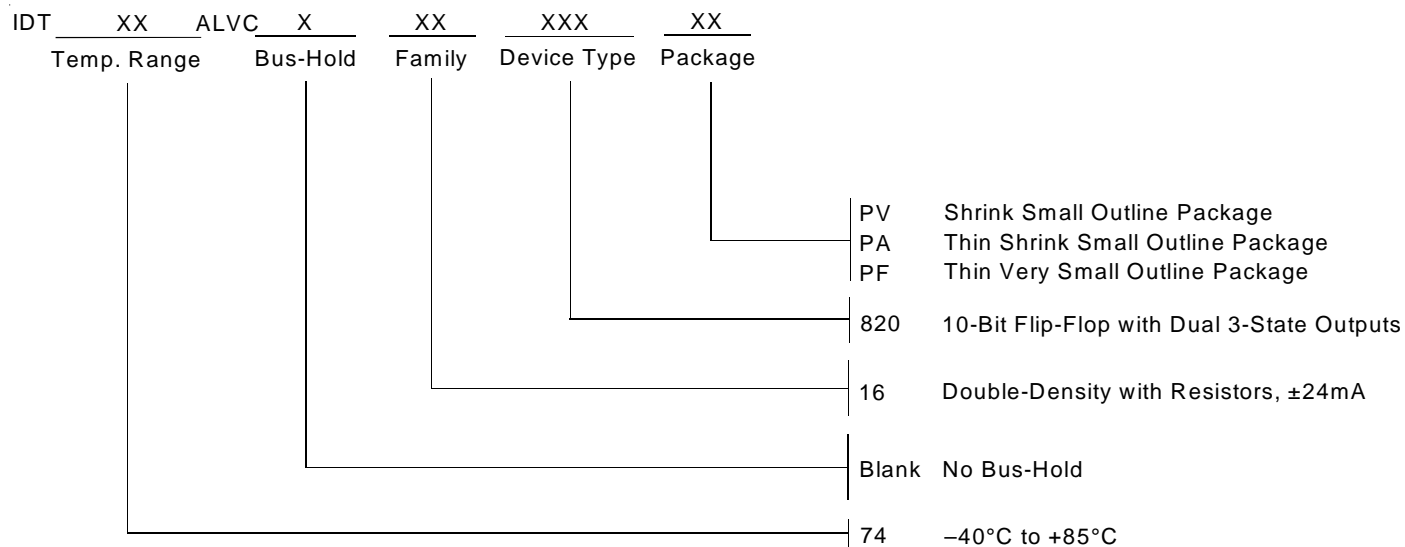


Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
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