



Integrated Device Technology, Inc.

# FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299T/AT/CT

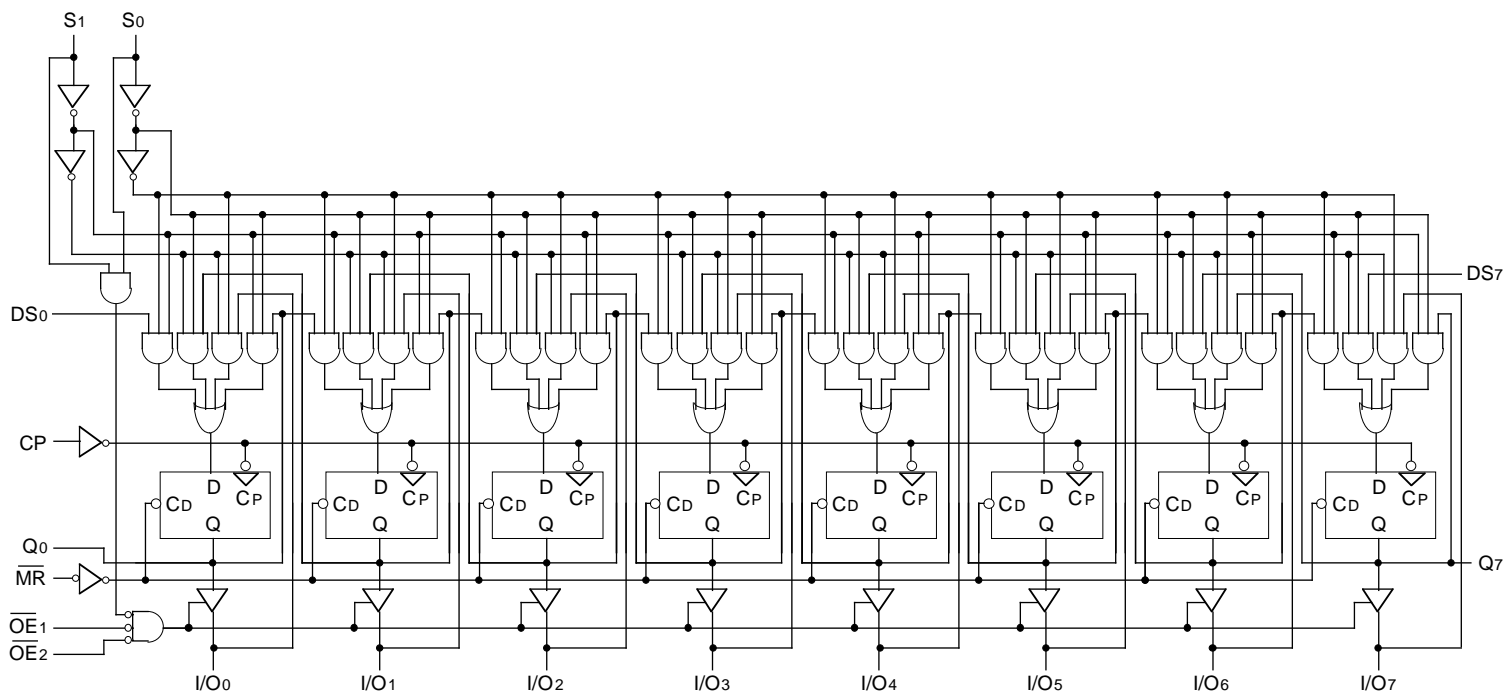
## FEATURES:

- Std., A and C speed grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- High drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

## DESCRIPTION:

The IDT54/74FCT299T/AT/CT are built using an advanced dual metal CMOS technology. The IDT54/74FCT299T/AT/CT are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

## FUNCTIONAL BLOCK DIAGRAM



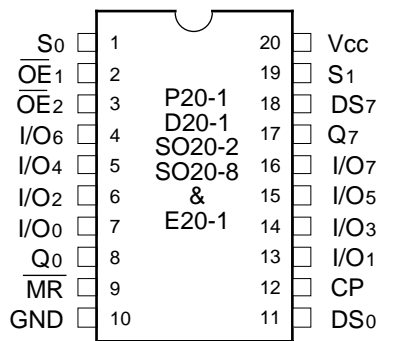
2632 drw 01

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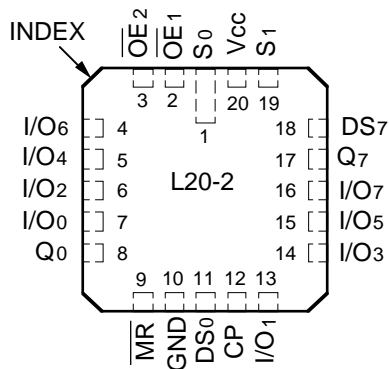
**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**APRIL 1995**

## PIN CONFIGURATIONS



2632 drw 02  
**DIP/SOIC/QSOP/CERPACK  
TOP VIEW**



2632 drw 03  
**LCC  
TOP VIEW**

## PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
MR	Asynchronous Master Reset Input (Active LOW)
OE1, OE2	3-State Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or 3-State Parallel Outputs
O0, O7	Serial Outputs

2632 tbl 01

## FUNCTION TABLE<sup>(1)</sup>

Inputs				Response
MR	S1	S0	CP	
L	X	X	X	Asynchronous Reset Q0–Q7 = LOW
H	H	H	↑	Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↑	Shift Right; DS0 → Q0, Q0 → Q1, etc.
H	H	L	↑	Shift Left; DS7 → Q7, Q7 → Q6, etc.
H	L	L	X	Hold

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH clock transition

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	–0.5 to V <sub>CC</sub> + 0.5	–0.5 to V <sub>CC</sub> + 0.5	V
T <sub>A</sub>	Operating Temperature	0 to +70	–55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	–55 to +125	–65 to +135	°C
T <sub>STG</sub>	Storage Temperature	–55 to +125	–65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	–60 to +120	–60 to +120	mA

**NOTES:**

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Input and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

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## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$	
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$	
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	—	—	$\pm 1$	$\mu\text{A}$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18\text{mA}$	—	-0.7	-1.2	V	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}$	-60	-120	-225	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$	
$V_H$	Input Hysteresis	—	—	200	—	mV	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$	—	0.01	1	mA	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .
- This parameter is guaranteed but not tested.

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## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1 = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7 = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7 = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.0	16.3 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ , +25°C ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Output Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

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## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT299T				IDT54/74FCT299AT				IDT54/74FCT299CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CP to Q0 or Q7	CL = 50pF RL = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPLH tPHL	Propagation Delay CP to I/On		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPHL	Propagation Delay MR to Q0 or Q7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
tPHL	Propagation Delay MR to I/On		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
tPZH tPZL	Output Enable Time OEn to I/On		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time OEn to I/On		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
tsu	Set-up Time HIGH or LOW S0 or S1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
tsu	Set-up Time HIGH or LOW I/On, DS0 or DS7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
th	Hold Time HIGH or LOW S0 or S1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
th	Hold Time HIGH or LOW I/On, DS0 or DS7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tw	MR Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tREM	Recovery Time		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

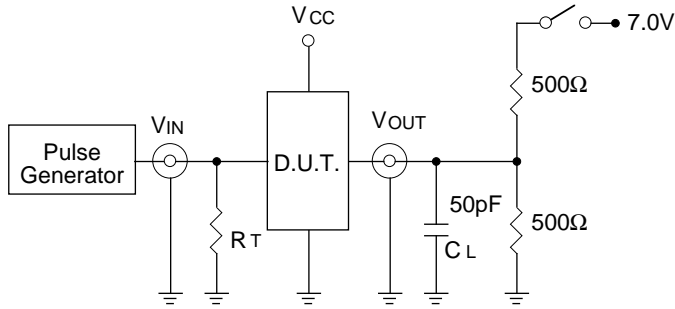
**NOTES:**

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

2619 tbl 07

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



2632 drw 04

### SWITCH POSITION

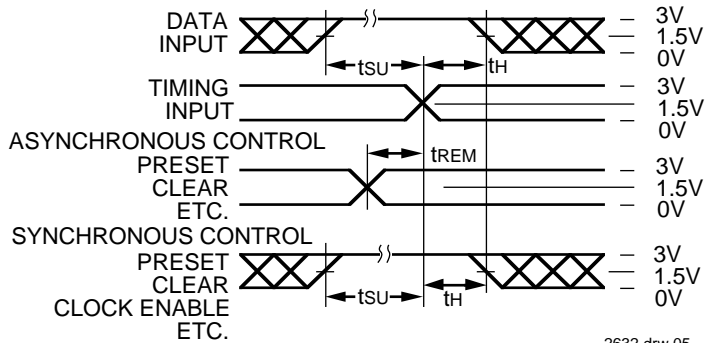
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

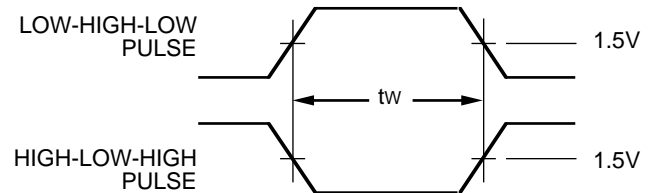
2632 Ink 08

### SET-UP, HOLD AND RELEASE TIMES



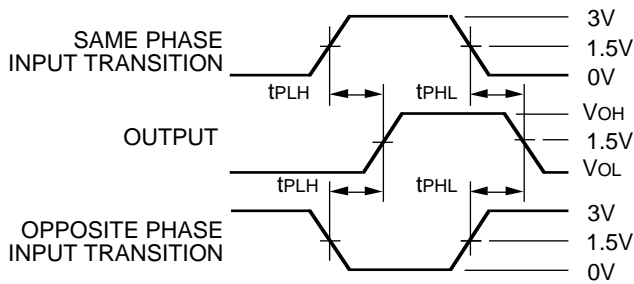
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### PULSE WIDTH



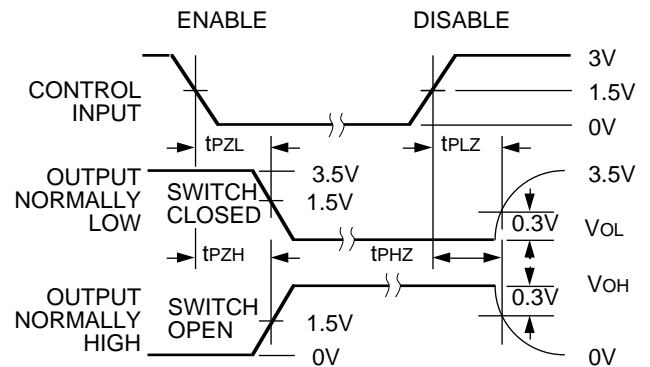
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### PROPAGATION DELAY



2632 drw 07

### ENABLE AND DISABLE TIMES

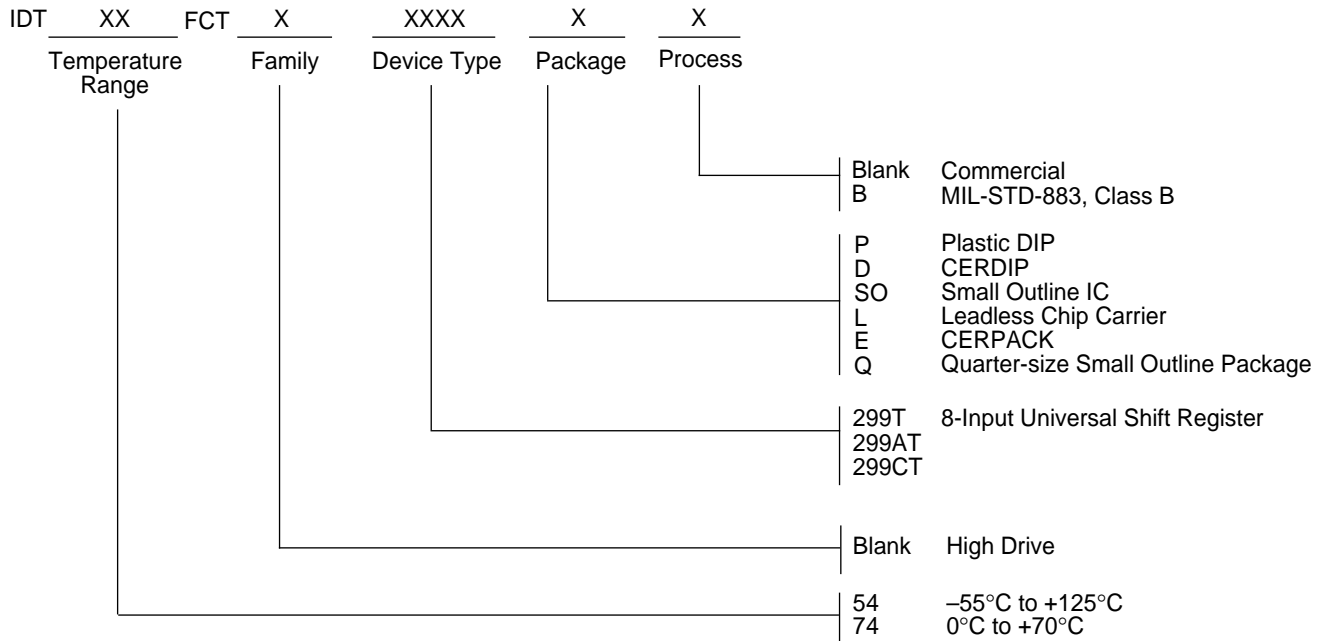


2632 drw 08

#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

**ORDERING INFORMATION**



2632 drw 09