



Integrated Device Technology, Inc.

# FAST CMOS 18-BIT REGISTER

## IDT54/74FCT16823AT/BT/CT/ET IDT54/74FCT162823AT/BT/CT/ET

### FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical  $t_{sk(o)}$  (Output Skew) < 250ps**
  - **Low input and output leakage  $\leq 1\mu A$  (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
  - Extended commercial range of -40°C to +85°C
  - $V_{CC} = 5V \pm 10\%$
- **Features for FCT16823AT/BT/CT/ET:**
  - High drive outputs (-32mA IOH, 64mA IOL)
  - Power off disable outputs permit "live insertion"
  - Typical VOLP (Output Ground Bounce) < 1.0V at  $V_{CC} = 5V, T_A = 25^\circ C$
- **Features for FCT162823AT/BT/CT/ET:**
  - Balanced Output Drivers:  $\pm 24mA$  (commercial),  $\pm 16mA$  (military)
  - Reduced system switching noise
  - Typical VOLP (Output Ground Bounce) < 0.6V at  $V_{CC} = 5V, T_A = 25^\circ C$

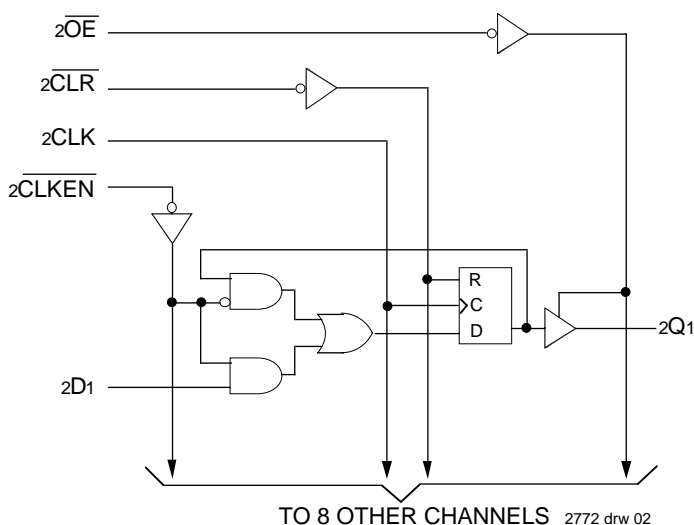
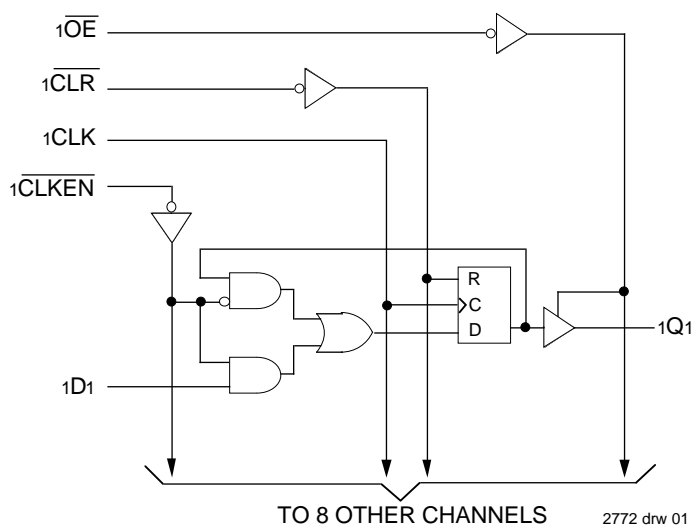
### DESCRIPTION:

The FCT16823AT/BT/CT/ET and FCT162823AT/BT/CT/ET 18-bit bus interface registers are built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable (xCLKEN) and clear (xCLR) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16823AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162823AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The FCT162823AT/BT/CT/ET are plug-in replacements for the FCT16823AT/BT/CT/ET and ABT16823 for on-board interface applications.

### FUNCTIONAL BLOCK DIAGRAM

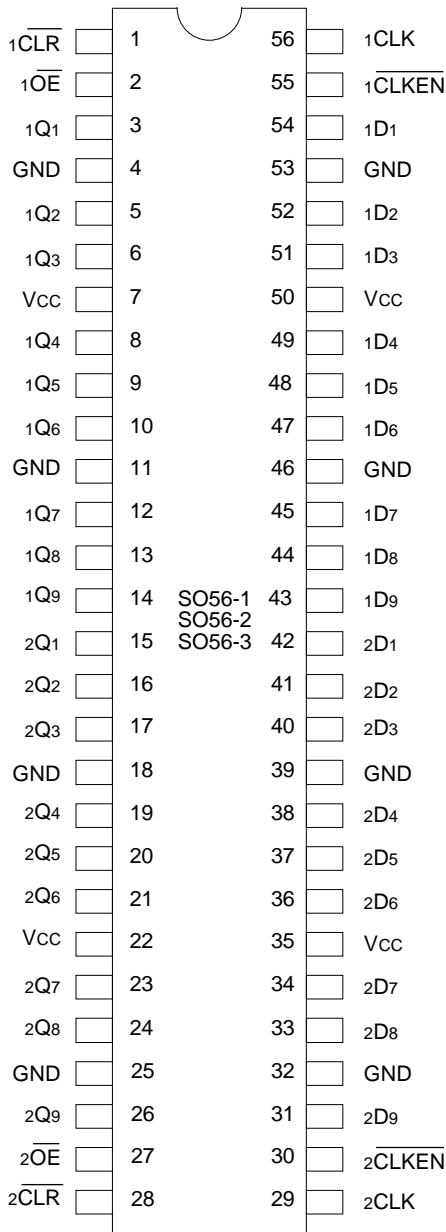


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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

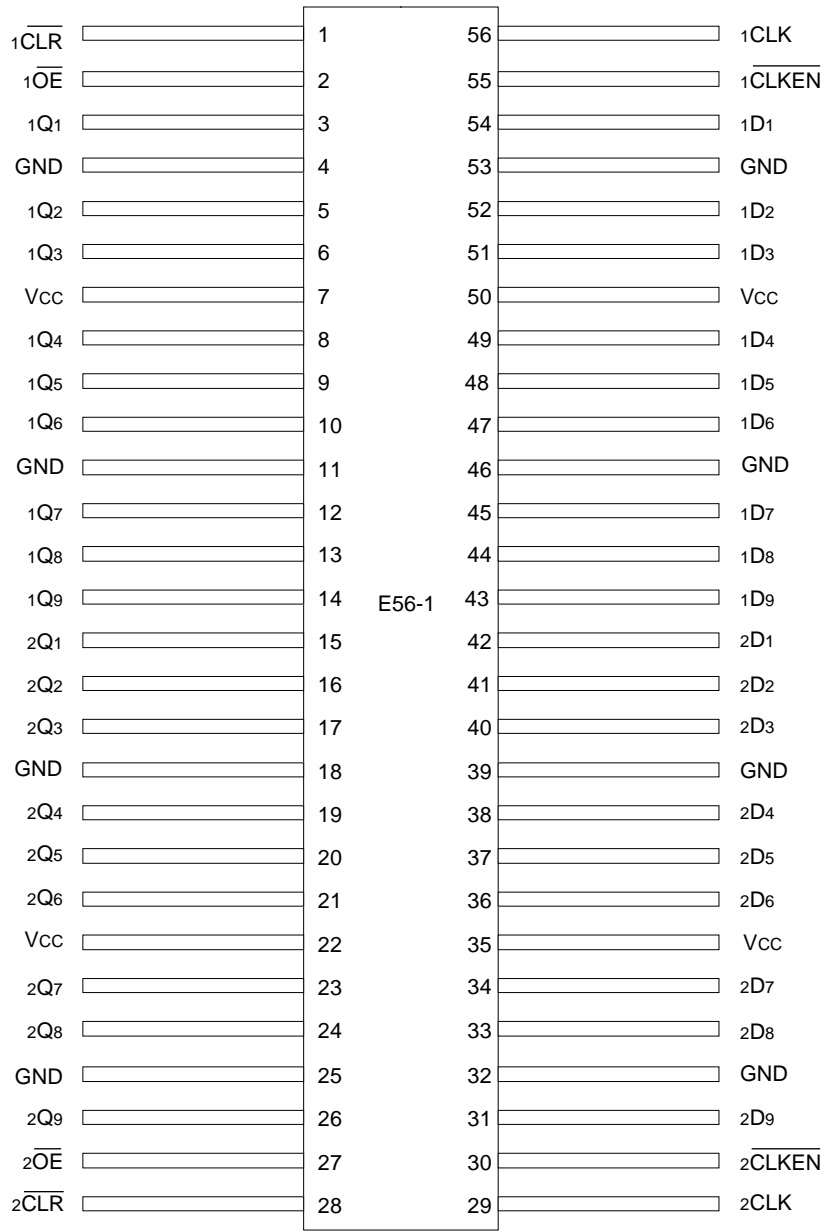
**AUGUST 1996**

**PIN CONFIGURATIONS**



**SSOP/  
TSSOP/TVSOP  
TOP VIEW**

2772 drw 03



**CERPACK  
TOP VIEW**

2772 drw 04

## PIN DESCRIPTION

Pin Names	Description
xDx	Data inputs
xCLK	Clock Inputs
$\overline{\text{xCLKEN}}$	Clock Enable Inputs (Active LOW)
$\overline{\text{xCLR}}$	Asynchronous clear Inputs (Active LOW)
$\overline{\text{xOE}}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

2772 tbl 01

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

2772 Ink 03

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

## FUNCTION TABLE<sup>(1)</sup>

Inputs					Outputs	Function
$\overline{\text{xOE}}$	$\overline{\text{xCLR}}$	$\overline{\text{xCLKEN}}$	xCLK	xDx	xQx	
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q <sup>(2)</sup>	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

2772 tbl 02

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance
- Output level before indicated steady-state input conditions were established.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	3.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	3.5	8.0	pF

2772 Ink 04

### NOTE:

- This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ ; Military:  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{iL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_i = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_o = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-225	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

2772 Ink 05

## OUTPUT DRIVE CHARACTERISTICS FOR FCT16823T

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_O$	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}^{(4)}$	2.0	3.0	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_o \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

2772 Ink 06

## OUTPUT DRIVE CHARACTERISTICS FOR FCT162823T

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	200	mA
$I_{ODH}$	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}, +25^{\circ}\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

2772 Ink 07

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \overline{xCLKEN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \overline{xCLKEN} = \text{GND}$ at $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \overline{xCLKEN} = \text{GND}$ at $f_i = 2.5\text{MHz}$ 50% Duty Cycle Eighteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	4.2	7.1 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	9.2	22.1 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC}$  = Quiescent Current ( $I_{CCL}$ ,  $I_{CCH}$  and  $I_{CCZ}$ )  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $N_{CP}$  = Number of Clock Inputs at  $f_{CP}$   
 $f_i$  = Input Frequency  
 $N_i$  = Number of Inputs at  $f_i$

2772 tbl 08

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT16823AT/162823AT				FCT16823BT/162823BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		CL = 300pF <sup>(5)</sup> RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
tPHL	Propagation Delay xCLR to xQx	CL = 50pF RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
tPZH tPZL	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF <sup>(5)</sup> RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time xOE to xQx	CL = 5pF <sup>(5)</sup> RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	
tsu	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW xDx to xCLK		2.0	—	2.0	—	1.5	—	1.5	—	ns
tsu	Set-up Time HIGH or LOW xCLKEN to xCLK		4.0	—	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW xCLKEN to xCLK		2.0	—	2.0	—	0	—	0	—	ns
tw	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
tw	xCLR Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time xCLR to xCLK		6.0	—	7.0	—	6.0	—	6.0	—	ns
tsk(o)	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	—	0.5	ns

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

2772 tbl 09

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT16823CT/162823CT				FCT16823ET/162823ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.4	—	—	ns
		CL = 300pF <sup>(5)</sup> RL = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	—	—	
tPHL	Propagation Delay xCLR to xQx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	4.4	—	—	ns
tPZH tPZL	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
		CL = 300pF <sup>(5)</sup> RL = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time xOE to xQx	CL = 5pF <sup>(5)</sup> RL = 500Ω	1.5	6.2	1.5	6.2	1.5	3.6	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.5	1.5	6.5	1.5	3.6	—	—	
tsu	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	3.0	—	3.0	—	1.5	—	—	—	ns
th	Hold Time HIGH or LOW xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
tsu	Set-up Time HIGH or LOW xCLKEN to xCLK		3.0	—	3.0	—	2.5	—	—	—	ns
th	Hold Time HIGH or LOW xCLKEN to xCLK		0	—	0	—	0.0	—	—	—	ns
tw	xCLK Pulse Width HIGH or LOW		6.0	—	6.0	—	3.0 <sup>(4)</sup>	—	—	—	ns
tw	xCLR Pulse Width LOW		6.0	—	6.0	—	3.0 <sup>(4)</sup>	—	—	—	ns
tREM	Recovery Time xCLR to xCLK		6.0	—	6.0	—	3.0	—	—	—	ns
tsk(o)	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	—	—	ns

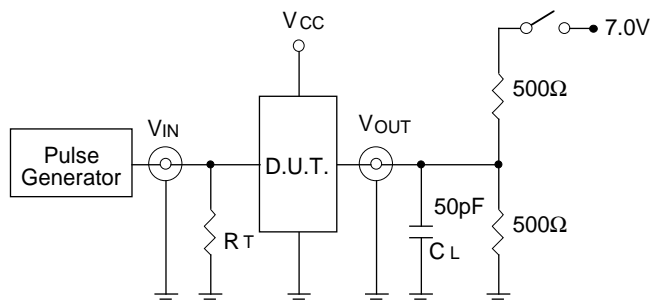
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

2772 tbl 10

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



2772 drw 05

### SWITCH POSITION

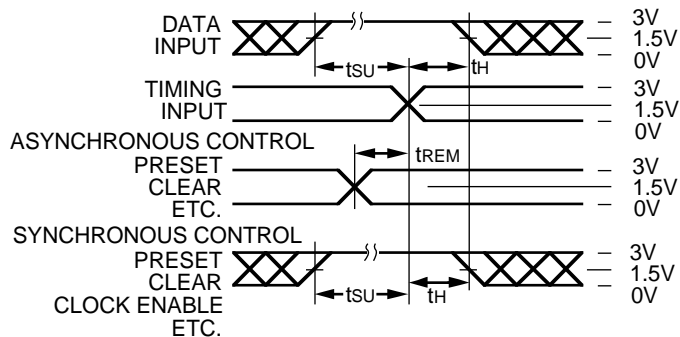
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

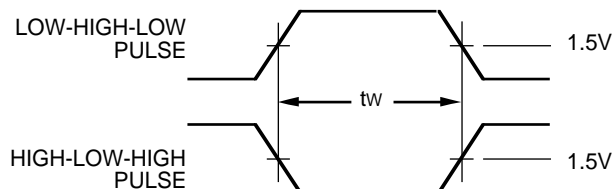
2772 Ink 10

### SET-UP, HOLD AND RELEASE TIMES



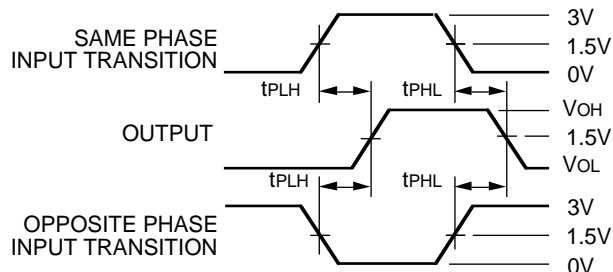
2772 drw 06

### PULSE WIDTH



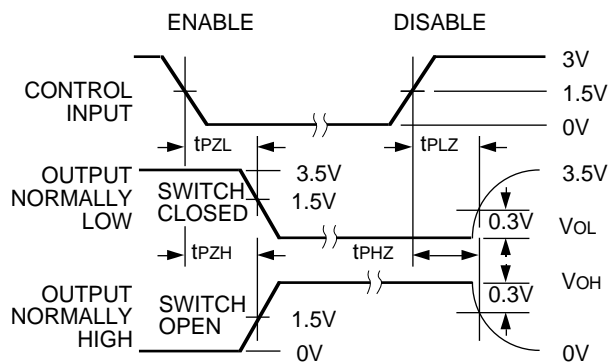
2772 drw 07

### PROPAGATION DELAY



2772 drw 08

### ENABLE AND DISABLE TIMES



2772 drw 09

#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$



**ORDERING INFORMATION**

IDT	XX	FCT	XXXX	X	X	
Temp. Range		Device Type		Package	Process	
						Blank B
						Commercial MIL-STD-883, Class B
						PV
						Shrink Small Outline Package (SO56-1)
						PA
						Thin Shrink Small Outline Package (SO56-2)
						PF
						Thin Very Small Outline Package (SO56-3)
						E
						CERPACK (E56-1)
						16823AT
						Non-Inverting 18-Bit Register
						16823BT
						16823CT
						16823ET
						162823AT
						162823BT
						162823CT
						162823ET
						54
						-55°C to +125°C
						74
						-40°C to +85°C

2772 drw 10