

20-BIT BUS SWITCH

FEATURES:

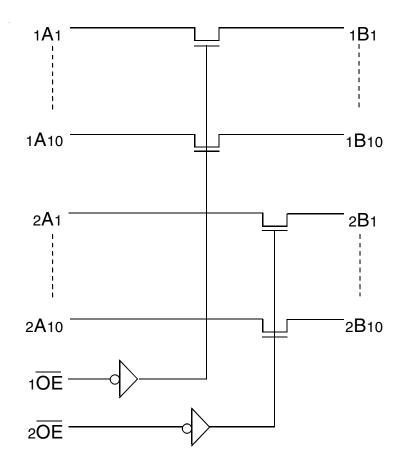
- · Bus switches provide zero delay paths
- Low switch on-resistance
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- · Hot insertion capability
- · Very low power dissipation
- · Available in SSOP and TSSOP packages

DESCRIPTION:

The FST163210 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no VCC applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

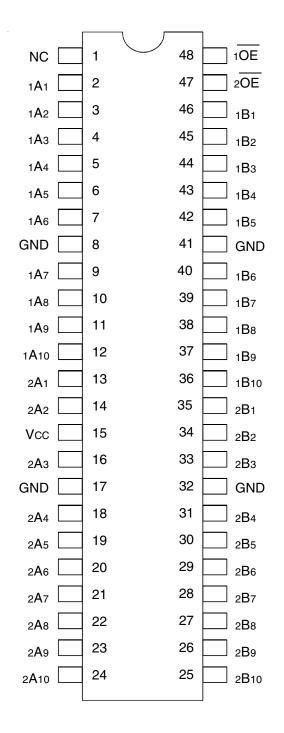
FUNCTIONAL BLOCK DIAGRAM



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IDT74FST163210 20-BIT BUS SWITCH

PINCONFIGURATION



SSOP/ TSSOP TOP VIEW

INDUSTRIAL TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	–0.5 to +7	V
Tstg	Storage Temperature	-65 to +150	°C
Ιουτ	Maximum Continuous Channel Current	128	mA

NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Vcc, Control, and Switch terminals.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Тур.	Unit
CIN	Control Input Capacitance		6	рF
Ci/o	Switch Input/Output Capacitance	Switch Off	12	pF

NOTES:

1. Capacitance is characterized but not tested.

2. TA = 25° C, f = 1MHz, VIN = 0V, VOUT = 0V.

PIN DESCRIPTION

Pin Names	I/O	Description
xAx	I/O	Bus A
xBx	I/O	Bus B
xŌĒ		Switch Enable

FUNCTION TABLE⁽¹⁾

1 OE	2 0E	1 A , 1 B	2A, 2B	Description
L	L	1A = 1B	2A = 2B	Connect
L	Н	1A = 1B	Z	Bank 1 Connect
Н	L	Z	2A = 2B	Bank 2 Connect
Н	Н	Z	Z	Disconnect

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

 $\label{eq:conditions} Following \ Conditions \ Apply \ Unless \ Otherwise \ Specified:$

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = 5.0V $\pm 10\%$

Symbol	Parameter	Test Con	ditions ⁽¹⁾	Min.	Тур.(2)	Max.	Unit
Vih	Control Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2	_	_	V
VIL	Control Input LOW Voltage	Guaranteed Logic LOW for Cont	Guaranteed Logic LOW for Control Inputs		—	0.8	V
Іін	Control Input HIGH Current	Vcc = Max.	VI = VCC	-	_	±1	μA
lıL	Control Input LOW Current		VI = GND	_	—	±1	
Іогн	Current During	Vcc = Max., Vo = 0 to 5V		-	—	±1	μA
Iozl	Bus Switch Disconnect			_	—	±1	
Vik	Clamp Diode Voltage	Vcc = Min., IIN = -18mA		_	-0.7	-1.2	V
IOFF	Switch Power Off Leakage	Vcc = 0V, VIN or Vo ≤ 5.5 V		_	_	±1	μA
Icc	Quiescent Power Supply Current	Vcc = Max., VIN = GND or Vcc		-	0.1	3	μA

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

 $Following \, Conditions \, Apply \, Unless \, Otherwise \, Specified:$

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = $5.0V \pm 10\%$

Symbol	Parameter	Test Conditions	Min.	Тур. ⁽¹⁾	Max.	Unit
		Vcc = Min., $Vin = 0V$, $Ion = 64mA$	_	5	7	
Ron	Ron Switch On Resistance ⁽²⁾	Vcc = Min., VIN = 0V, ION = 30mA	_	5	7	Ω
		Vcc = Min., Vin = 2.4V, Ion = 15mA	_	8	15	
los	Short Circuit Current, A to B ⁽³⁾	A(B) = 0V, B(A) = Vcc	100	_	_	mA

NOTES:

1. Typical values are at Vcc = 5.0V, +25°C ambient.

2. The voltage drop between the indicated ports divided by the current through the switch.

3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
Δlcc	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = Max.$ $V_{IN} = 3.4V^{(3)}$		_	0.5	1.5	mA
ICCD	Dynamic Power Supply Current ^(4,5)	Vcc = Max. One Enable Pin Toggling 50% Duty Cycle	VIN = VCC VIN = GND		120	160	μΑ/ MHz/ Switch
Ic	Total Power Supply Current ⁽⁶⁾	Vcc = Max. One Enable Pin Toggling	VIN = VCC VIN = GND	-	1.2	1.6	mA
		fi = 10MHz 50% Duty Cycle	VIN = 3.4V VIN = GND	_	1.5	2.4	
		Vcc = Max. Two Enable Pins Toggling	VIN = VCC VIN = GND	_	2.4	3.2	
		fi = 10MHz 50% Duty Cycle	VIN = 3.4V VIN = GND	_	2.9	4.7	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type. TA = -40°C to +85°C

2. Typical values are at Vcc = 5.0V, +25°C ambient.

3. Per TTL driven input (VIN = 3.4V). All other inputs at Vcc or GND. Switch inputs do not contribute to Δ Icc.

4. This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency.

Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. 5. CPD = IccD/Vcc

- CPD = Power Dissipation Capacitance
- 6. IC = IQUIESCENT + INPUTS + IDYNAMIC
- $IC = ICC + \Delta ICC DHNT + ICCD (fiN)$
- Icc = Quiescent Current
- Δ Icc = Power Supply Current for a TTL High Input (VIN = 3.4V)
- DH = Duty Cycle for TTL Inputs High
- $N \tau$ = Number of TTL Inputs at $D \ensuremath{\mathsf{H}}$
- ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
- fi = Control Input Frequency
- N = Number of Control Inputs Toggling at fi

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = $5.0V \pm 10\%$

			$Vcc = 5V \pm 10\%$		Vcc = 4V	
Symbol	Description ⁽¹⁾	Min.	Тур.	Max.	Max.	Unit
t PLH	Data Propagation Delay	_	—	0.25	0.25	ns
t PHL	A to B, B to A ⁽²⁾					
tрzн	Switch CONNECT Delay	1.5	—	6.5	—	ns
tpzl	xOE to A or B					
tрнz	Switch DISCONNECT Delay	1.5	—	5.5	—	ns
t PLZ	xOE to A or B					
Qci	Charge Injection During Switch DISCONNECT	_	1.5	—	—	рС
	$x\overline{OE}$ to A or $B^{(3)}$					

NOTES:

1. See test circuits and waveforms.

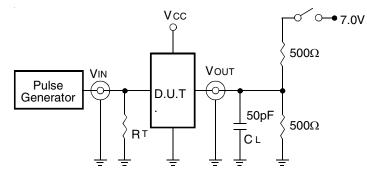
2. The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.

3. |Qci| is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers. |Qbci| is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

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INDUSTRIAL TEMPERATURE RANGE

TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs

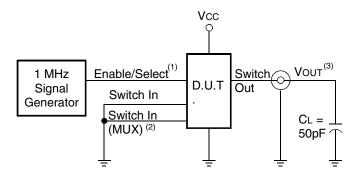
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

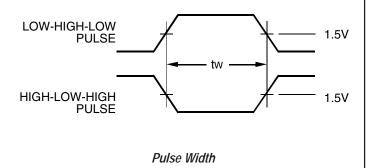
CL = Load capacitance: includes jig and probe capacitance.

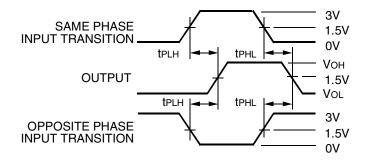
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



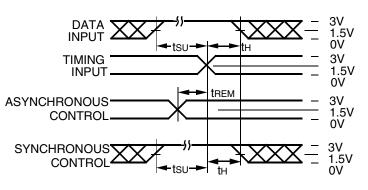
Charge Injection

- NOTES:
- 1. Select is used with multiplexers for measuring IQDCII during multiplexer select. During all other tests Enable is used.
- 2. Used with multiplexers to measure IQDCII only.
- 3. Charge Injection = Δ Vout CL, with Enable toggling for IQcII or Select toggling for IQDCII. Δ Vout is the change in Vout and is measured with a 10M Ω probe.

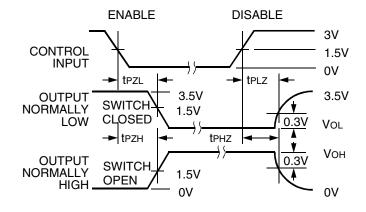




Propagation Delay



Set-up, Hold, and Release Times



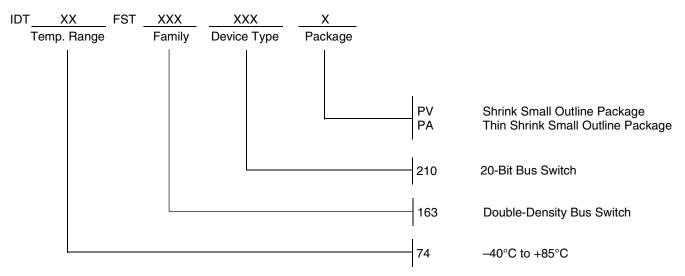
Enable and Disable Times

NOTES:

- 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- 2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; tr \leq 2.5ns; tr \leq 2.5ns.

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ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

5/21/2002 Removed TVSOP package



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