MICROCLOCK

MK2761
Set-Top Clock Source

Description

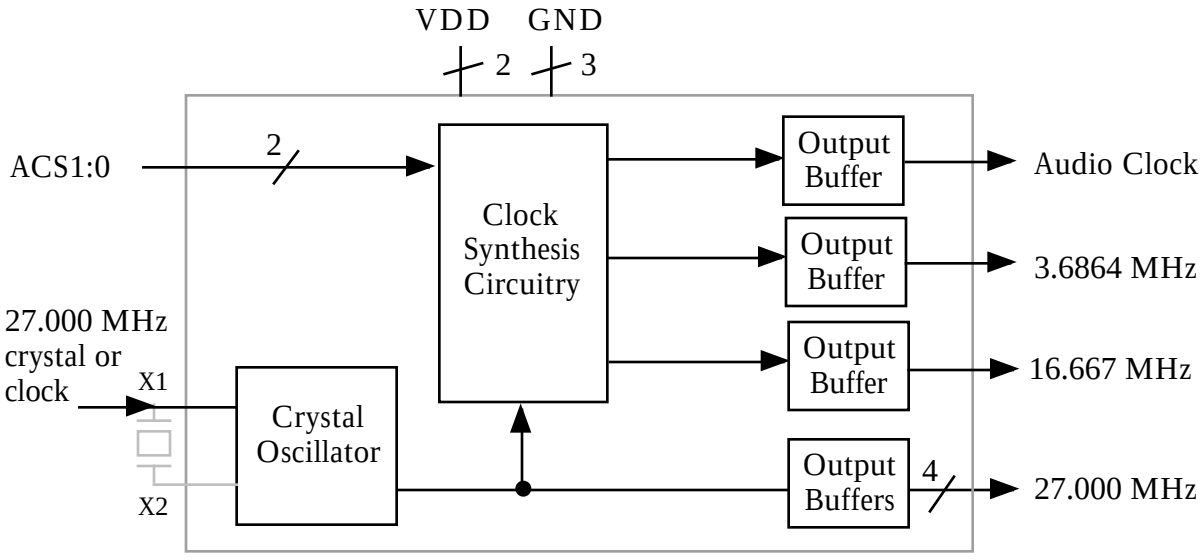
The MK2761 is a low cost, low jitter, high performance clock synthesizer designed for set-top boxes. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 27.00MHz crystal or clock input to produce multiple output clocks including the processor clock, the UART clock, a selectable audio clock, and four low skew copies of the 27MHz. The audio clocks are exactly frequency locked to the 27.00MHz input with zero ppm error, allowing audio and video to track exactly.

MicroClock manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult MicroClock to eliminate crystals and oscillators from your board.

Features

- Packaged in 16 pin narrow (150 mil) SOIC
- Selectable audio sampling frequencies support 32 kHz, 44.1 kHz, and 48 kHz in most DACs
- 27.00 MHz crystal or clock input
- Processor frequency of 16.67MHz
- Zero ppm error in audio clocks exactly track video frequency
- 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 5V±10% operating voltage

Block Diagram



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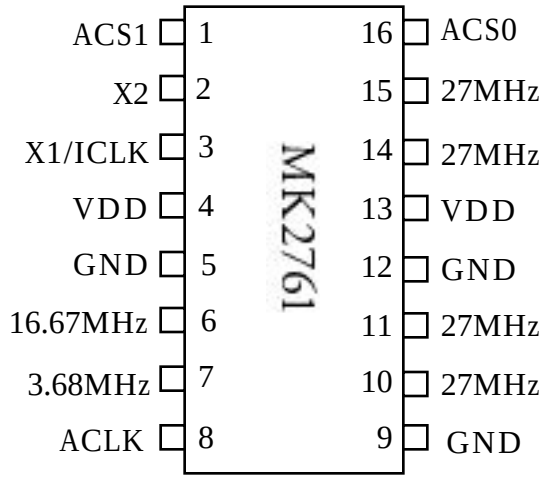
Pin Assignment



16 pin narrow (150 mil) SOIC

ACS1	ACS0	ACLK (MHz)
0	0	8.192
0	1	11.2896
1	0	12.288
1	1	5.6448

Pin Descriptions

Number	Name	Type	Description
1	ACS1	I	Audio Clock Select 1. Selects ACLK on pin 8. See table above.
2	X2	O	Crystal connection. Connect to 27 MHz crystal. Leave unconnected for clock input.
3	X1/ICLK	I	Crystal connection. Connect to 27 MHz crystal or connect to 27 MHz input clock.
4	VDD	P	Connect to +5V.
5	GND	P	Connect to ground.
6	16.67M	O	16.667 MHz processor clock output.
7	3.68M	O	3.6864 MHz clock output.
8	ACLK	O	Audio Clock output. Determined by status of ACS1, ACS0. See table above.
9	GND	P	Connect to ground.
10	27M	O	27.00 MHz buffered reference clock output. Duty cycle matches input clock.
11	27M	O	27.00 MHz buffered reference clock output. Duty cycle matches input clock.
12	GND	P	Connect to ground.
13	VDD	P	Connect to +5V.
14	27M	O	27.00 MHz buffered reference clock output. Duty cycle matches input clock.
15	27M	O	27.00 MHz buffered reference clock output. Duty cycle matches input clock.
16	ACS0	I	Audio Clock Select 0. Selects audio clock on pin 8. See table above.

Key: I = Input, O = output, P = power supply connection

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless noted)					
Operating Voltage, VDD		4.5		5.5	V
Input High Voltage, VIH, X1/ICLK pin only		3.5	2.5		V
Input Low Voltage, VIL, X1/ICLK pin only			2.5	1.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load, note 2		45		mA
Short Circuit Current	Each output		±100		mA
Input Capacitance			7		pF
Frequency error, ACLK				0	ppm
AC CHARACTERISTICS (VDD = 5.0V unless noted)					
Input Frequency			27.000		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At 1.4V	40		60	%
Maximum Absolute Jitter, short term			200		ps
Skew of 27 MHz outputs	Rising edges at 1.4V	-500	0	500	ps

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With ACLK at 12.28MHz.

External Components

The MK2761 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF should be connected between VDD and GND (pins 4 and 5, and 13 and 12), as close to the MK2761 as possible. A series termination resistor of 33Ω may be used for each clock output. If a clock input is not used, the 27.00 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode, parallel resonant, 50 ppm or better. Crystal capacitors should be connected from pins X1 to ground and X2 to ground. The value (in pF) of these crystal capacitors should be = $(C_L-4)*2$, where C_L is the crystal load capacitance in pF. So for a crystal with 16pF load capacitance, the crystal capacitors should be 24pF each.

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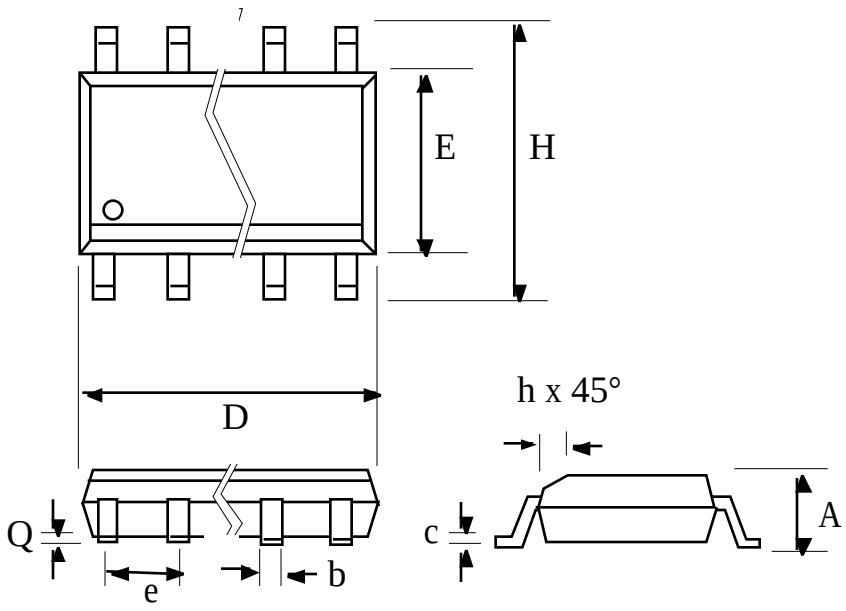
Package Outline and Package Dimensions

16 pin SOIC narrow



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.070	1.397	1.778
b	0.013	0.019	0.330	0.483
c	0.007	0.010	0.191	0.254
D	0.385	0.400	9.779	10.160
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.016		0.406
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2761S	MK2761S	tubes	16 pin SOIC	0-70°C
MK2761STR	MK2761S	tape and reel	16 pin SOIC	0-70°C