MK2049-35
3.3 V Communications Clock PLL

Description

The MK2049-35 is a Phase-Locked Loop (PLL) based clock synthesizer that accepts multiple input frequencies. With an 8 kHz clock input as a reference, the MK2049-35 generates T1, E1, T3, E3, OC3/3, Gigabit Ethernet, and other communications frequencies. This allows for the generation of clocks frequency-locked to an 8 kHz backplane clock, simplifying clock synchronization in communications systems.

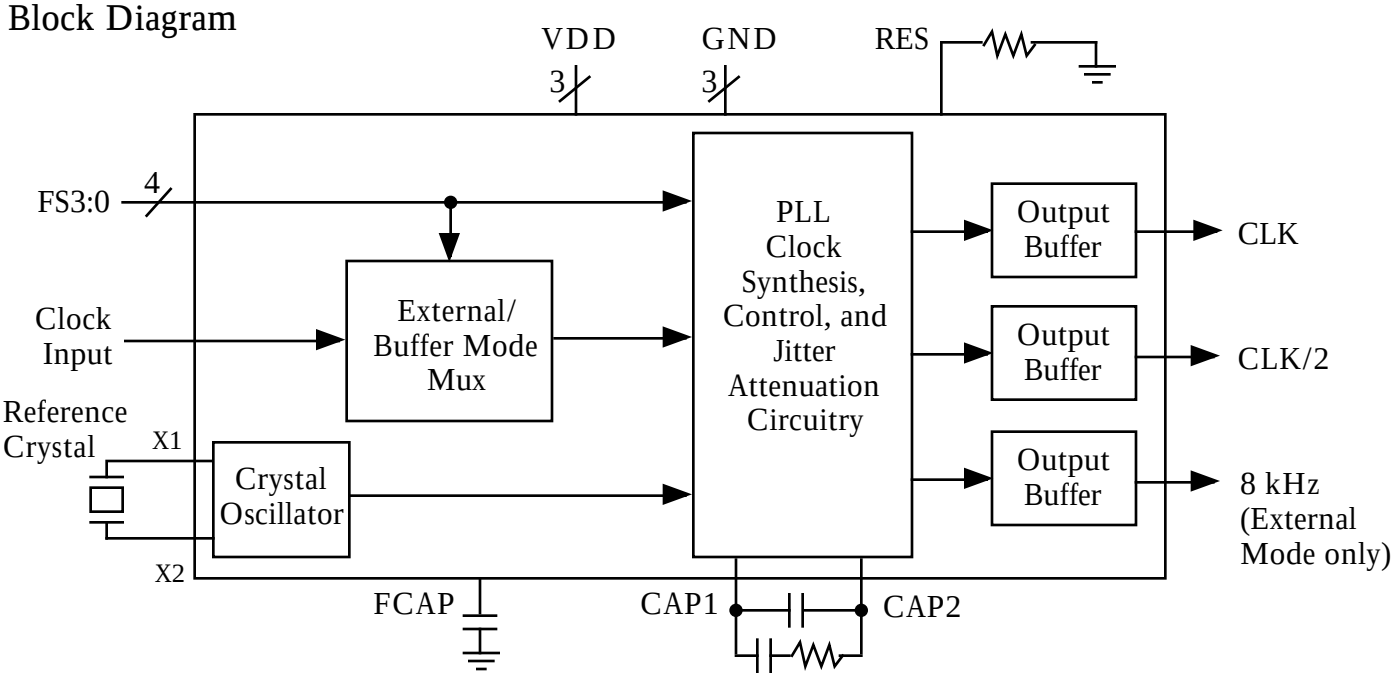
This part also has a jitter-attenuated Buffer capability. In this mode, the MK2049-35 is ideal for filtering jitter from with high jitter clocks.

ICS/MicroClock can customize these devices for many other different frequencies. Contact your ICS/MicroClock representative for more details.

Features

- Packaged in 20 pin SOIC
- 3.3 V ±5% operation
- Meets the TR62411, ETS300 011, and GR-1244 specification for MTIE, Pull-in/Hold-in Range, Phase Transients, and Jitter Generation for Stratum 3, 4, and 4E
- Accepts multiple inputs: 8 kHz backplane clock, or 10 to 50 MHz
- Locks to 8 kHz ±100 ppm (External mode)
- Buffer Mode allows jitter attenuation of 10-50 MHz input and x1/x0.5 or x1/x2 outputs
- Exact internal ratios enable zero ppm error
- Output clock rates include T1, E1, T3, E3, and OC3 submultiples
- See the MK2049-01, -02, and -03 for more selections at VDD = 5 V, and the MK2049-34 for more selections at 3.3 V

Block Diagram



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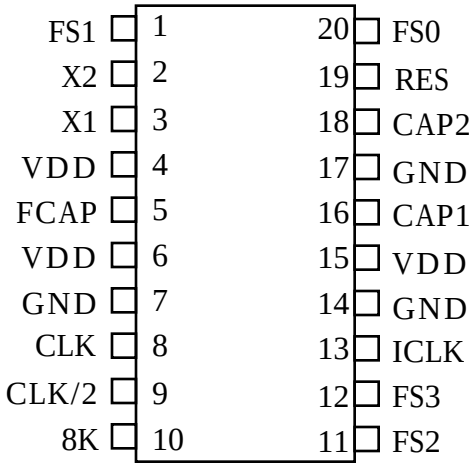
Pin Assignment



20 pin (300 mil) SOIC

Pin Descriptions

Number	Name	Type	Description
1	FS1	I	Frequency Select 1. Determines CLK input/outputs per tables on page 4.
2	X2	XO	Crystal connection. Connect to a MHz crystal as shown in the tables on page 4.
3	X1	XI	Crystal connection. Connect to a MHz crystal as shown in the tables on page 4.
4	VDD	P	Connect to +3.3V.
5	FCAP	-	Filter Capacitor. Connect a 1000 pF ceramic capacitor to ground.
6	VDD	P	Connect to +3.3V.
7	GND	P	Connect to ground.
8	CLK	O	Clock output determined by status of FS3:0 per tables on page 4.
9	CLK/2	O	Clock output determined by status of FS3:0 per tables on page 4. Always 1/2 of CLK.
10	8K	O	Recovered 8 kHz clock output.
11	FS2	I	Frequency Select 2. Determines CLK input/outputs per tables on page 4.
12	FS3	I	Frequency Select 3. Determines CLK input/outputs per tables on page 4.
13	ICLK	I	Input clock connection. Connect to 8 kHz backplane or MHz clock.
14	GND	P	Connect to ground.
15	VDD	P	Connect to +3.3V.
16	CAP1	LF	Connect the loop filter ceramic capacitors and resistor between this pin and CAP2.
17	GND	P	Connect to ground.
18	CAP2	LF	Connect the loop filter ceramic capacitors and resistor between this pin and CAP1.
19	RES	-	Connect a 10-200kΩ resistor to ground. Contact ICS applications dept. at 408-297-1201 for the recommended value for your app.
20	FS0	I	Frequency Select 0. Determines CLK input/outputs per tables on page 4.

Type: XI, XO = crystal connections, I = Input, O = output, P = power supply connection, LF = loop filter connections

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs		-0.5		VDD+0.5	V
Ambient Operating Temperature	MK2049-34SI	-40		85	°C
Soldering Temperature	Max of 10 seconds			250	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.15	3.3	3.45	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH, CMOS level	IOH=-4 mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-8 mA	2.4			V
Output Low Voltage	IOL=8 mA			0.4	V
Operating Supply Current, IDD	No Load, VDD=3.3 V		15		mA
Short Circuit Current	Each output		±50		mA
Input Capacitance, FS3:0			5		pF
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Frequency, External Mode	ICLK		8.000		kHz
Input Clock Pulse Width		10			ns
Propagation Delay	ICLK to 8 kHz		7		ns
Delay, CLK/2 after CLK			4		ns
Output Clock Rise Time	0.8 to 2.0 V			2	ns
Output Clock Fall Time	2.0 to 0.8 V			2	ns
Output Clock Duty Cycle, High Time	At VDD/2, except 8k	40		60	%
Actual mean frequency error versus target	Any clock selection		0	0	ppm

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

MK2049-35 Output Decoding Table – External Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK/2	CLK	8K	Crystal
8 kHz	0	0	0	0	1.544	3.088	8 kHz	24.576
8 kHz	0	0	0	1	2.048	4.096	8 kHz	24.576
8 kHz	0	0	1	0	22.368	44.736	8 kHz	24.576
8 kHz	0	0	1	1	17.184	34.368	8 kHz	24.576
8 kHz	0	1	0	0	19.44	38.88	8 kHz	19.44
8 kHz	0	1	0	1	12.8	25.6	8 kHz	25.6
8 kHz	0	1	1	0	25.92	51.84	8 kHz	17.28
8 kHz	0	1	1	1	4.096	8.192	8 kHz	16.384
8 kHz	1	0	0	0	18.528	37.056	8 kHz	24.704
8 kHz	1	0	0	1	12.352	24.704	8 kHz	24.704
8 kHz	1	0	1	0	24.576	49.152	8 kHz	16.384
8 kHz	1	0	1	1	16.384	32.768	8 kHz	16.384
8 kHz	1	1	0	0	17.28	34.56	8 kHz	17.28
8 kHz	1	1	0	1	62.5	125	8 kHz	25

MK2049-35 Output Decoding Table – Buffer Mode (MHz)

ICLK	FS3	FS2	FS1	FS0	CLK/2	CLK	8K	Crystal
20 - 50	1	1	1	0	ICLK	2*ICLK	N/A	ICLK/2
10 - 25	1	1	1	1	ICLK/2	ICLK	N/A	ICLK

- 0 = connect directly to ground, 1 = connect directly to VDD.
- Crystal is connected to pins 2 and 3; clock input is applied to pin 13.

OPERATING MODES

The MK2049-35 has two operating modes: External and Buffer. Although both modes use an input clock to generate various output clocks, there are important differences in their input and crystal requirements.

External Mode

The MK2049-35 accepts an external 8 kHz clock and will produce a number of common communication clock frequencies. The 8 kHz input clock does not need to have a 50% duty cycle; a “high” or “on” pulse as narrow as 10 ns is acceptable.

Buffer Mode

Unlike the other mode that accepts only a single specified input frequency, Buffer Mode will accept a wider range of input clocks. The input jitter is attenuated, and the outputs on CLK and CLK/2 also provide the option of getting x1, x2, or 1/2 of the input frequency. For example, this mode can be used to remove the jitter from a 27 MHz clock, generating low-jitter 27 MHz and 54 MHz outputs.

FREQUENCY LOCKING TO THE INPUT

In all modes, the output clocks are frequency-locked to the input. The output will remain at the specified output frequency as long as the combined variation of the input frequency and the crystal does not exceed 100 ppm. For example, if the crystal can vary ±40 ppm (initial accuracy + temperature + aging), then the input frequency can vary by up to 60 ppm and still have the output clock remain frequency-locked.

EXTERNAL COMPONENT SELECTION

The MK2049-35 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF must be connected between VDD and GND pins close to the chip (especially pins 4 and 7, 15 and 17), and 33 Ω series terminating resistors should be used on clock outputs with traces longer than 1 inch (assuming 50 Ω traces). The selection of additional external components is described in the following sections.

Loop Filter Components

The external loop filter should be connected between CAP1 and CAP2 as shown in Figure 3 below, and as close to the chip as possible. High quality ceramic capacitors are recommended. DO NOT use any type of polarized or electrolytic capacitor. Ceramic capacitors should have C0G or NP0 dielectric. Another alternative is the Panasonic PPS polymer dielectric series; their part number for the 0.1 µF cap is ECHU1C104JB5. Avoid high-K dielectrics like Z5U and X7R; these and other ceramics which have piezolectric properties allow mechanical vibration in the system to increase the output jitter because the mechanical energy is converted directly to voltage noise on the VCO input.

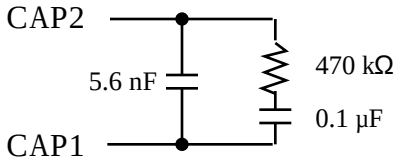


Figure 3. Loop Filter Component Values
(Typical component values are shown. Contact the ICS MicroClock applications department at (408)297-1201 for the recommended values for your application)

Crystal Operation

The MK2049 operates by phase locking the input signal to a VCXO which consists of the special recommended crystal and the integrated VCXO oscillator circuit on the MK2049. To achieve the best performance and reliability, the layout guidelines shown on the next page must be closely followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the load capacitors connected to it. The MK2049 has variable load capacitors on-chip which “pull”, or change the frequency of the crystal. External stray capacitance must be kept to a minimum to ensure maximum pullability of the crystal. To achieve this, the layout should use short traces between the MK2049 and the crystal.

EXTERNAL COMPONENT SELECTION (continued)

Crystal Specifications

Parameter	Minimum	Typical	Maximum	Units
Operating Temperature Range	0	25	70	°C
Initial Accuracy at 25 C	-20		20	ppm
Temperature stability	-30		30	ppm
Aging, first year	-5		5	ppm
Aging, 10 years	-20		20	ppm
Load Capacitance		Note 1		
Shunt Capacitance, C0			7	pF
Motional Capacitance, C1	none		none	pF
C0/C1 ratio			250	none
Equivalent Series Resistance			35	Ohms

Note 1: Nominal crystal load capacitance specifications varies with frequency. Contact the ICS MicroClock applications department at (408)297-1201

Note 2: The third overtone mode of the crystal and all spurs must be >200 ppm away from 3x the fundamental resonance shown in the table below.

For recommended crystal devices, please contact the ICS MicroClock application department at 408-297-1201.

EXTERNAL COMPONENT SELECTION (continued)

Determining the Crystal Frequency Adjustment Capacitors

To determine the crystal adjustment capacitor values, you will need a PC board of your final layout, a frequency counter capable of less than 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified load capacitance, C_L .

To determine the value of the crystal capacitors:

1. Connect VDD of the MK2049 to 3.3 V. Connect pin 18 of the MK2049 to the second power supply. Adjust the voltage on pin 18 to 0.0 V. Measure and record the frequency of the CLK or CLK/2 output .
2. Adjust the voltage on pin 18 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$\text{Centering error} = 10^6 \left[\frac{(f_{3.3V} - f_{target}) + (f_{0.0V} - f_{target})}{f_{target}} \right] - \text{error}_{xtal}$$

Where f_{target} = 44.736000 MHz, for example, and error_{xtal} = actual initial accuracy (in ppm) of the crystal being measured.

If the centering error is less than ±15 ppm, no adjustment is needed. If the centering error is more than 15 ppm negative, the PC board has too much stray capacitance and will need to be redone with a new layout to reduce stray capacitance. (The crystal may be re-specified to a lower load capacitance instead. Contact ICS MicroClock for details.) If the centering error is more than 15 ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor = 2*(centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (less than ±15 ppm).

The MicroClock Applications department can perform this procedure on your board. Call us at 408–295–9800, and we will arrange for you to send us a PC board (stuffed or unstuffed) and one of your crystals. We will calculate the value of capacitors needed.

PC BOARD LAYOUT

A proper board layout is critical to the successful use of the MK2049. In particular, the CAP1 and CAP2 pins are very sensitive to noise and leakage (CAP2 at pin 18 is the most sensitive). Traces must be as short as possible and the two capacitors and resistor must be mounted next to the device as shown below. The capacitor shown between pins 15 and 17, and the one between pins 4 and 7 are the power supply decoupling capacitors. The high frequency output clocks on pins 8 and 9 should have a series termination of 33 Ω connected close to the pin. Additional improvements will come from keeping all components on the same side of the board, minimizing vias through other signal layers, and routing other signals away from the MK2049. You may also refer to MAN05 for additional suggestions on layout of the crystal section.

The crystal traces should include pads for small capacitors from X1 and X2 to ground; these are used to adjust the stray capacitance of the board to match the crystal load capacitance. The typical telecom reference frequency is accurate to much less than 1 ppm, so the MK2049 may lock and run properly even if the board capacitance is not adjusted with these fixed capacitors. However, ICS MicroClock recommends that the adjustment capacitors be included to minimize the effects of variation in individual crystals, temperature, and aging. The value of these capacitors (typically 0-4 pF) is determined once for a given board layout, using the procedure described in the section titled “Determining the Crystal Frequency Adjustment Capacitors”.

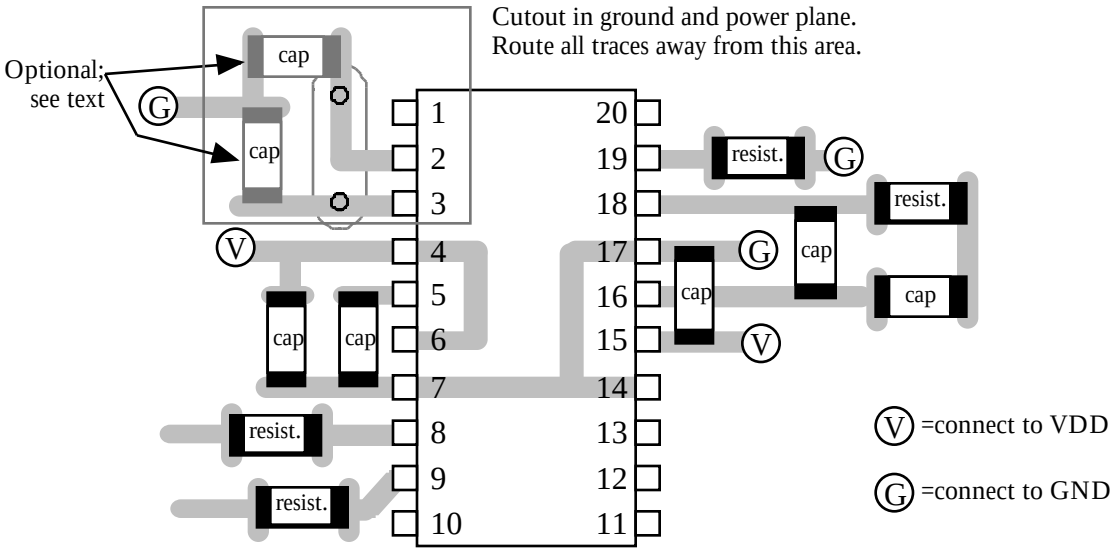
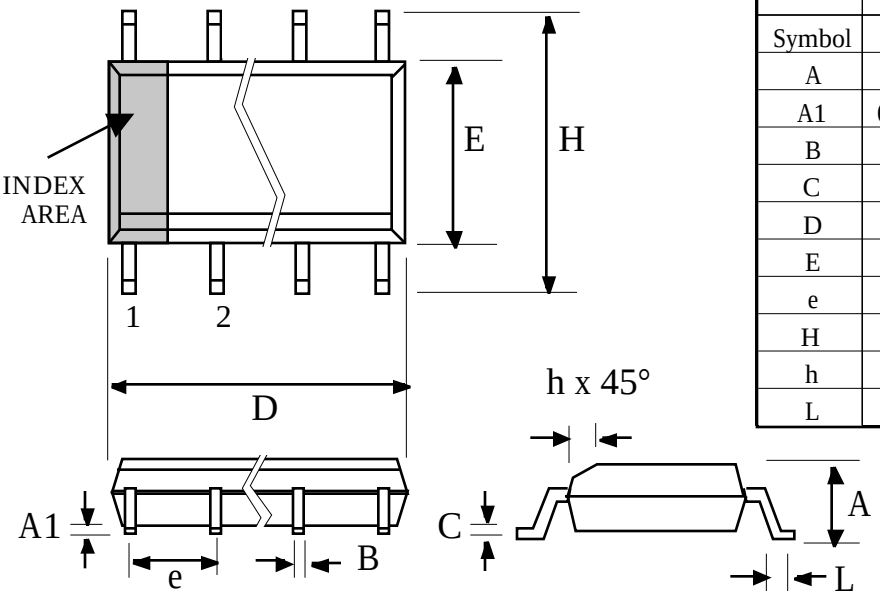


Figure 2. Typical MK2049-35 Layout

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



20 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	--	0.104	--	2.65
A1	0.0040	--	0.10	--
B	0.013	0.020	0.33	0.51
C	0.007	0.013	0.18	0.33
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	0.394	0.419	10.01	10.64
h	0.01	0.029	0.25	0.74
L	0.016	0.050	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK2049-35SI	MK2049-35SI	20 pin SOIC	-40 to 85 °C
MK2049-35SITR	MK2049-35SI	Add Tape & Reel	-40 to 85 °C