Integrated Circuit Systems, Inc.

Product Brief

M830/831

10 GBIT OC-192 CLOCK & DATA RECOVERY MODULE

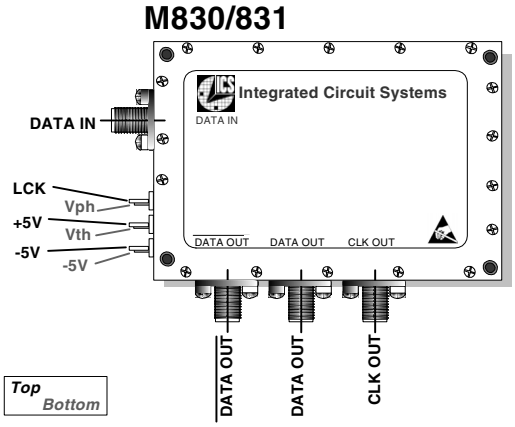
GENERAL DESCRIPTION

The M830/831 Voltage Controlled Clock & Data Recovery Module recovers the spectral component from an incoming NRZ data stream and outputs a low-jitter clock and retimed complementary data. The Phase Locked Loop (PLL) architecture incorporates a SAW (Surface Acoustic Wave) based Voltage Controlled Oscillator (VCSO) to provide extremely low jitter clock and data outputs. The M830 differs from the M831 in that it has a narrower PLL bandwidth, enabling it to be used in transmitter applications when paired with the M831 as the receiver.

FEATURES

- Superior VCSO-based PLL jitter performance
- 9.5ps peak-to-peak clock output jitter, typical
- 0.9V peak-to-peak complementary data output
- 1 UI externally adjustable clock phase
- 200mV peak-to-peak input sensitivity
- Externally adjustable decision threshold
- Designed for SONET OC-192 and SDH STM-64 physical layer clock and data recovery applications
- +5V and -5V power supplies
- Easy to connect 1.89 x 2.49 inch SMA package

PIN ASSIGNMENT (1.89 x 2.49 inch SMA)



Example Input/Output Frequency Combinations

Operating Data Rate (Gb/sec)	Clock Output Freq [1] (GHz) OC-192	Applications
9.953	9.953	OC-192
10.312	10.312	
10.664	10.664	
10.709	10.709	
12.249	12.249	

1. Consult factory for frequency availability

BLOCK DIAGRAM