Integrated Circuit Systems, Inc.

ICS950806

Advance Information

Frequency Generator with 200MHz Differential CPU Clocks

Recommended Application

CK-408 clock with driven mode only for Almador - M chipset with P4 processor. Programmable for group to group skew.

Output Features:

- 3 Differential CPU Clock Pairs @ 3.3V
- 7 PCI (3.3V) @ 33.3MHz including 2 early PCI clocks
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz, 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz
- 3 66MHz_OUT/3V66 (3.3V) @ 66.6MHz_IN or 66.6MHz

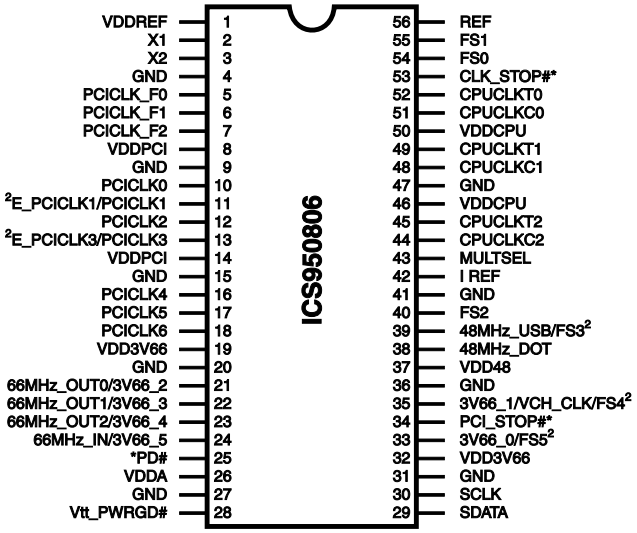
Features:

- Provides standard frequencies and additional 5% and 10% over-clocked frequencies
- Supports spread spectrum modulation: No spread, Center Spread (±0.35%, ±0.5%, or ±0.75%), or Down Spread (-0.5%, -1.0%, or -1.5%)
- Offers adjustable PCI early clock via I^2C interface
- Selectable 1X or 2X strength for REF via I^2C interface
- Efficient power management scheme through PD#, CLK_STOP# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through I^2C interface.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- 66MHz Output Jitter (Buffered Mode Only) <100ps
- CPU Output Skew <100ps

Pin Configuration

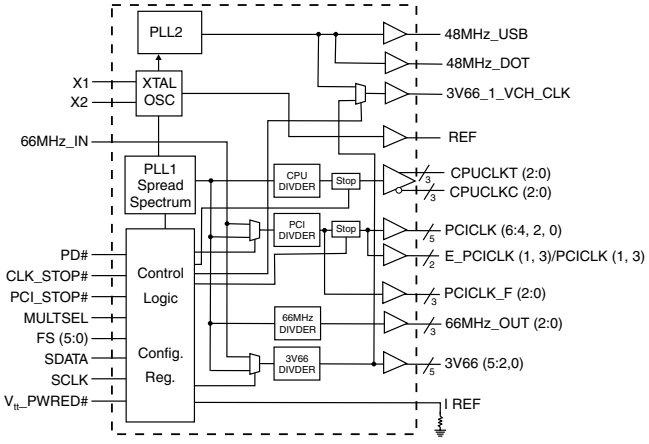


56-Pin 300mil SSOP

240mil 6.10 mm. Body, 0.50 mm. pitch TSSOP

* These inputs have 120K internal pull-up resistor to VDD.
1. Includes internal selectabel 10K resistor for adjustable PCI early clock.
2. Internal pull-down to ground.

Block Diagram



Functionality

Bit			CPUCLK	3V66	66MHz_OUT (2:0)	66MHz_IN	PCICLK_F
					3V66 (4:2)	3V66_5	PCICLK
FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	0	0	66.66	66.66	66.66	66.66	33.33
0	0	1	100.00	66.66	66.66	66.66	33.33
0	1	0	200.00	66.66	66.66	66.66	33.33
0	1	1	133.33	66.66	66.66	66.66	33.33
1	0	0	66.66	66.66	66MHz_IN	Input	66MHz_IN/2
1	0	1	100.00	66.66	66MHz_IN	Input	66MHz_IN/2
1	1	0	200.00	66.66	66MHz_IN	Input	66MHz_IN/2
1	1	1	133.33	66.66	66MHz_IN	Input	66MHz_IN/2

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 19, 26, 32, 37, 46, 50	VDD	PWR	3.3V power supply
2	X1	X2 Crystal Input	14.318MHz Crystal input
3	X2	X1 Crystal Output	14.318MHz Crystal output
7, 6, 5	PCICLK_F (2:0)	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
4, 9, 15, 20, 27, 31, 36, 41, 47	GND	PWR	Ground pins for 3.3V supply
13, 11	E_PCICLK (3, 1)	OUT	Early PCI clock outputs latched at power up through internal pull-down to ground
	PCICLK (3, 1)	OUT	PCI clock output
18, 17, 16, 12, 10	PCICLK (6:4,2,0)	OUT	PCI clock outputs
23, 22, 21	66MHz_OUT (2:0)	OUT	66MHz buffered 66MHz_OUT from 66MHz_IN input.
	3V66 (4:2)	OUT	66MHz reference clocks, from internal VCO
24	66MHz_IN	IN	66MHz input to buffered 66MHz_OUT and PCI clocks
	3V66_5	OUT	66MHz reference clock, from internal VCO
25	PD#	IN	Invokes power-down mode. Active Low.
28	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS[0:2] and MULTISEL0 inputs are valid and are ready to be sampled (active low)
29	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
33	FS5	IN	Frequency select pin controlling, spread selection. Internal pull-down
	3V66_0	OUT	66MHz reference clocks, from internal VCO
34	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low except PCICLK_F which are free running
35	FS4	IN	Frequency select pin controlling, spread selection. Internal pull-down
	3V66_1_VCH_CLK	OUT	3.3V output selectable through I^2C to be 66MHz from internal VCO or 48MHz (non-SSC)
38	48MHz_DOT	OUT	48MHz output clock for DOT
39	FS3	IN	Frequency select pin controlling, spread selection. Internal pull-down
	48MHz_USB	OUT	48MHz output clock for USB
40	FS2	IN	Special frequency select pin controlling either buffered mode or PLL-driven mode for 3V66, 66MHz_OUT, PCICLK, and PCICLK_F clocks.
42	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL	IN	MULTSEL0 input is sensed on power-up and then internally latched prior to the pin being used for output on 3V 14.318MHz clocks.
44, 48, 51	CPUCLKC (2:0)	OUT	"Complementary" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
45, 49, 52	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
53	CLK_STOP#	IN	Controls CPU_STOP and 3V66_STOP, internal pull-up
55, 54	FS (1:0)	IN	Frequency select pins
56	REF	OUT	14.318MHz reference clock.

Power Groups

(Analog)
VDDA = PLL1
VDD48 = 48MHz, PLL
VDDREF = VDD for Xtal, POR

(Digital)
VDDPCI
VDD3V66
VDDCPU

Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PD# = 0)	40mA
Full Active	360mA

Host Swing Select Functions

MULTISEL	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3*Rr)	Output Current	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4* I REF	1.0V @ 50
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

PCI Slect Functions

E_PCICLK1	E_PCICLK3	E_PCICLK (1, 3)
0	0	0ns
0	1	0.5ns
1	0	1.0ns
1	1	1.5ns

Note:
E_PCICLK1 = 10KΩ resistor
E_PCICLK3 = 10KΩ resistor
0 = No resistor
1 = 10KΩ pull-up to VDD

Frequency Select Table 1

Bit	Description									
	Bit				CPUCLK	3V66	66MHz_OUT (2:0)	66MHz_IN	PCICLK_F	Clocking Mode
							3V66 (4:2)	3V66_5	PCICLK	
	FS5:3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz	
	From 000 to 101 (See Table 2)	0	0	0	66.66	66.66	66.66	66.66	33.33	Standard Clocking
		0	0	1	100.00	66.66	66.66	66.66	33.33	Standard Clocking
		0	1	0	200.00	66.66	66.66	66.66	33.33	Standard Clocking
		0	1	1	133.33	66.66	66.66	66.66	33.33	Standard Clocking
		1	0	0	66.66	66.66	66M Hz_IN	Input	66M Hz_IN/2	Standard Clocking
		1	0	1	100.00	66.66	66M Hz_IN	Input	66M Hz_IN/2	Standard Clocking
		1	1	0	200.00	66.66	66M Hz_IN	Input	66M Hz_IN/2	Standard Clocking
		1	1	1	133.33	66.66	66M Hz_IN	Input	66M Hz_IN/2	Standard Clocking
	110 (See Table 2)	0	0	0	70.00	70.00	70.00	70.00	35.00	5% Over-clocking
		0	0	1	105.00	70.00	70.00	70.00	35.00	5% Over-clocking
		0	1	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
		0	1	1	140.00	70.00	70.00	70.00	35.00	5% Over-clocking
		1	0	0	70.00	70.00	66M Hz_IN	Input	66M Hz_IN/2	5% Over-clocking
		1	0	1	105.00	70.00	66M Hz_IN	Input	66M Hz_IN/2	5% Over-clocking
		1	1	0	Test	Test	Test	Test	Test	Test
		1	1	1	140.00	70.00	66M Hz_IN	Input	66M Hz_IN/2	5% Over-clocking
	111 (See Table 2)	0	0	0	73.32	73.32	73.32	73.32	36.66	10% Over-clocking
		0	0	1	110.00	73.32	73.32	73.32	36.66	10% Over-clocking
		0	1	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
		0	1	1	146.60	73.32	73.32	73.32	36.66	10% Over-clocking
		1	0	0	73.32	73.32	66M Hz_IN	Input	66M Hz_IN/2	10% Over-clocking
		1	0	1	110.00	73.32	66M Hz_IN	Input	66M Hz_IN/2	10% Over-clocking
		1	1	0	Test/2	Test/4	Test/4	Test/4	Test/8	Test
		1	1	1	146.60	73.32	66M Hz_IN	Input	66M Hz_IN/2	10% Over-clocking

Note: FS2 controls 3V66, 66MHz_OUT (2:0), 3V66 (4:2), 66MHz_IN/3V66_5, PCICLK_F, and PCICLK clocks for either buffered or unbuffered (PLL-driven) modes.

Note: Default settings: FS (2:0) = left floating (unconnected).

Frequency Select Table 2

Bit	Description				
	Bit			CPUCLK, 3V66, 66MHz_OUT (2:0)/3V66 (4:2), 66MHz_IN/3V66_5, PCICLK_F, and PCICLK (controlled by FS 2:0) (See Table 1)	Spread Selection
	FS5	FS4	FS3		
	0	0	0	Standard Clocking	No Spread (default) or ±0.4%
	0	0	1	Standard Clocking	0 to -0.5%, Down Spread
	0	1	0	Standard Clocking	0 to -1.0%, Down Spread
	0	1	1	Standard Clocking	0 to -1.5%, Down Spread
	1	0	0	Standard Clocking	0.5%, Center Spread
	1	0	1	Standard Clocking	0.75%, Center Spread
	1	1	0	5% Over-clocking	0.35%, Center Spread
	1	1	1	10% Over-clocking	0.35%, Center Spread

Note: Default settings: FS (5:3) = 000

Byte 0: Control Register

Bit	Pin#	Name	PWD[3]	Type[2]	Description
Bit 0	54	FS0	X	R	Reflects the value of FS0 pin sampled on power up
Bit 1	55	FS1	X	R	Reflects the value of FS1 pin sampled on power up
Bit 2	39	FS3	X	R	Reflects the value of FS3 pin sampled on power up
Bit 3	34	PCI_STOP#[3]	X	R	Hardware mode: Reflects the value of PCI_STOP# pin sampled on PWD
			1	RW	Software mode: 0=PCICLK stopped 1=PCICLK running
Bit 4	35	FS4	X	R	FS4 (read only)
Bit 5	35	3V66_1_VCH	0	RW	VCH Select 66MHz/48MHz 0=66MHz, 1=48MHz
Bit 6	33	FS5	0		Reflects the value of FS5 pin sampled on power up
Bit 7	-	Spread Enabled	0	RW	0=Spread Off, 1=Spread On

Note: For PCI_STOP#, refer to table 3

Byte 1: Control Register

Bit	Pin#	Name	PWD[3]	Type[2]	Description
Bit 0	52, 51	CPUCLKT0 CPUCLKC0	1	RW	0=Disabled, 1=Enabled[5]
Bit 1	49, 48	CPUCLKT1 CPUCLKC1	1	RW	0=Disabled, 1=Enabled[5]
Bit 2	45, 44	CPUCLKT2 CPUCLKC2	1	RW	0=Disabled, 1=Enabled[5]
Bit 3	52, 51	CPUCLKT/C0 Control	0	RW	Allows control of CPUCLKT/C0 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 4	33,35	3V66_0/1	1	RW	3V66_0/1 mode 0 = Not free running 1= Free running
Bit 5	21,22, 23,24	3V66_2/3/4/5	1	RW	3V66_2/3/4/5 mode 0 = Not free running 1= Free running
Bit 6	49, 48	CPUCLKT/C1 Control	0	RW	Allows control of CPUCLKT/C1 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 7	45, 44	CPUCLKT/C2 Control	0	RW	Allows control of CPUCLKT/C2 with assertion of CPU_STOP# 0=Not free running 1=Free running

Notes:

1. For Byte1, Bits (3:7) refer to tables 4, 5, and 6.
2. R= Read only RW= Read and Write
3. PWD = Power on Default
4. The purpose of this bit is to allow a system designer to implement PCI_STOP functionality in one of two ways. Wither the system designer can choose to use the externally provided PCI_STOP# pin to assert and de-assert PCI_STOP functionality via I^2C Byte 0 Bit 3.

   In Hardware mode it is not allowed to write to the I^2C Byte 0 Bit3. In Software mode it is not allowed to pull the external PCI_STOP pin low. This avoids the issues related with Hardware started and software stopped PCI_STOP conditions. The clock chip is to be operated in the Hardware or Software PCI_STOP mode ONLY, it is not allowed to mix these modes.

   In Hardware mode the I^2C byte 0 Bit 3 is R/W and should reflect the status of the part. Whether or not the chip is in PCI_STOP mode.

   Functionality PCI_STOP mode should be entered when [(PCI_STOP#=0) or (I^2C Byte 0 Bit 3 = 0)].
5. For disabled clocks, they stop low for single ended clocks. Differential CPU clocks stop with CPUCLKT at high, CPUCLKC off, and external resistor termination will bring CPUCLKC low.

Byte 2: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	10	PCICLK0	1	RW	0=Disabled 1=Enabled
Bit 1	11	PCICLK1	1	RW	0=Disabled 1=Enabled
Bit 2	12	PCICLK2	1	RW	0=Disabled 1=Enabled
Bit 3	13	PCICLK3	1	RW	0=Disabled 1=Enabled
Bit 4	16	PCICLK4	1	RW	0=Disabled 1=Enabled
Bit 5	17	PCICLK5	1	RW	0=Disabled 1=Enabled
Bit 6	18	PCICLK6	1	RW	0=Disabled 1=Enabled
Bit 7	-	REF_1X2X	0	RW	REF 1X or 2X strength control 0 = 1X, 1 = 2X

Byte 3: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	5	PCICLK_F0	1	RW	0=Disabled 1=Enabled
Bit 1	6	PCICLK_F1	1	RW	0=Disabled 1=Enabled
Bit 2	7	PCICLK_F2	1	RW	0=Disabled 1=Enabled
Bit 3	5	PCICLK_F0 Stop	0	RW	Allow control of PCICLK_F0 with assertion of PCI_STOP#. 0=Free Running, 1=Stop
Bit 4	6	PCICLK_F1 Stop	0	RW	Allow control of PCICLK_F1 with assertion of PCI_STOP#. 0=Free Running, 1=Stop
Bit 5	7	PCICLK_F2 Stop	0	RW	Allow control of PCICLK_F2 with assertion of PCI_STOP#. 0=Free Running, 1=Stop
Bit 6	39	48MHz_USB	1	RW	0=Disabled 1=Enabled
Bit 7	38	48MHz_DOT	1	RW	0=Disabled 1=Enabled

Notes:
1. PCICLK_F (2:0) can be turned on/off by PCI_STOP#.
2. For PCICLK_F (2:0), please refer to table 7.

Byte 4: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	21	66MHz_OUT0/3V66-2	1	RW	0=Disabled 1=Enabled
Bit 1	22	66MHz_OUT1/3V66-3	1	RW	0=Disabled 1=Enabled
Bit 2	23	66MHz_OUT2/3V66-4	1	RW	0=Disabled 1=Enabled
Bit 3	24	3V66_5	1	RW	0=Disabled 1=Enabled
Bit 4	35	3V66_1_VCH_CLK	1	RW	0=Disabled 1=Enabled
Bit 5	33	3V66_0	1	RW	0=Disabled 1=Enabled
Bit 6	-	CPUSTOP# Buffer/Driven mode switch enable	0	RW	0=Disabled 1=Enabled
Bit 7	-	-	0	R	(Reserved)

Notes:
1. R= Read only RW= Read and Write
2. PWD = Power on Default

Byte 5: Programming Edge Rate
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Type	Description
Bit 0	39	48MHz_USB	0	RW	USB edge rate cntrol
Bit 1	39	48MHz_USB	0	RW	USB edge rate cntrol
Bit 2	38	48MHz_DOT	0	RW	DOT edge rate control
Bit 3	38	48MHz_DOT	0	RW	DOT edge rate control
Bit 4	23	66MHz_OUT (2)	0	RW	T_{pd} 66MHz_IN to 66MHz_OUT propagation delay control for 3V66 Skew Control
Bit 5	23	66MHz_OUT (2)	0	RW	T_{pd} 66MHz_IN to 66MHz_OUT propagation delay control for 3V66 Skew Control
Bit 6	22, 21	66MHz_OUT (1:0)	0	RW	T_{pd} 66MHz_IN to 66MHz_OUT propagation delay control for 3V66 Skew Control
Bit 7	22, 21	66MHz_OUT (1:0)	0	RW	T_{pd} 66MHz_IN to 66MHz_OUT propagation delay control for 3V66 Skew Control

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Type	Description
Bit 0	X	Vendor ID Bit0	1	R	(Reserved)
Bit 1	X	Vendor ID Bit1	0	R	(Reserved)
Bit 2	X	Vendor ID Bit2	0	R	(Reserved)
Bit 3	X	Vendor ID Bit3	0	R	(Reserved)
Bit 4	X	Revision ID Bit0	X	R	Revision ID values will be based on individual device's revision
Bit 5	X	Revision ID Bit1	X	R	
Bit 6	X	Revision ID Bit2	X	R	
Bit 7	X	Revision ID Bit3	X	R	

Byte 7: CPU Skew and 3V66 Slew Control Register
(1 = enable, 0 = disable)

Bit	Description	PWD
Bit 0	3V66_5:2 Slew Control	0
Bit 1		1
Bit 2	3V66_1:0 Slew Control	0
Bit 3		1
Bit 4	CPUCLKT1/C1 Skew Control	0
Bit 5		0
Bit 6	CPUCLKT0/C0 & CPUCLKT2/C2	0
Bit 7	Skew Control	0

Byte 8: Slew Control Register
(1 = enable, 0 = disable)

Bit	Description	PWD
Bit 0	PCICLK (6:4) Slew Rate	0
Bit 1		1
Bit 2	PCICLK (3:0) Slew Rate	0
Bit 3		1
Bit 4	PCICLK_F (1:0) Slew Rate	0
Bit 5		1
Bit 6	VCH_CLK Slew Rate	0
Bit 7		1

Notes:

1. R= Read only RW= Read and Write
2. PWD = Power on Default

Table 3

PCI_STOP# I²C Control Table- Byte 0, Bit 3

PCI_STOP#	Byte 0, Bit 3 Write Bit	Byte 0, Bit 3 Read Bit (Internal Status)
0	0	0
0	1	0
1	0	0
1	1	1

Note: When this Byte 0, Bit 1 is low (0), all PCI clocks are stopped.

Table 4

CPUCLKT/C (0:2) Outputs I²C Control Table

Byte 1, Bit 3, 6, 7	CLK_STOP# (Pin 53)	CPU_CLKT/C Outputs (0:2)
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Table 5

3V66 (1:0) I²C Control Table - Byte 1, Bit 4

Byte 1, Bit 4	CLK_STOP#	3V66 (1:0)
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Table 6

3V66 (5:2) I²C Control Table - Byte 1, Bit 5

Byte 1, Bit 5	CLK_STOP#	3V66 (5:2)
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Table 7

PCICLK_F (0:2) Stop

PCI_STOP#	Byte 3, Bits 3, 4, & 5	PCICLK_F (0:2)
0	0	Running
0	1	Stop
1	0	Running
1	1	Running

Table 8

3V66_0/1 I²C Control Table - Byte 1, Bit 4

Byte 1, Bit 4	CLK_STOP#	3V66_0/1
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Table 9

3V66_2/3/4/5 I²C Control Table - Byte 1, Bit 4

Byte 1, Bit 5	CLK_STOP#	3V66_2/3/4/5
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Table 10

Byte 3, Bit 3, 4, & 5 (PCICLK_F (0:2) Stop)

PCI_STOP#	Byte 3, Bits 3, 4, & 5	PCICLK_F (2:0)
0	0	Running
0	1	Stop
1	0	Running
1	1	Running

Absolute Maximum Ratings

Supply Voltage ..... 5.5 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Case Temperature ..... 115°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
		C_L = Full load			360	mA
Power Down Supply Current	$I_{DD3.3PD}$	IREF=2.32			25	mA
		IREF= 5mA			45	m_A
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Z_O	$V_O = V_X$	3000			Ω
Output High Voltage	V_{OH}	V_R = 475Ω +1%; IREF =		0.71	1.2	V
Output High Current	I_{OH}	2.32mA; I_{OH} = 6*IREF		-13.92		mA
Rise Time[1]	t_r	V_{OL} = 20%, V_{OH} = 80%	175		700	ps
Differential Crossover Voltage[1]	V_X	Note 3	45	50	55	%
Duty Cycle[1]	d_t	V_T = 50%	45	51	55	%
Skew[1], CPU to CPU	t_{sk}	V_T = 50%			100	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	$V_T = V_X$			150	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK Buffered Mode

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F0[1]			33.33		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jadditive}$[1]	V_T = 1.5 V			100	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK Un-Buffered Mode

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F0[1]			33.33		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66 - Buffered Mode: 3V66 [1:0] 66MHz_OUT [2:0]

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V 3V66 [1:0]			500	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V 3V66 [1:0]			250	ps
Skew	t_{sk1}[1]	V_T = 1.5 V 66MHz_OUT [2:0]			175	ps
Jitter	$t_{jadditive}$	V_T = 1.5 V 66MHz_OUT [2:0]			100	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66 - Un- Buffered Mode: 3V66 [5:0]

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	tjcyc-cyc[1]	V_T = 1.5 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O[1]	$V_O = V_{DD}*(0.5)$		48		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1	ns
VCH 48 USB Rise Time	t_r[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns
VCH 48 USB Fall Time	tf[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns
48 DOT to 48 USB Skew	tskew[1]	VT=1.5V			1	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

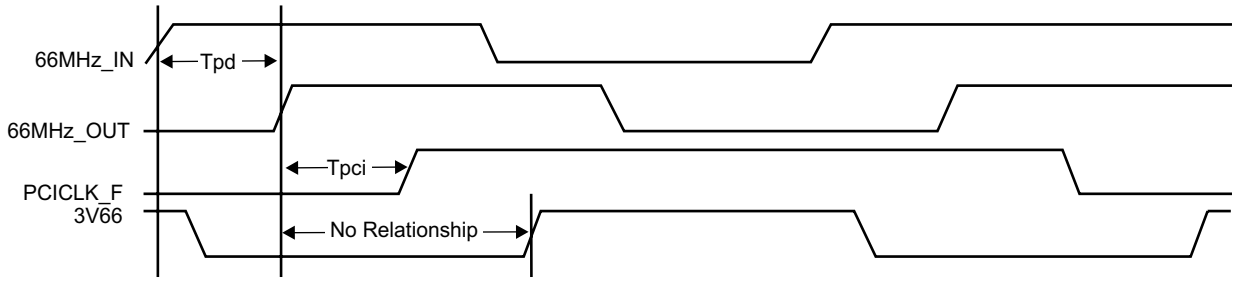
Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Buffered Mode - 3V66[0:1], 66MHz_IN, 66MHz_OUT[0:2] and PCI Phase Relationship

All 3V66 clocks are to be in phase with each other. All 66MHz_OUT clocks are to be in phase with each other. There is NO phase relationship between the 3V66 clocks and the 66MHz_OUT and PCI clocks. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1_VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.

The 66MHz_IN to 66MHz_OUT delay is shown in the figure below and is specified to be within a min and max propagation value.



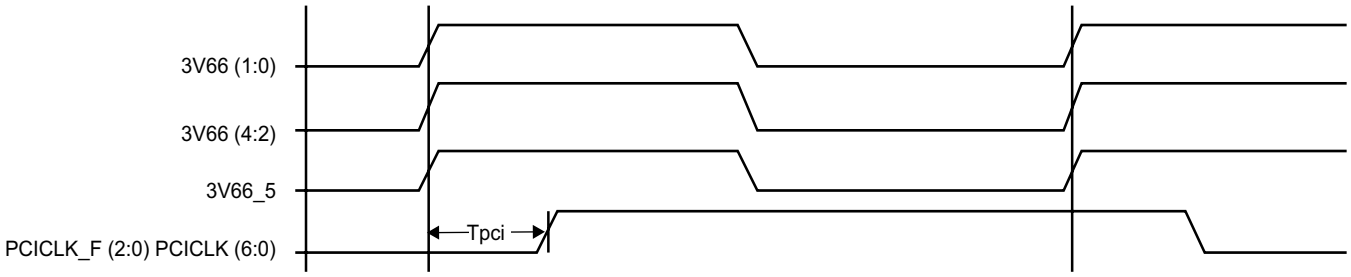
Group Skews at Common Transition Edges: (Buffered Mode)

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 (1:0) pin to pin skew	0		500	ps
66MHz_OUT	66OUT	66MHz_OUT (2:0) pin to pin skew	0		175	ps
PCICLK	PCICLK	PCICLK_F (2:0) and PCICLK (6:0) pin to pin skew	0		500	ps
66MHz_IN 66MHz_OUT	Tpd	Propogation delay from 66MHz_IN to 66MHz_OUT (2:0)	2.5		4.5	nS
66MHz_OUT to PCI	Tpci	66MHz_OUT (2:0) leads 33 MHz PCICLK	1.5		3.5	nS

[1]Guaranteed by design, not 100% tested in production.

Un-Buffered Mode 3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1_VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group Skews at Common Transition Edges: (Un-Buffered Mode)

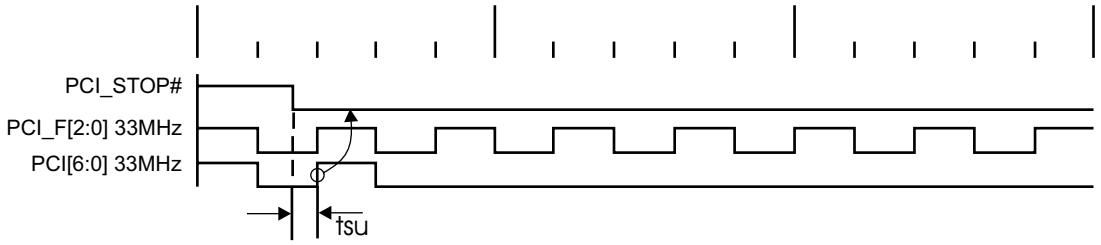
GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 (5:0) pin to pin skew	0		500	ps
PCICLK	PCICLK	PCICLK_F (2:0) and PCICLK (6:0) pin to pin skew	0		500	ps
3V66 to PCICLK	$S_{3V66-PCI}$	3V66 (5:0) leads 33MHz PCI	1.5		3.5	ns

[1]Guaranteed by design, not 100% tested in production.

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCICLK(6:0) and stoppable PCICLK_F(2,0) clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

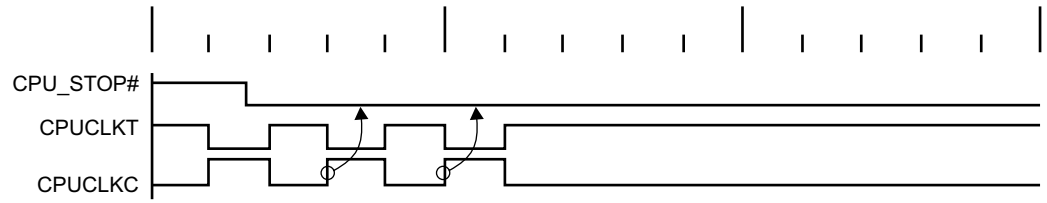
Assertion of PCI_STOP# Waveforms



CLK_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CLK_STOP# Functionality

CLK_STOP#	CPUCLKT	CLKC	66MHz_OUT*
1	Normal	Normal	66MHz_OUT (2:0) (buffer mode)
0	iref * Mult	Float	3V66 (4:2) (driven mode)

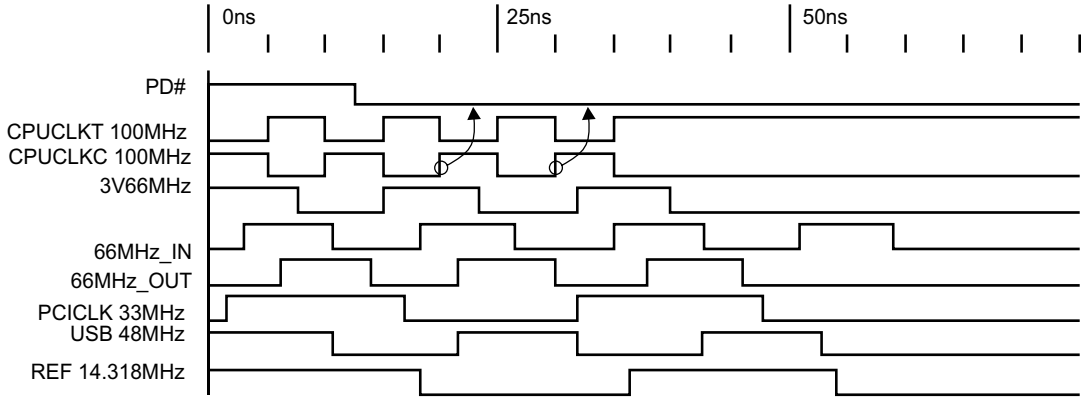
* This feature will only work when the part is in buffer mode (FS2 = 1).

PD# - Assertion (transition from logic "1" to logic "0")

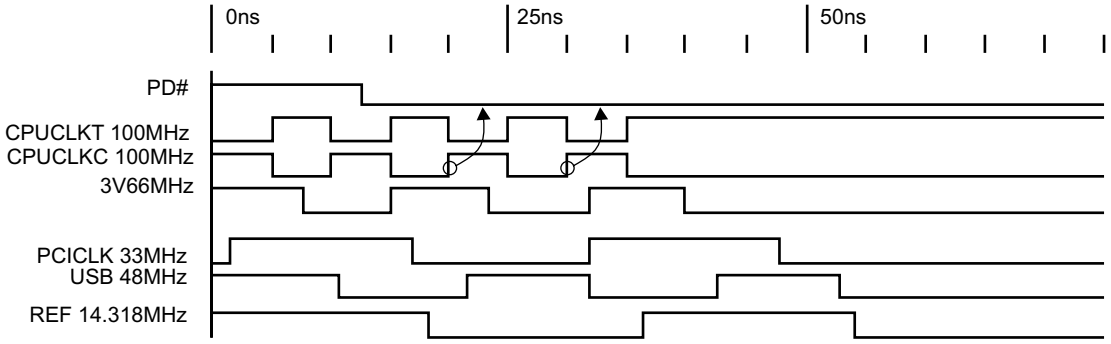
When PD# is sampled low by two consecutive rising edges of CPU clock then all clock outputs except CPU clocks must be held low on their next high to low transition. CPU clocks must be held with the CPU clock pin driven high with a value of 2x Iref, and CPUCLKC undriven. Note the example below shows CPU = 100MHz, this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200MHz.

Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms - Buffered Mode

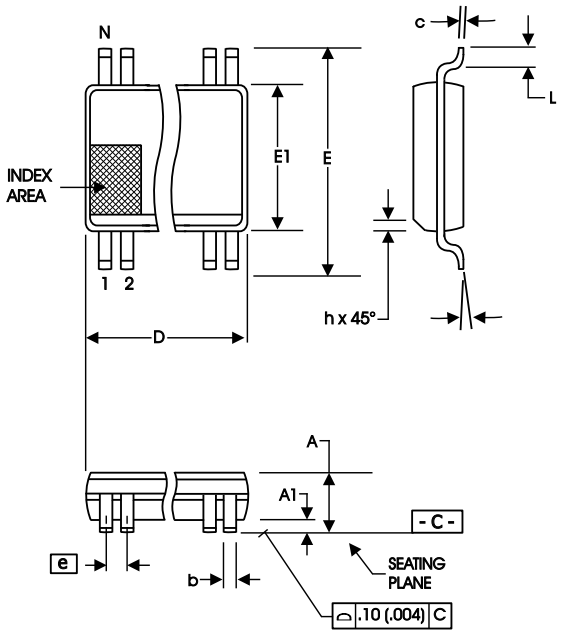


Power Down Assertion of Waveforms - Unuffered Mode



PD# Functionality

CPU_STOP#	CPUCLKT	CPUCLKC	3V66	66MHz_OUT	PCICLK_F PCICLK	PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	66MHz_IN	66MHz_IN	66MHz_IN	48MHz
0	iref * Mult	Float	Low	Low	Low	Low	Low



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

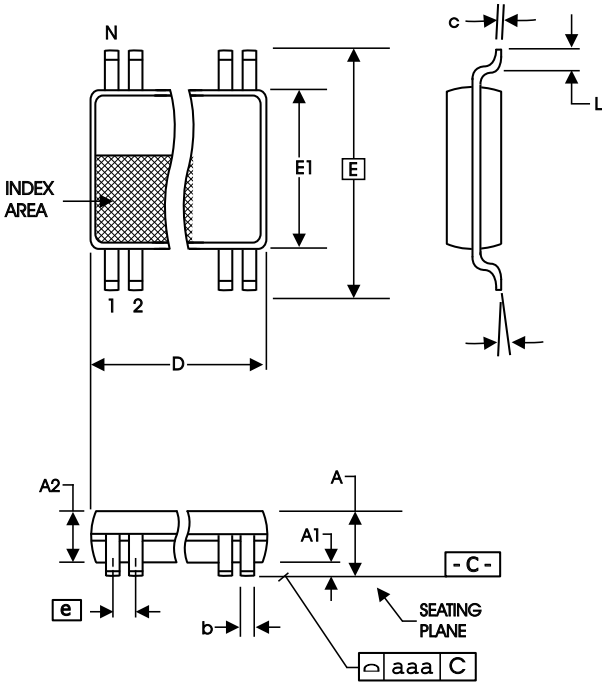
Ordering Information

ICS94239yFT

Example:

ICS XXXX y F - T

- **Designation for tape and reel packaging**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

'ARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

Ordering Information

ICS94239yGT

Example:

ICS XXXX y G - T

- **Designation for tape and reel packaging**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device