Integrated Circuit Systems, Inc.

ICS9248-172

Advance Information

PII/III™ System Clock Chip

Recommended Application:
ALI 1651 style chipset

Output Features:

- 2 - CPU clocks @ 2.5V
- 13 - SDRAM @ 3.3V
- 7 - PCI @3.3V
- 2 - AGP @ 3.3V
- 1 - IOAPIC @ 2.5V
- 1 - 48MHz, @3.3V
- 1 - REF @3.3V, (selectable strength) through I^2C

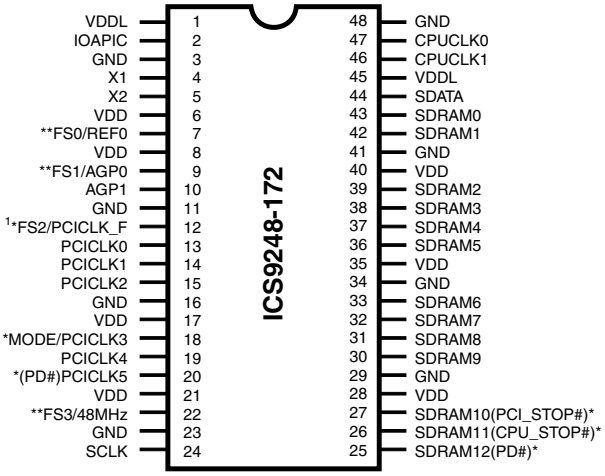
Features:

- Up to 147MHz frequency support
- Support power management: CPU stop, PCI stop and Power down.
- Spread spectrum for EMI control (0 to -0.5% down spread, ± 0.25% center spread).
- Uses external 14.318MHz crystal

Skew Specifications:

- CPU - CPU: <250ps
- PCI - PCI: <500ps
- SDRAM - SDRAM: <250ps
- AGP - AGP: <250ps
- PCI - AGP: <750ps
- CPU - SDRAM:<350ps
- CPU - PCI: <3ns

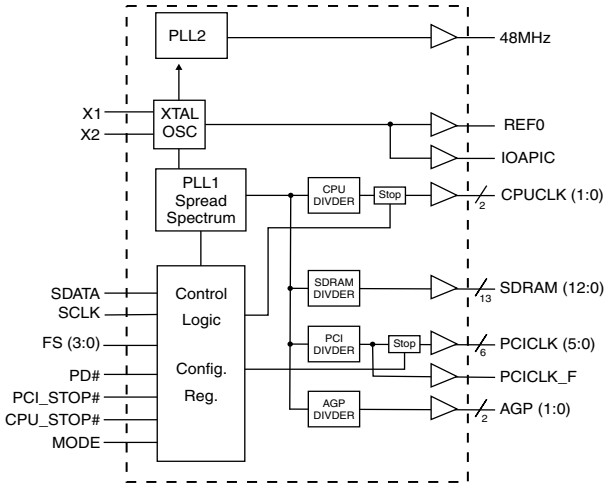
Pin Configuration



48-Pin 300mil SSOP & 240mil TSSOP

Notes:
REF0 can be 1X or 2X strength controlled by I^2C.
* Internal Pull-up Resistor of 120K to VDD.
** Internal Pull-down of 120K to GND.
1. This input has 2X drive strength.

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU	SDRAM
0	0	0	0	66.66	66.66
0	0	0	1	66.66	100.00
0	0	1	0	100.00	66.66
0	0	1	1	100.00	100.00
0	1	0	0	100.00	133.33
0	1	0	1	133.33	66.66
0	1	1	0	133.33	100.00
0	1	1	1	133.33	133.33
1	0	0	0	66.66	66.66
1	0	0	1	66.66	100.00
1	0	1	0	100.00	66.66
1	0	1	1	100.00	100.00
1	1	0	0	100.00	133.33
1	1	0	1	133.33	66.66
1	1	1	0	133.33	100.00
1	1	1	1	133.33	133.33

Note:
PCICLK = 33.33MHz
AGP = 66.66MHz

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1,45	VDDL	PWR	Power supply pins, nominal 2.5V
2	IOAPIC	OUT	2.5V clock outputs
4	X1	IN	Crystal input,nominally 14.318MHz.
5	X2	OUT	Crystal output, nominally 14.318MHz.
3, 11, 16, 23, 29, 34, 41, 48	GND	PWR	Ground pins
6, 8, 17, 21, 28, 35, 40	VDD	PWR	Power supply pins, nominal 3.3V
7	FS0[2, 3]	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
9	FS1[2, 3]	IN	Frequency select pin.
	AGP0	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
10	AGP1	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
12	PCICLK_F	OUT	Free running PCICLK not stoped by PCI_STOP#
	FS2[1, 3]	IN	Frequency select pin.
19, 15, 14, 13	PCICLK (4, 2, 1, 0)	OUT	PCI clock outputs.
18	PCICLK3	OUT	PCI clock output.
	MODE[1, 3]	IN	Function select pin, 1=Desktop Mode, 0=Mobile Mode.
20	PD#[1]	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. This pin will be activiated when
	PCICLK5	OUT	PCI clock output.
22	FS3[2, 3]	IN	Frequency select pin.
	48MHz	OUT	48MHz output clock
24	SCLK	IN	Clock input of I^2C input, 5V tolerant input
25	PD#[1]	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. This pin will be activiated when
	SDRAM12	OUT	SDRAM clock output.
27	CPU_STOP#[1]	IN	This asynchronous input halts CPU, SDRAM, and AGP clocks at logic "0" level when driven low, the stop selection can be programmed through I^2C.
	SDRAM11	OUT	SDRAM clock output.
28	PCI_STOP#[1]	IN	Stops all PCICLKsbesides the PCICLK_F clocks at logic 0 level, when input low
	SDRAM10	OUT	SDRAM clock output.
30, 31, 32, 33, 36, 37, 38, 39, 42, 43	SDRAM (9:0)	OUT	SDRAM clock outputs.
44	SDATA	IN	Data input for I^2C serial input, 5V tolerant input
46, 47	CPUCLK (1:0)	OUT	2.5V CPU clocks

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

3: Internal Pull-down resistor of 120K to GND on indicated inputs.

General Description

The **ICS9248-172** is a main clock synthesizer chip for PII/III based systems with ALI 1651 style chipset. This provides all clocks required for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-172 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Mode Pin - Power Management Input Control

MODE, Pin 18 (Latched Input)	Pin 20	Pin 25	Pin 26	Pin 27
0	PCICLK5 (Output)	PD# (Input)	CPU_STOP# (Input)	PCI_STOP# (Input)
1	PD# (Input)	SDRAM12 (Output)	SDRAM11 (Output)	SDRAM10 (Output)

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description										PWD
		FS3	FS2	FS1	FS0	CPUCLK	SDRAM	PCICLK	AGP	Spread Precentage	
	Bit2	Bit7	Bit6	Bit5	Bit4	(MHz)	(MHz)	(MHz)	(MHz)		
Bit 2, Bit 7:4	0	0	0	0	0	66.66	66.66	33.33	66.66	+/- 0.25% Center Spread	00000 Note1
	0	0	0	0	1	66.66	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	0	1	0	100.00	66.66	33.33	66.66	+/- 0.25% Center Spread	
	0	0	0	1	1	100.00	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	0	0	100.00	133.33	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	0	1	133.33	66.66	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	1	0	133.33	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	1	1	133.33	133.33	33.33	66.66	+/- 0.25% Center Spread	
	0	1	0	0	0	66.66	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	0	1	66.66	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	1	0	100.00	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	1	1	100.00	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	0	0	100.00	133.33	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	0	1	133.33	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	1	0	133.33	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	1	1	133.33	133.33	33.33	66.66	0 to -0.5% Down Spread	
	1	0	0	0	0	69.99	69.99	35.00	69.99	+/- 0.25% Center Spread	
	1	0	0	0	1	69.99	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	0	1	0	105.00	69.99	35.00	69.99	+/- 0.25% Center Spread	
	1	0	0	1	1	105.00	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	0	0	105.00	140.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	0	1	140.00	69.99	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	1	0	140.00	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	1	1	140.00	140.00	35.00	69.99	+/- 0.25% Center Spread	
	1	1	0	0	0	73.33	73.33	36.66	73.33	+/- 0.25% Center Spread	
	1	1	0	0	1	73.33	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	0	1	0	110.00	73.33	36.66	73.33	+/- 0.25% Center Spread	
	1	1	0	1	1	110.00	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	0	0	110.00	146.66	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	0	1	146.66	73.33	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	1	0	146.66	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	1	1	146.66	146.66	36.66	73.33	+/- 0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4										0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled										0
Bit 0	0 - Running 1- Tristate all outputs										0

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
The I^2C readback of the power up default indicates the revision ID in bits 2, 7:4 as shown.

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3#
Bit 6	10	1	AGP1
Bit 5	9	1	AGP0
Bit 4	22	1	48MHz
Bit 3	2	1	IOAPIC
Bit 2	7	1	REF0 - 1X or 2X default = 1=1X
Bit 1	46	1	CPUCLK1
Bit 0	47	1	CPUCLK0

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	MODE#
Bit 6	20	1	PCICLK5
Bit 5	19	1	PCICLK4
Bit 4	18	1	PCICLK3
Bit 3	15	1	PCICLK2
Bit 2	14	1	PCICLK1
Bit 1	13	1	PCICLK0
Bit 0	12	1	PCICLK_F

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS0#
Bit 6	-	X	FS1#
Bit 5	-	X	FS2#
Bit 4	31	1	SDRAM8
Bit 3	30	1	SDRAM9
Bit 2	27	1	SDRAM10
Bit 1	26	1	SDRAM11
Bit 0	25	1	SDRAM12

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	43	1	SDRAM0
Bit 6	42	1	SDRAM1
Bit 5	39	1	SDRAM2
Bit 4	38	1	SDRAM3
Bit 3	37	1	SDRAM4
Bit 2	36	1	SDRAM5
Bit 1	33	1	SDRAM6
Bit 0	32	1	SDRAM7

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	0	Bit (1:0) = 00 CPU_STOP will stop CPU clocks Bit (1:0) = 01 CPU_STOP will stop CPU, SDRAM, AGP clocks
Bit 0	-	0	Bit (1:0) = 10 CPU_STOP will stop CPU, SDRAM clocks Bit (1:0) = 11 CPU_STOP will stop CPU, AGP clocks

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	1	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage $V_{DD = 3.3V}$, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			77	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz			100	
Input frequency	F_i	V_{DD} = 3.3 V;	12		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V			1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew[1]	t_{sk1}	V_T = 1.5 V			500	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.5 V			250	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V			150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-500		500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-54	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41			mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45		55	%
Skew[1]	T_{sk1}	V_T = 1.5 V			250	ps
Propagation Delay	Tprop	VT = 1.5 V			5	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19			mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V			2	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45		55	%
Jitter, One Sigma[1]	T_{j1s4B}	V_T = 1.25 V			0.5	ns
Jitter, Absolute[1]	T_{jabs4B}	V_T = 1.25 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz, REF

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V			0.5	ns
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-172 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

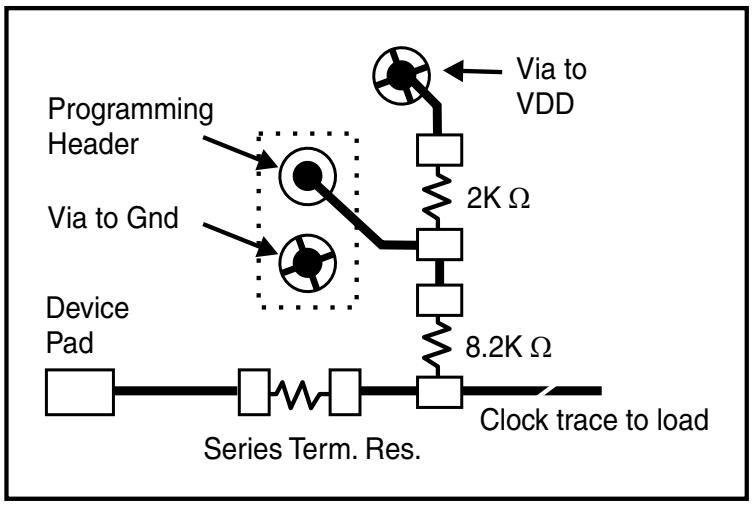
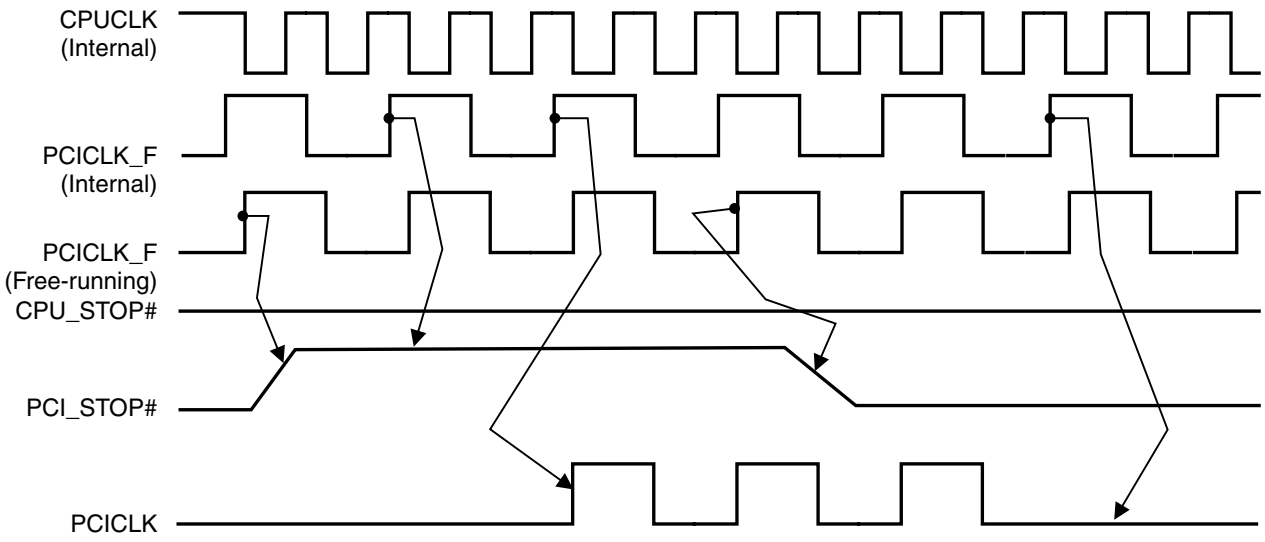


Fig. 1

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-172**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-172** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

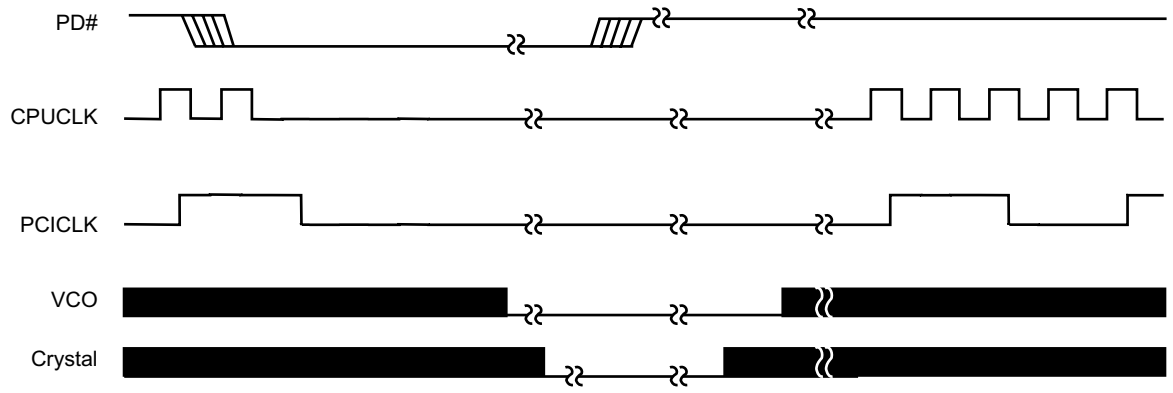


Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-172 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-172.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

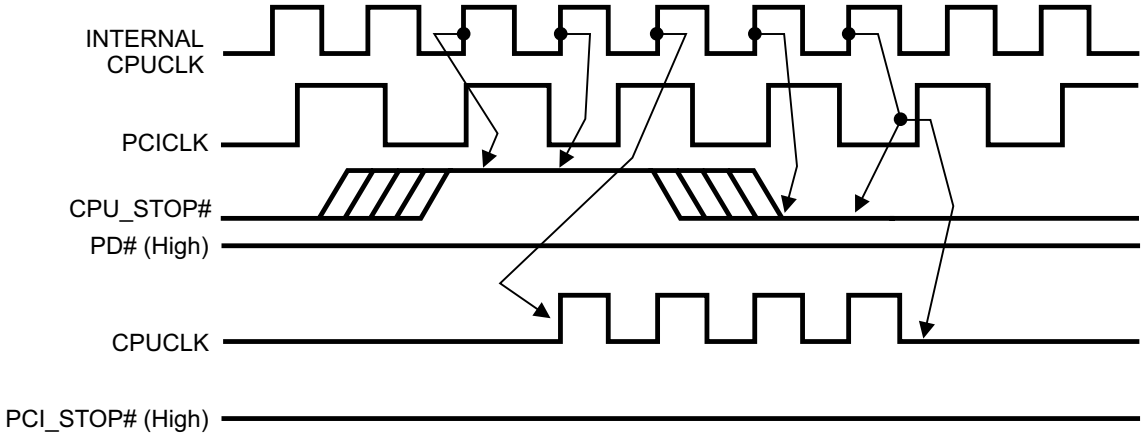


Notes:

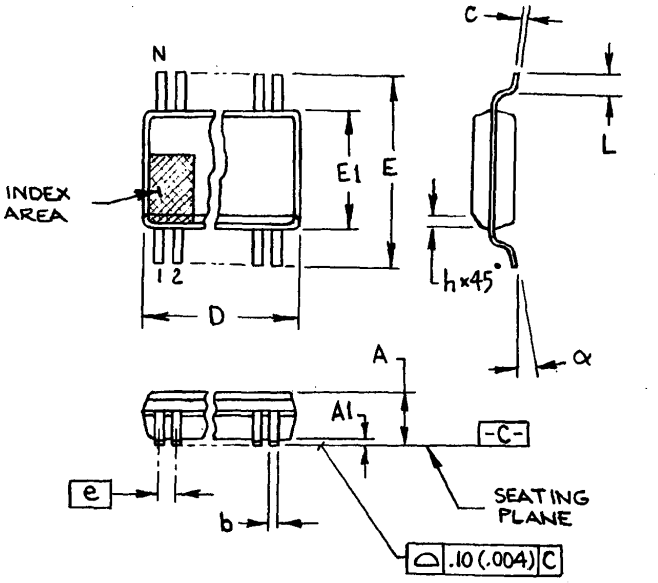
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-172 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-172**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



Notes:
1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-172.
3. All other clocks continue to run undisturbed.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

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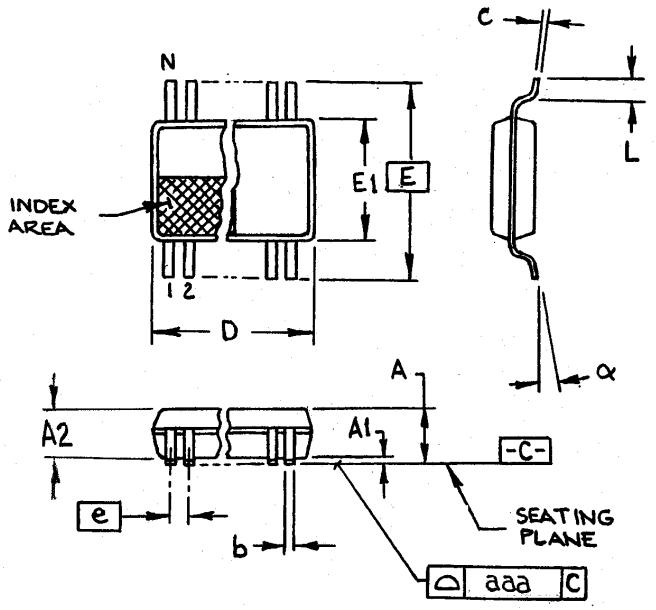
Ordering Information

ICS9248yF-172-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device



6.10 mm. Body, 0.50 mm. pitch TSSOP (240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

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Ordering Information

ICS9248yG-172-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device