Integrated Circuit Systems, Inc.

ICS9148-46

Pentium/Pro™ System Clock Chip

General Description

The **ICS9148-46** is part of a reduced pin count two-chip clock solution for designs using an Intel BX style chipset. Companion SDRAM buffers are ICS9179-03, and -12.

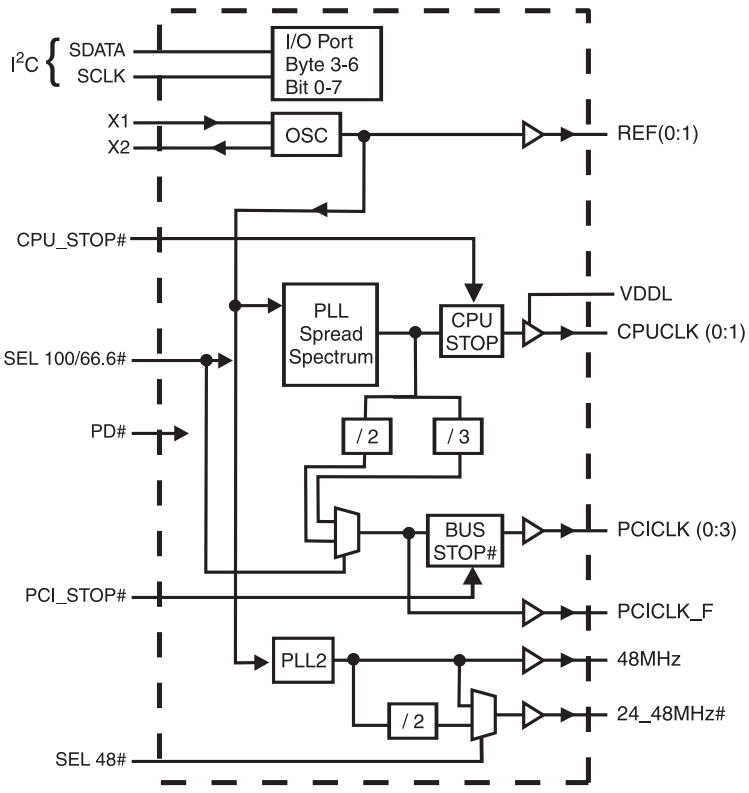
There are two PLLs, with the first PLL capable of spread spectrum operation. Spread spectrum typically reduces system EMI by 8-10dB. The second PLL provides support for USB (48MHz) and 24MHz requirements. CPU frequencies up to 100MHz are supported.

The I^2C interface allows stop clock programming, frequency selection, and spread spectrum operation to be programmed. Clock outputs include two CPU (2.5V or 3.3V), five PCI (3.3V), two REF (3.3V), one 48MHz, and one selectable 48_24MHz.

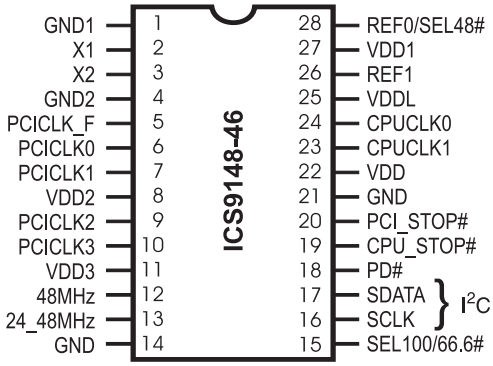
Features

- Generates system clocks for CPU, PCI, 14.314 MHz, 48 and 24MHz.
- Supports single or dual processor systems
- Skew from CPU (earlier) to PCI clock 1 to 4ns
- Separate 2.5V and 3.3V supply pins
- 2.5V outputs: CPU
- 3.3V outputs: PCI, REF
- No power supply sequence requirements
- 28 pin SSOP
- Spread Sectrum operation optional for PLL1
- CPU frequencies to 100MHz are supported.

Block Diagram



Pin Configuration



28 pin SSOP

Power Groups

VDD = Supply for PLL core
VDD1 = REF(0:1), X1, X2
VDD2 = PCICLK_F, PCICLK (0:3)
VDD3 = 48MHz, 24/48MHz
VDDL = CPUCLK (0:1)

Ground Groups

GND = Ground Source Core, CPUCLK (0:1)
GND1 = REF(0:1), X1, X2
GND2 = PCICLK_F, PCICLK (0:5)
GND3=48MHz, 24/48MHz

Pentium is a trademark on Intel Corporation.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND1	PWR	Ground for REF (0:1), X1, X2.
2	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
3	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
4	GND2	PWR	Ground for PCI outputs
5	PCICLK_F	OUT	Free Running PCI output. Not affected by PCI_STOP#
6, 7, 9, 10	PCICLK (0:3)	OUT	PCI clock outputs. TTL compatible 3.3V
8	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V
11	VDD3	PWR	Poer for 48MHz
12	48MHz	OUT	Fixed CLK output @ 48MHz
13	24_48MHz	OUT	Fixed CLK output; 24MHz if pin 27 =1 at power up, 48MHz if pin 27=0 at power up.
14	GND3	PWR	Ground for 48MHz
15	SEL100/66.6#	IN	Select pin for enabling 100MHz or 66.6MHz H=100MHz, L=66.6MHz (PCI always synchronous 33.3MHz)
16	SCLK	IN	Clock input for I^2C input
17	SDATA	IN	Data input for I^2C input
18	PD#	IN	Asynchronous input when driven active (LOW) disables internal clocks, stops VCO early. All outputs are placed in a LOW state at the end of the curent cycle.
19	CPU_STOP#	IN	Asynchronous input when driven active (LOW) stops CPUCLK(0:1) in a LOW state.
20	PCI_STOP#	IN	Asynchronous input when driven active (LOW) stops PCICLK(0:3) in a LOW state. PCICLK_F is not affected.
21	GND	PWR	Ground for CPUCLK (0:1) and the core
22	VDD	PWR	Power for PLL core
23, 24	CPUCLK (1:0)	OUT	CPU and Host clock outputs nominally 2.5V
25	VDDL	PWR	Power for CPU outputs, nominally 2.5V
26	REF1	OUT	14.318MHz Reference clock output
27	VDD1	PWR	Power for REF outputs.
28	REF0	OUT	14.318MHz clock output
	SEL 48#	IN	Latched input at power up. When low, pin 13 is 48MHz.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controler (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Bitmap

Byte 3: Functionality & Frequency Select & Spread Slect Register

Bit	Description			PWD
7	0: Center Spread ±0.255% 1: Down Spread 0 to -0.6%			0
6:4	Bit 654	CPU	PCI	
	000	68.5	34.25	0
	001	75.0	37.5	
	010	83.3	41.6	
	011	66.6	33.3	
	100	103	34.3	
	101	112	37.3	
	110	133.3	44.43	
	111	100	33.33	
3	0 - Frequency is selected by hardware select SEL100/66.6# 1 - Frequency is selected by 6:4 above			0
2	(Reserved)			
10	00 - Normal operation 01 - Test mode 10 - Spread sprectrum ON 11 - Tristate all outputs			00

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	-	-	-	(Reserved)	(Reserved)
6	-	-	-	(Reserved)	(Reserved)
5	-	-	-	(Reserved)	(Reserved)
4	-	-	-	(Reserved)	(Reserved)
3	-	-	-	(Reserved)	(Reserved)
2	23	CPUCLK1	1	Disabled (low)	Enabled
1	-	-	0	(Reserved)	(Reserved)
0	24	CPUCLK0	1	(Disabled) (low)	Enabled

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

Byte 5:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	5	PCICLK_F	1	Disabled (low)	Enabled
6	10	PCICLK3	1	Disabled (low)	Enabled
5	9	PCICLK2	1	Disabled (low)	Enabled
4	-	-	0	(Reserved)	(Reserved)
3	7	PCICLK1	1	Disabled (low)	Enabled
2	6	PCICLK0	1	Disabled (low)	Enabled
1	-	-	0	(Reserved)	(Reserved)
0	-	-	0	(Reserved)	(Reserved)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 6:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	-	-	0	(Reserved)	(Reserved)
6	-	-	0	(Reserved)	(Reserved)
5	-	-	0	(Reserved)	(Reserved)
4	-	-	0	(Reserved)	(Reserved)
3	-	-	0	(Reserved)	(Reserved)
2	26	REF1	1	(Disabled) (low)	Enabled
1	-	-	0	(Reserved)	(Reserved)
0	28	REF0	1	(Disabled) (low)	Enabled

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz		60	170	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz		66	170	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		3	650	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{AGP-PCI1}$	V_T = 1.5 V;	1	3.5	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	C_L = 0 pF; Select @ 66.8 MHz		16	72	mA
	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		23	100	mA
Power Down Supply Current	$I_{DD2.5PD}$	C_L = 0 pF; With input address to Vdd or GND		10	100	µA
Skew[1]	$t_{CPU-AGP}$		0	0.5	1	ns
	$t_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V	1	2.6	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.2	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-41	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	37		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.25	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	48	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		30	175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		150	250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V		40	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	140	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.1	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	57		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		140	500	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V		17	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-500	70	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	3.1		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.17	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-44	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	29	42		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	47	54	57	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		1	3	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V		3	5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48, 24 MHz

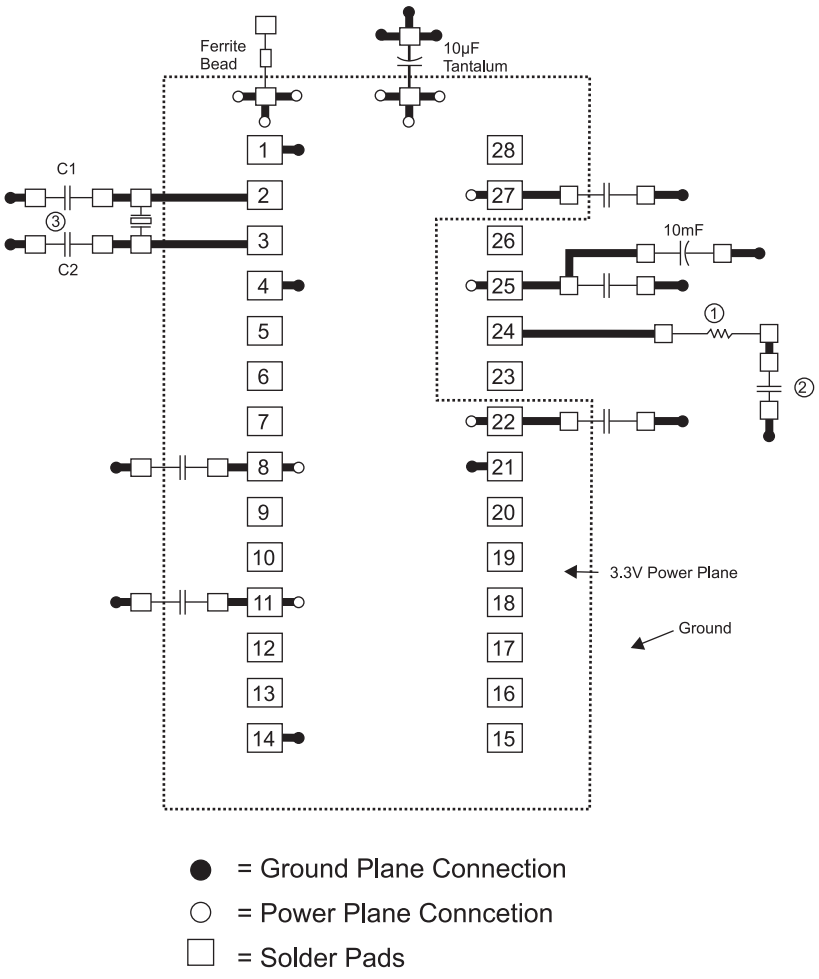
T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	3		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.14	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-44	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	42		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52	55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		1	3	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V		3	5	%

[1]Guaranteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.



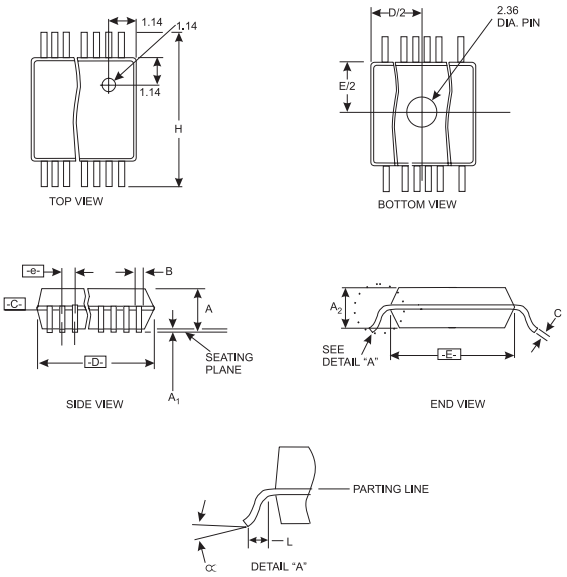
Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
3 Optional crystal load capacitors are recommended.

Capacitor Values:

C1, C2 : Crystal load values determined by user

All unmarked capacitors are 0.01µF ceramic



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.	N	MIN.	NOM.	MAX.
A	0.068	0.073	0.078	14	0.239	0.244	0.249
A1	0.002	0.005	0.008	16	0.239	0.244	0.249
A2	0.066	0.068	0.070	20	0.278	0.284	0.289
b	0.010	0.012	0.015	24	0.318	0.323	0.328
c	0.004	0.006	0.008	28	0.397	0.402	0.407
D	See Variations			30	0.397	0.402	0.407
E	0.205	0.209	0.212				
e		0.0256 BSC					
H	0.301	0.307	0.311				
L	0.025	0.030	0.037				
N	See Variations						
∝	0°	4°	8°				

28 Pin SSOP Package

Ordering Information

ICS9148yF-46

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device