

## Low Skew Output Buffer

### General Description

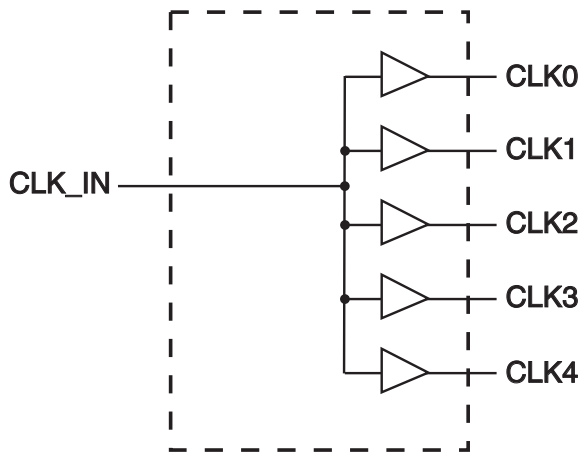
The ICS9112-28 is a high performance, low skew, low jitter clock driver. It is designed to distribute high speed clocks in PC systems operating at speeds from 0 to 133 MHz.

The ICS9112-28 comes in an eight pin 150 mil SOIC package. It has four output clocks.

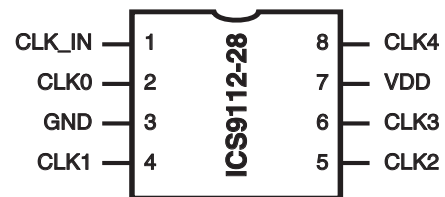
### Features

- Frequency range 0 - 133 MHz (3.3V)
- Less than 200 ps Jitter between outputs
- Skew controlled outputs
- Skew less than 250 ps between outputs
- Available in 8 pin 150 mil SOIC & 173 mil TSSOP packages.
- 3.3V  $\pm$ 10% operation

### Block Diagram



### Pin Configuration



**8 pin SOIC**

### Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CLK_IN	IN	Input reference frequency.
2	CLK0 <sup>1</sup>	OUT	Buffered clock output
3	GND	PWR	Ground
4	CLK1 <sup>1</sup>	OUT	Buffered clock output
5	CLK2 <sup>1</sup>	OUT	Buffered clock output
6	CLK3 <sup>1</sup>	OUT	Buffered clock output
7	VDD	PWR	Power Supply (3.3V)
8	CLK4 <sup>1</sup>	OUT	Buffered clock output

Notes:

1. Weak pull-down on all outputs

# ICS9112-28

## Preliminary Product Preview



### Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs	GND –0.5 V to V <sub>DD</sub> +0.5 V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics at 3.3V

V<sub>DD</sub> = 3.0 – 3.6 V, T<sub>A</sub> = 0 – 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V <sub>IL</sub>				0.8	V
Input High Voltage	V <sub>IH</sub>		2.0			V
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> =0V			50.0	μA
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> =V <sub>DD</sub>			100.0	μA
Output Low Voltage <sup>1</sup>	V <sub>OL</sub>	I <sub>OL</sub> = 8mA			0.4	V
Output High Voltage <sup>1</sup>	V <sub>OH</sub>	I <sub>OH</sub> = 8mA	2.4			V
Supply Current	I <sub>DD</sub>	REF = 0 MHz			50.0	μA
Supply Current	I <sub>DD</sub>	Unloaded outputs at 66.66 MHz			40.0	mA

Notes:

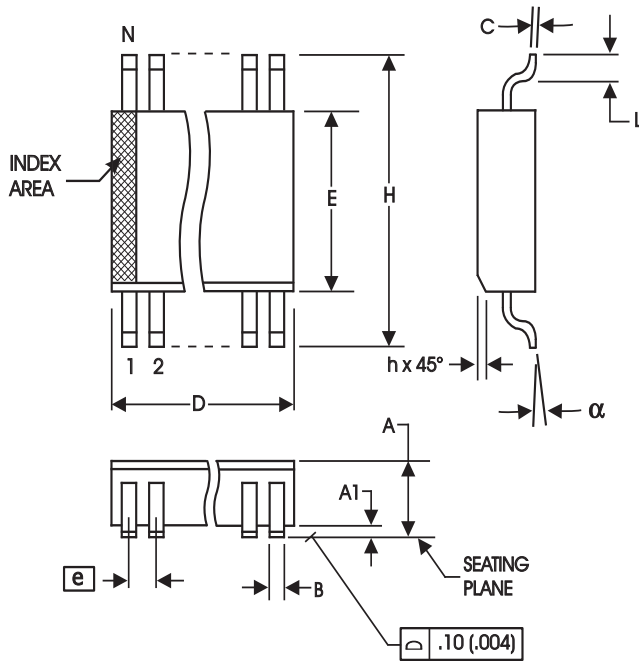
1. Guaranteed by design and characterization. Not subject to 100% test.
2. All Skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

### Switching Characteristics (3.3V Continued)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Propagation delay	tp		4.5		8.0	ns
Rise Time <sup>1</sup>	tr1	Measured between 0.8V and 2.0V; CL=30pF @ all operating frequencies			1.5	ns
Fall Time <sup>1</sup>	tf1	Measured between 2.0V and 0.8V; CL=30pF @ all operating frequencies			1.5	ns
Output to Output Skew <sup>1</sup>	Tskew	All outputs equally loaded, CL=20pF			250	ps
Device to Device Skew <sup>1</sup>	Tdsk-Tdsk	Measured at VDD/2 on the CLKOUT pins of devices			700	ps

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. CLK\_IN input has a threshold voltage of 1.4V
3. All parameters expected with loaded outputs



**150 mil (Narrow Body) SOIC**

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SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

**VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968

Reference Doc.: JEDEC Publication 95, MS-012  
10-0030

## Ordering Information

**ICS9112yM-28LF-T**

Example:

**ICS XXXX y M - PPP LF - T**

