Document Title

512 K x 16 bit Low Voltage and Ultra Low Power CMOS Static RAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	January 3,2002	
0B	1. Add CE2 pin for 48 pin TF-BGA 2. Change for I_{CC}: 35 mA to 30 mA for 55 ns Industrial product 30 mA to 25 mA for 70 ns Industrial product 25 mA to 20 mA for 100 ns Industrial product 30 mA to 25 mA for 55 ns Commerical product 25 mA to 20 mA for 70 ns Commerical product 20 mA to 15 mA for 100 ns Commerical product 3. Change for I_{SB2}: 20 µA to 15 µA for Commerical product 4. Change for I_{DR}: 15 µA to 20 µA for Commerical/L product 6 µA to 13 µA for Commerical/LL product 20 µA to 30 µA for Industrial/L product 9 µA to 23 µA for Industrial/LL product	September 2,2002	
0C	1. Revise typo for pin assignment H1 from NC to A18 2. Change Truth Table of LB/UB control,$\overline{CE}$1 and CE2 to "Don't care" 3. Change DC parameters for TSOP-2 package as follows (1)V_{IH} : 2.2V to 2.8V (2)$I_{SB}1$: 0.2mA to 0.7mA for commercial product 0.3mA to 0.8mA for Industrial product (3)$I_{SB}2$: 15µA to 20µA for commercial/LL product 25µA to 30µA for Industrial/LL product (4)I_{CC} : 25mA to 30mA for commercial/LL product 30mA to 35mA for Industrial/LL product	January 22,2003	

512K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

FEATURES

- High-speed access times: 55, 70, 100 ns
- CMOS low power operation
  I_{CC}=18mA (typical)* operating
  I_{SB2}=3µA (typical)* CMOS standby
- TTL compatible interface levels
- Single 2.7V-3.6V Vcc power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in the know good die from 44-pin TSOP-2 and 48-pin 8x10mm TF-BGA
- CE2 pin only for 48-pin TF-BGA.

* Typical values are measured at V_{CC}=3.0V, T_A=25°C

DESCRIPTION

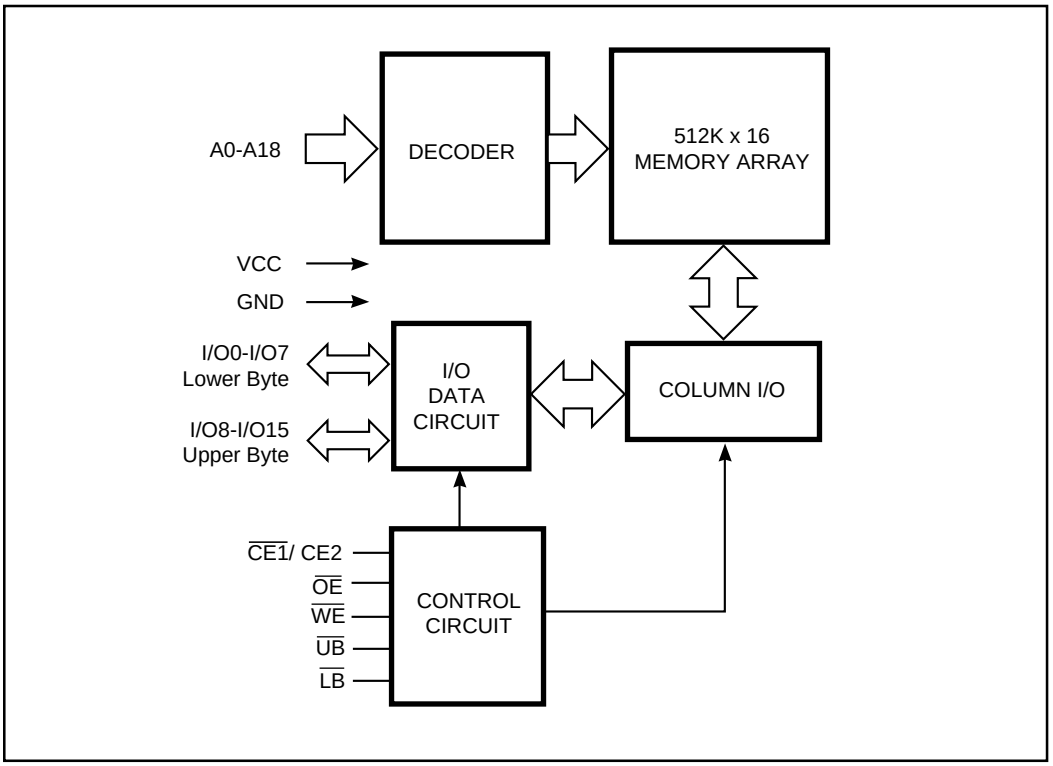
The *ICSI* IC62LV51216L and IC62LV51216LL are low-power, 8.388,608 bit static RAMs organized as 524,288 words by 16 bits. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or when CE2 is low (deselected) or both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using Chip Enable Output and Enable inputs, $\overline{CE1}$, CE2 and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

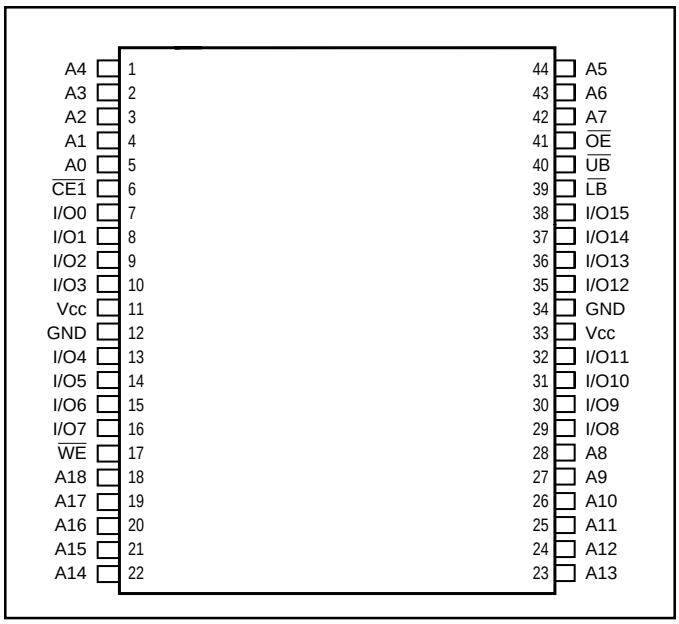
The IC62LV51216L and IC62LV51216LL are packaged in the JEDEC standare 44-pin TSOP-2 and 48-pin 8*10mm TF-BGA.

FUNCTIONAL BLOCK DIAGRAM

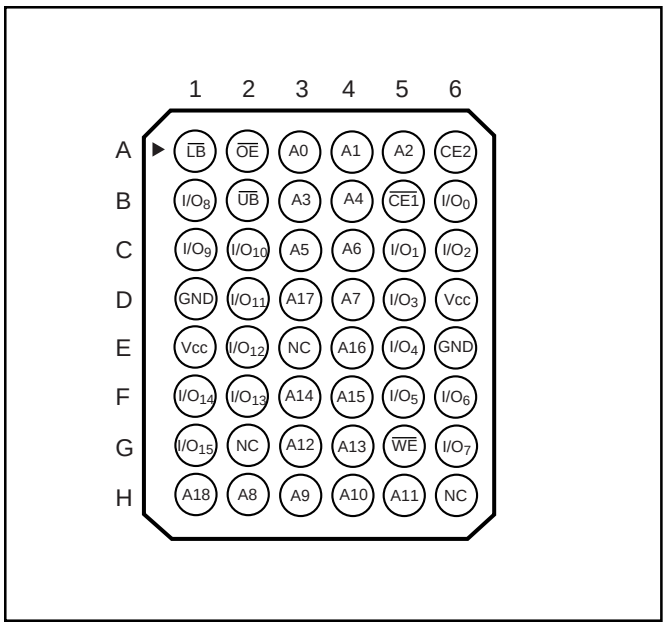


PIN CONFIGURATIONS

44-Pin TSOP-2



48-Pin TF-BGA (TOP View)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Input/Output
$\overline{CE1}$	Chip Enable1 Input
CE2	Chip Enable2 Input, BGA only
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0/-I/O7	I/O PIN I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	Standby
	X	X	L	X	X	X	High-Z	High-Z	Standby
	X	X	X	X	H	H	High-Z	High-Z	Standby
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	Active
	H	L	H	H	X	L	High-Z	High-Z	Active
Read	H	L	H	L	L	H	DOUT	High-Z	Active
	H	L	H	L	H	L	High-Z	DOUT	Active
	H	L	H	L	L	L	DOUT	DOUT	Active
Write	L	L	H	X	L	H	DIN	High-Z	Active
	L	L	H	X	H	L	High-Z	DIN	Active
	L	L	H	X	L	L	DIN	DIN	Active

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V- 3.6V
Industrial	–40°C to +85°C	2.7V - 3.6V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{CC}	Vcc related to GND	–0.3 to +4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA	2.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage		2.2 2.8*	V_{CC} + 0.2 V_{CC} + 0.2	V
V_{IL}(2)	Input LOW Voltage(1)		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Notes:
1. V_{IH}(max.) = Vcc + 0.2V for pulse width less than 10ns.
2. V_{IL}(min.) = –2.0V for pulse width less than 10 ns.
*. For TSOP-2

CAPACITANCE(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input Reference Level	1.3V
Output Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

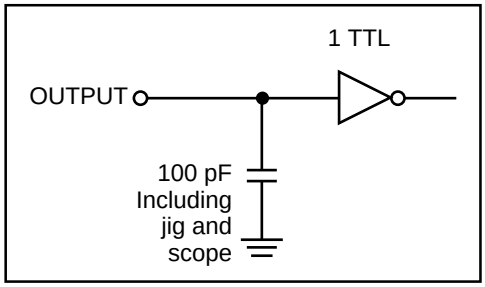


Figure 1

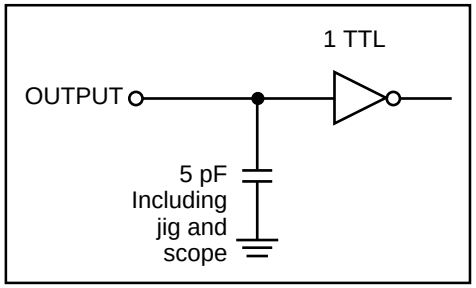


Figure 2

IC62LV51216L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = 3.0V., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	30	—	25	—	20	mA
			Ind.	—	35	—	30	—	25	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, f = 0	Com.	—	0.2	—	0.2	—	0.2	mA
			Ind.	—	0.3	—	0.3	—	0.3	
		$\overline{CE}1$ = V_{IH}, CE2 = V_{IL}	Com.	—	0.7*	—	0.7*	—	0.7*	
			Ind.	—	0.8*	—	0.8*	—	0.8*	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}1 \geq V_{CC} - 0.2V$, or CE2 ≤ 0.2V other input = 0-V_{CC}, f = 0	Com.	—	35	—	35	—	35	µA
			Ind.	—	50	—	50	—	50	
	OR									
	ULB Control	V_{CC} = Max., $\overline{CE}1$ = V_{IL}, CE2 = V_{IH} $V_{IN} \leq 0.2V$, f = 0, $\overline{UB}$ / $\overline{LB} \geq V_{CC} - 0.2V$								

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
*.For TSOP-2

IC62LV51216LL POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = 3.0V I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind. Com. Ind.	— — — —	25 30 30* 35*	— — — —	20 25 25* 30*	— — — —	15 20 20* 25*	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}1$ = V_{IH}, CE2 = V_{IL}	Com. Ind. Com. Ind.	— — — —	0.2 0.3 0.7* 0.8*	— — — —	0.2 0.3 0.7* 0.8*	— — — —	0.2 0.3 0.7* 0.8*	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 $\overline{CE}1 \geq V_{CC} - 0.2V$, or CE2 ≤ 0.2V other input = 0-V_{CC}, f = 0 **OR**	Com. Ind. Com. Ind.	— — — —	15 25 20* 30*	— — — —	15 25 20* 30*	— — — —	15 25 20* 30*	µA
	ULB Control	V_{CC} = Max., $\overline{CE}1$ = V_{IL}, CE2 = V_{IH} $V_{IN} \leq 0.2V$, f = 0, $\overline{UB}$ / $\overline{LB} \geq V_{CC} - 0.2V$								

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
*. For TSOP-2

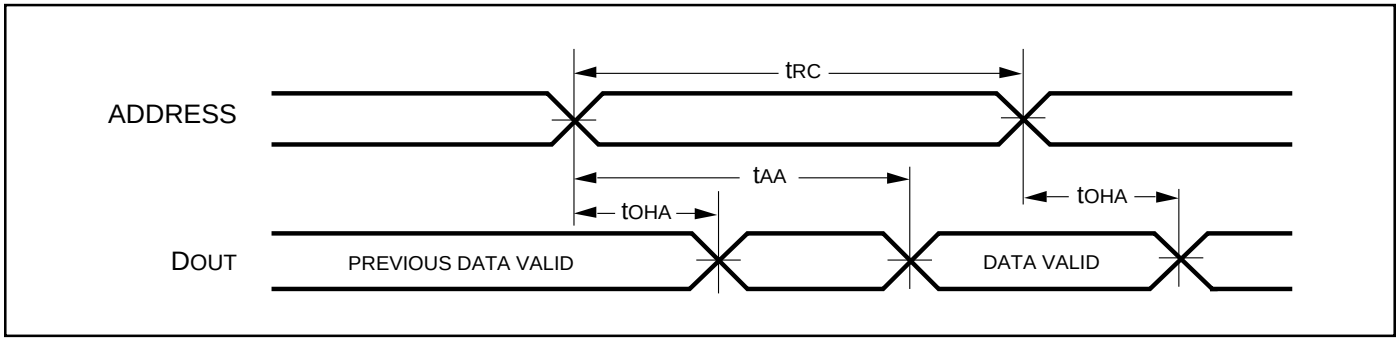
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	100	ns
t_{OHA}	Output Hold Time	10	—	10	—	15	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	55	—	70	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	30	—	38	—	50	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	—	30	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZCE}[2]	$\overline{CE}$1 or CE2 to High-Z Output	0	20	0	25	0	30	ns
t_{LZCE}[2]	$\overline{CE}$1 and CE2 to Low-Z Output	10	—	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	—	100	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ o High-Z Output	0	25	0	25	0	35	ns
t_{LZB}	$\overline{LB}$. $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

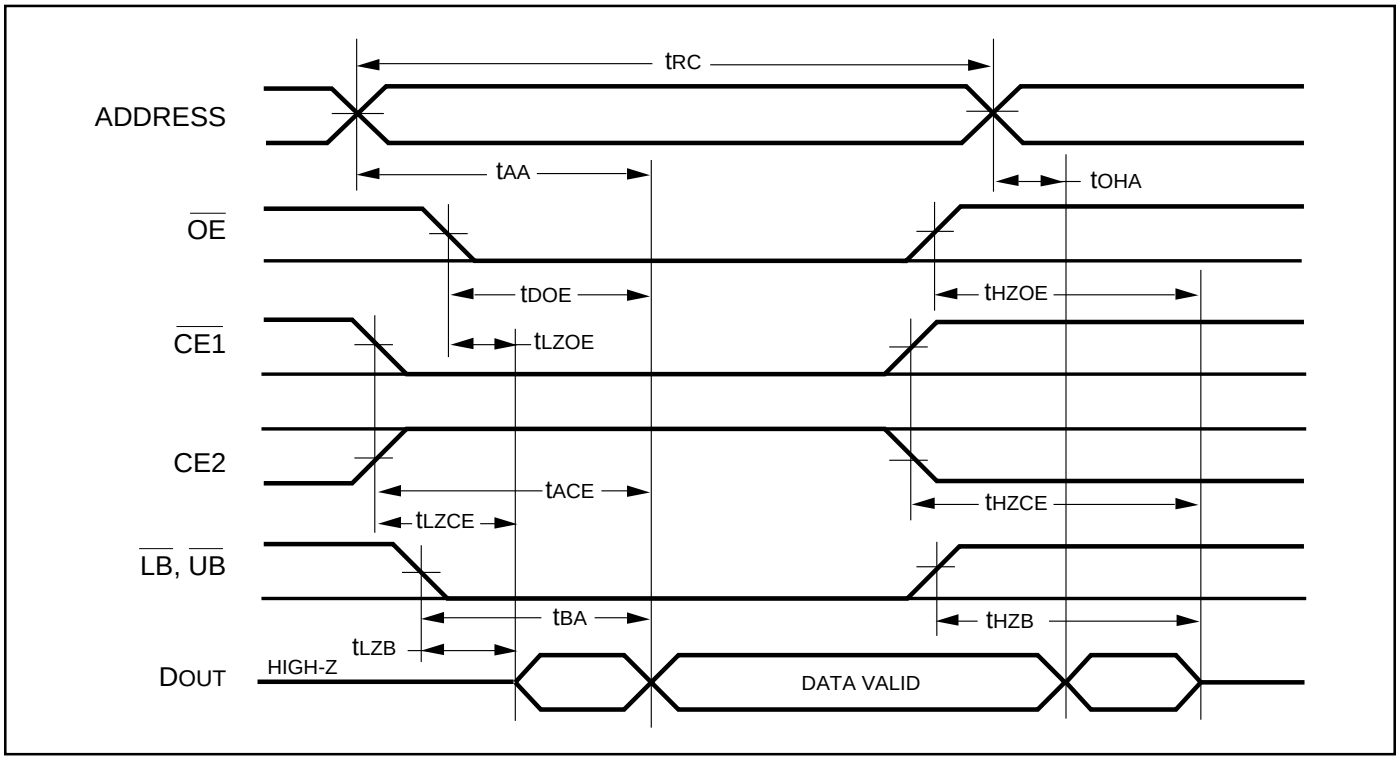
AC TEST LOADS

READ CYCLE NO.1[1,2] (Address Controlled) ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{OE}$, Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}, CE2 = V_{IH}
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

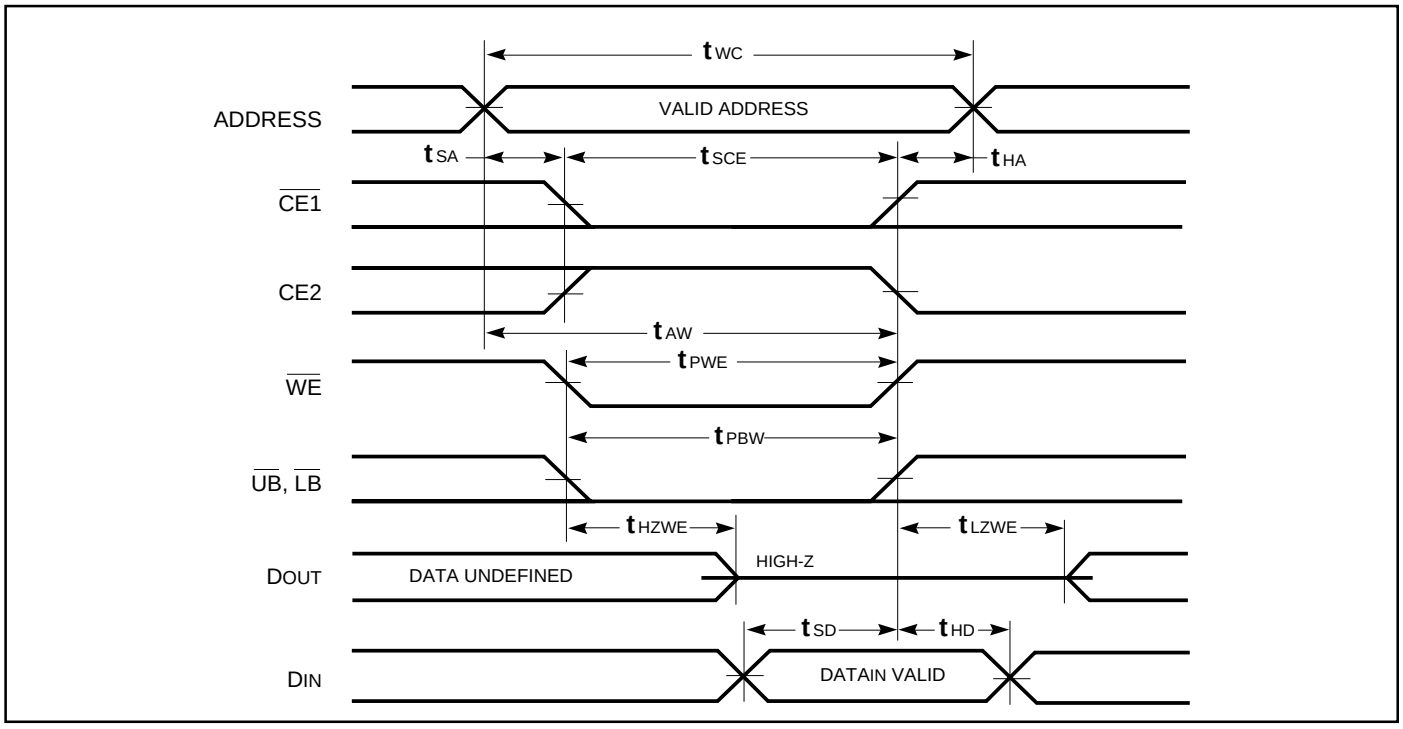
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max	Unit
t_{WC}	Write Cycle Time	55	—	70	—	100	—	ns
t_{SCE}	$\overline{CE1}$ Low and CE2 HIGH to Write End	50	—	65	—	80	—	ns
t_{AW}	Address Setup Time to Write End	50	—	65	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	80	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	45	—	55	—	80	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	30	—	30	—	40	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, and $\overline{UB}$ or $\overline{LB}$, $\overline{WE}$ LOW, and CE2 HIGH. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

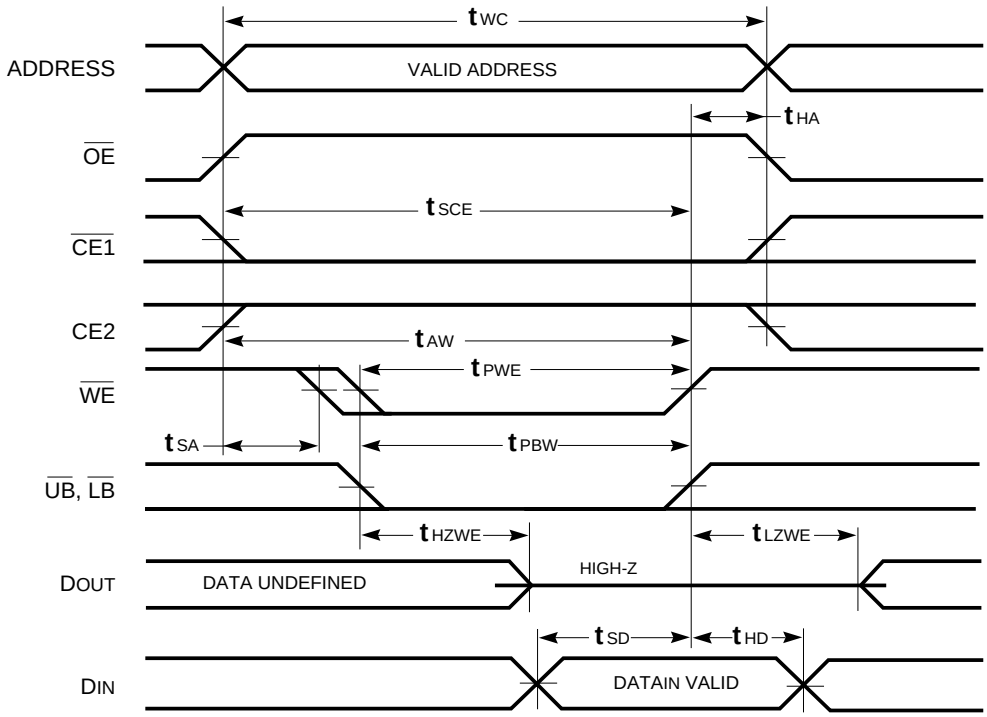
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE1}$ or CE2, Controlled, $\overline{OE}$ = HIGH or LOW)

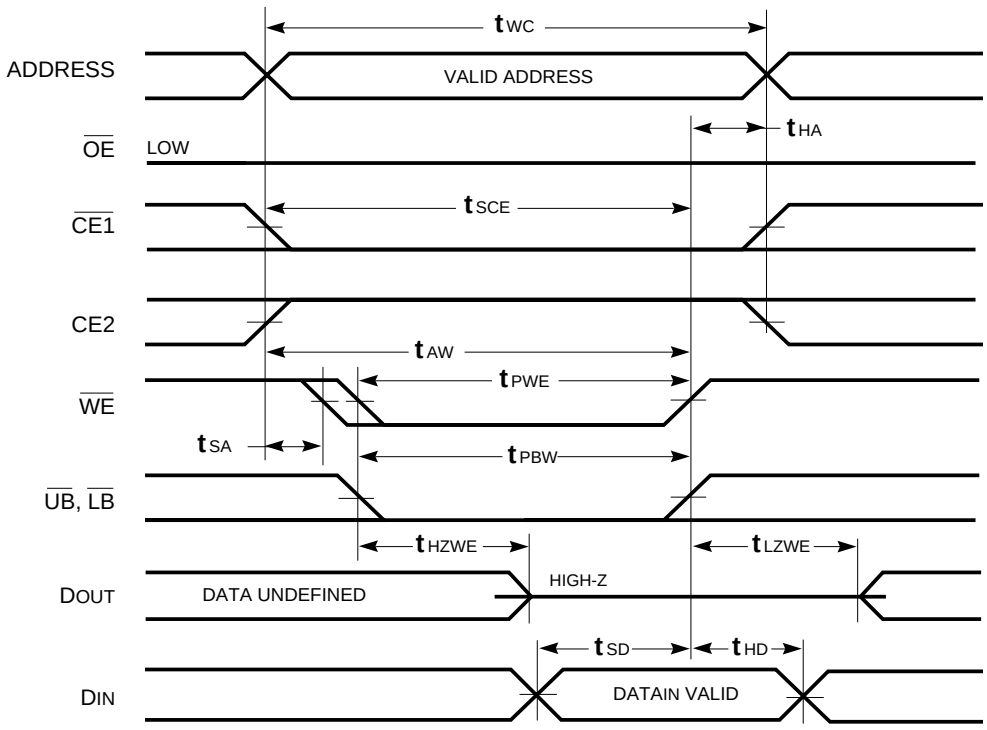


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the $\overline{WE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH} and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.

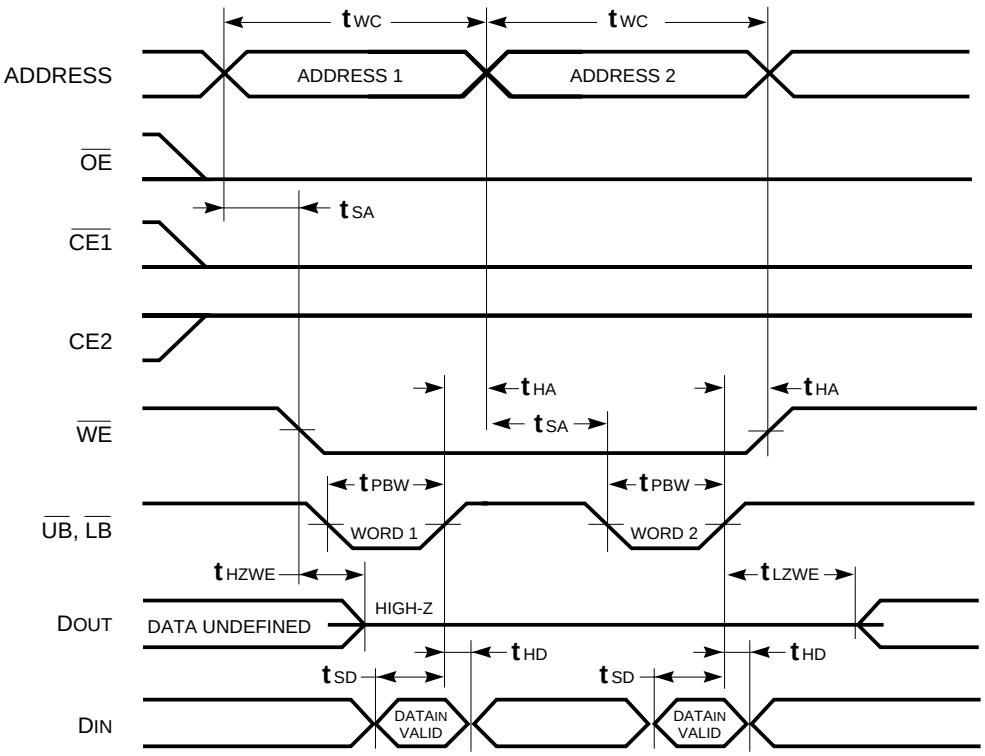
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled; $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled; $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}$ / $\overline{LB}$ Controlled)

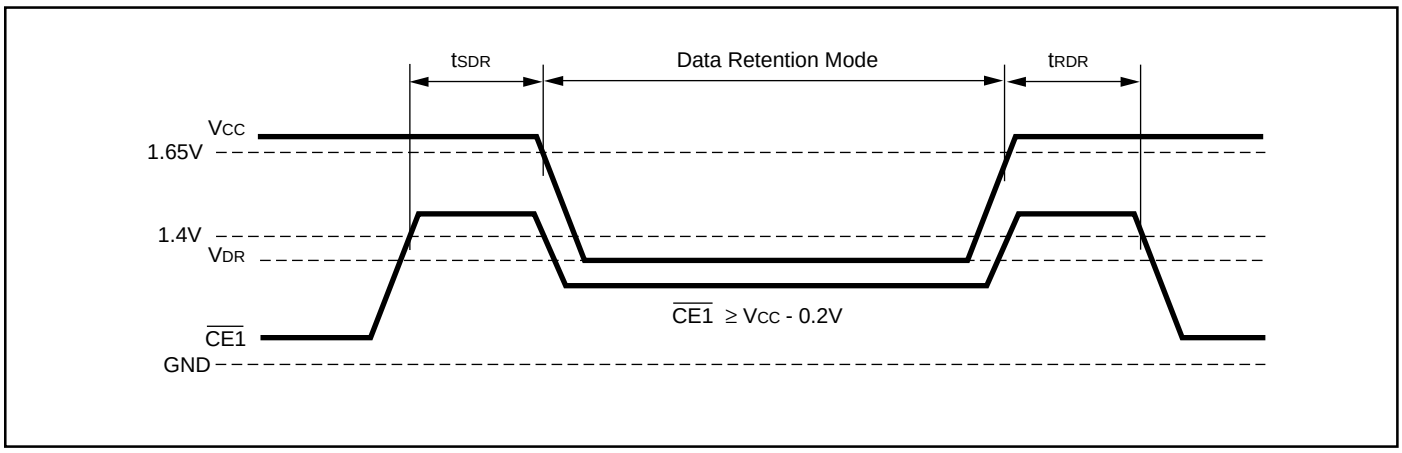


DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		1.5	3.6	V
I_{DR}	Data Retention Current	V_{CC} = 1.5V, $\overline{CE1} \geq V_{CC} - 0.2V$[1]	Com. (-L)	—	20	µA
			Com. (-LL)	—	13	
			Ind. (-L)	—	30	
			Ind. (-LL)	—	23	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		10	—	ns

Notes:
1. 1) $\overline{CE1} \geq V_{CC}$ -0.2V, CE2 ≥ V_{CC} -0.2V, ($\overline{CE1}$ controlled) or
   2) 0V ≤ CE2 ≤ 0.2V (CE2 controlled) or
   3) $\overline{LB}$ = $\overline{UB} \geq V_{CC}$ -0.2V, CE2 ≥ V_{CC} -0.2V ($\overline{LB}$/$\overline{UB}$ controlled)

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216L-55T	TSOP-2
	IC62LV51216L-55B	8*10mm TF-BGA
70	IC62LV51216L-70T	TSOP-2
	IC62LV51216L-70B	8*10mm TF-BGA
100	IC62LV51216L-100T	TSOP-2
	IC62LV51216L-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216L-55TI	TSOP-2
	IC62LV51216L-55BI	8*10mm TF-BGA
70	IC62LV51216L-70TI	TSOP-2
	IC62LV51216L-70BI	8*10mm TF-BGA
100	IC62LV51216L-100TI	TSOP-2
	IC62LV51216L-100BI	8*10mm TF-BGA

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216LL-55T	TSOP-2
	IC62LV51216LL-55B	8*10mm TF-BGA
70	IC62LV51216LL-70T	TSOP-2
	IC62LV51216LL-70B	8*10mm TF-BGA
100	IC62LV51216LL-100T	TSOP-2
	IC62LV51216LL-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV51216LL-55TI	TSOP-2
	IC62LV51216LL-55BI	8*10mm TF-BGA
70	IC62LV51216LL-70TI	TSOP-2
	IC62LV51216LL-70BI	8*10mm TF-BGA
100	IC62LV51216LL-100TI	TSOP-2
	IC62LV51216LL-100BI	8*10mm TF-BGA

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