## Document Title

1Mx4 bit Dynamic RAM with Fast Page Mode

## Revision History

| Revision No | History | Draft Date | Remark |
|---|---|---|---|
| 0A | Initial Draft | August 1,2001 | |

# 1M x 4 (4-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

## FEATURES

- Fast Page Mode Access Cycle
- TTL compatible inputs and outputs
- Refresh Interval:
  -- 1,024 cycles/16 ms
- Refresh Mode: $\overline{RAS}$-Only,
  $\overline{CAS}$-before-$\overline{RAS}$ (CBR), and Hidden
- JEDEC standard pinout
- Single power supply:
  5V ± 10% or 3.3V ± 10%
- Byte Write and Byte Read operation via two $\overline{CAS}$

## DESCRIPTION

The *ICSI* 4105 Series is a 1,048,576 x 4-bit high-performance CMOS Dynamic Random Access Memory. The Fast Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 12 ns per 4-bit word.

These features make the 4105 Series ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The 4105 Series is packaged in a 20-pin 300mil SOJ and a 20 pin TSOP-2

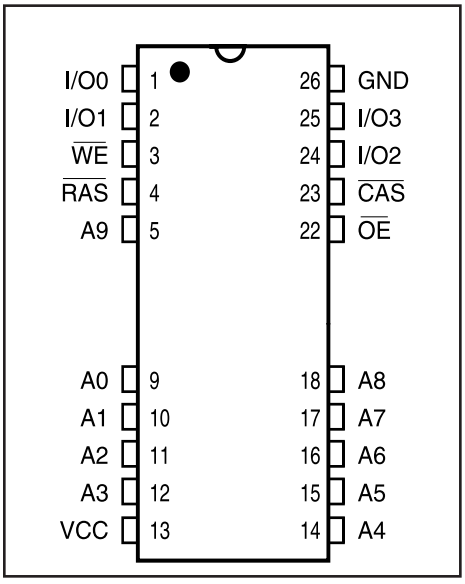
## PRODUCT SERIES OVERVIEW

| Part No. | Refresh | Voltage |
|---|---|---|
| IC41C4105 | 1K | 5V ± 10% |
| IC41LV4105 | 1K | 3.3V ± 10% |

## KEY TIMING PARAMETERS

| Parameter | -35 | -50 | -60 | Unit |
|---|---|---|---|---|
| $\overline{RAS}$ Access Time ($t_{RAC}$) | 35 | 50 | 60 | ns |
| $\overline{CAS}$ Access Time ($t_{CAC}$) | 10 | 14 | 15 | ns |
| Column Address Access Time ($t_{AA}$) | 18 | 25 | 30 | ns |
| Fast Page Mode Cycle Time ($t_{PC}$) | 12 | 20 | 25 | ns |
| Read/Write Cycle Time ($t_{RC}$) | 60 | 90 | 110 | ns |

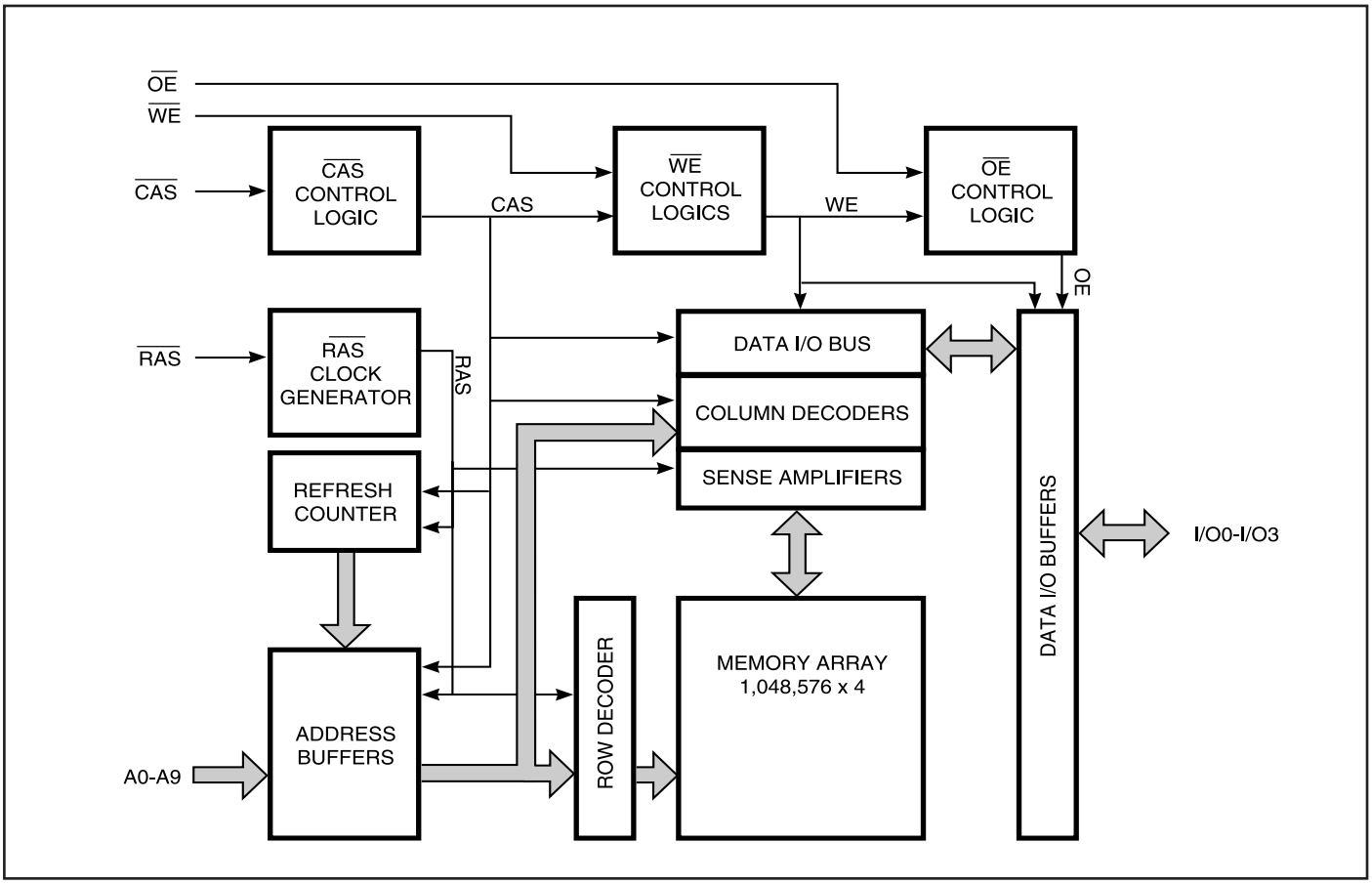
## PIN CONFIGURATION
## 20 (26) Pin SOJ, TSOP-2




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A9 | Address Inputs |
| I/O0-3 | Data Inputs/Outputs |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| Vcc | Power |
| GND | Ground |

## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| Function | | RAS | CAS | WE | OE | Address tR/tC | I/O |
|---|---|---|---|---|---|---|---|
| Standby | | H | H | X | X | X | High-Z |
| Read | | L | L | H | L | ROW/COL | DOUT |
| Write: Word (Early Write) | | L | L | L | X | ROW/COL | DIN |
| Read-Write | | L | L | H→L | L→H | ROW/COL | DOUT, DIN |
| Hidden Refresh | Read | L→H→L | L | H | L | ROW/COL | DOUT |
| | Write[1] | L→H→L | L | L | X | ROW/COL | DOUT |
| RAS-Only Refresh | | L | H | X | X | ROW/NA | High-Z |
| CBR Refresh | | H→L | L | X | X | X | High-Z |

**Note:**
1. EARLY WRITE only.

## Functional Description

The IC41C4105 and IC41LV4105 are CMOS DRAMs optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 10 address bits. These are entered 10 bits (A0-A9) at a time. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address is latched by the Column Address Strobe ($\overline{CAS}$). $\overline{RAS}$ is used to latch the first ten bits and $\overline{CAS}$ is used the latter ten bits.

## Memory Cycle

A memory cycle is initiated by bring $\overline{RAS}$ LOW and it is terminated by returning both $\overline{RAS}$ and $\overline{CAS}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum $t_{RAS}$ time has expired. A new cycle must not be initiated until the minimum precharge time $t_{RP}$, $t_{CP}$ has elapsed.

## Read Cycle

A read cycle is initiated by the falling edge of $\overline{CAS}$ or $\overline{OE}$, whichever occurs last, while holding $\overline{WE}$ HIGH. The column address must be held for a minimum time specified by $t_{AR}$. Data Out becomes valid only when $t_{RAC}$, $t_{AA}$, $t_{CAC}$ and $t_{OE}$ are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

## Write Cycle

A write cycle is initiated by the falling edge of $\overline{CAS}$ and $\overline{WE}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

## Refresh Cycle

To retain data, 1,024 refresh cycles are required in each 16 ms period . There are two ways to refresh the memory:

1. By clocking each of the 1,024 row addresses (A0 through A9) with $\overline{RAS}$ at least once every 16 ms . Any read, write, read-modify-write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated by the falling edge of $\overline{RAS}$, while holding $\overline{CAS}$ LOW. In $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, an internal 10-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{CAS}$-before-$\overline{RAS}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

## Power-On

After application of the $V_{CC}$ supply, an initial pause of 200 µs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ signal).

During power-on, it is recommended that $\overline{RAS}$ track with $V_{CC}$ or be held at a valid $V_{IH}$ to avoid current surges.

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameters | | Rating | Unit |
|---|---|---|---|---|
| $V_T$ | Voltage on Any Pin Relative to GND | 5V | –1.0 to +7.0 | V |
| | | 3.3V | –0.5 to +4.6 | |
| $V_{CC}$ | Supply Voltage | 5V | –1.0 to +7.0 | V |
| | | 3.3V | –0.5 to +4.6 | |
| $I_{OUT}$ | Output Current | | 50 | mA |
| $P_D$ | Power Dissipation | | 1 | W |
| $T_A$ | Commercial Operation Temperature | | 0 to +70 | °C |
| $T_{STG}$ | Storage Temperature | | –55 to +125 | °C |

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 5V | 4.5 | 5.0 | 5.5 | V |
| | | 3.3V | 3.0 | 3.3 | 3.6 | |
| $V_{IH}$ | Input High Voltage | 5V | 2.4 | – | $V_{CC}$ + 1.0 | V |
| | | 3.3V | 2.0 | – | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input Low Voltage | 5V | –1.0 | – | 0.8 | V |
| | | 3.3V | –0.3 | – | 0.8 | |
| $T_A$ | Commercial Ambient Temperature | | 0 | – | 70 | °C |

## CAPACITANCE(1,2)

| Symbol | Parameter | Max. | Unit |
|---|---|---|---|
| $C_{IN1}$ | Input Capacitance: A0-A9 | 5 | pF |
| $C_{IN2}$ | Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | 7 | pF |
| $C_{IO}$ | Data Input/Output Capacitance: I/O0-I/O3 | 7 | pF |

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz.

## ELECTRICAL CHARACTERISTICS[1]

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter | Test Condition | Speed | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | Any input 0V ≤ $V_{IN}$ ≤ Vcc<br>Other inputs not under test = 0V | | –5 | 5 | µA |
| $I_{IO}$ | Output Leakage Current | Output is disabled (Hi-Z)<br>0V ≤ $V_{OUT}$ ≤ Vcc | | –5 | 5 | µA |
| $V_{OH}$ | Output High Voltage Level | $I_{OH}$ = –5.0 mA with $V_{CC}$=5V<br>$I_{OH}$ = –2.0 mA with $V_{CC}$=3.3V | | 2.4 | – | V |
| $V_{OL}$ | Output Low Voltage Level | $I_{OL}$ = 4.2 mA with $V_{CC}$=5V<br>$I_{OL}$ = 2 mA with $V_{CC}$=3.3V | | – | 0.4 | V |
| $I_{CC1}$ | Standby Current: TTL | $\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH}$ | 5V<br>3.3V | –<br>– | 2<br>0.5 | mA |
| $I_{CC2}$ | Standby Current: CMOS | $\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2V | 5V<br>3.3V | –<br>– | 1<br>0.5 | mA |
| $I_{CC3}$ | Operating Current:<br>Random Read/Write[2,3,4]<br>Average Power Supply Current | $\overline{RAS}$, $\overline{CAS}$,<br>Address Cycling, $t_{RC}$ = $t_{RC}$ (min.) | -35<br>-50<br>-60 | –<br>–<br>– | 110<br>95<br>85 | mA |
| $I_{CC4}$ | Operating Current:<br>Fast Page Mode[2,3,4]<br>Average Power Supply Current | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ ≥ $V_{IH}$<br>$t_{RC}$ = $t_{RC}$ (min.) | -35<br>-50<br>-60 | –<br>–<br>– | 90<br>80<br>70 | mA |
| $I_{CC5}$ | Refresh Current:<br>$\overline{RAS}$-Only[2,3]<br>Average Power Supply Current | $\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ $V_{IH}$<br>$t_{RC}$ = $t_{RC}$ (min.) | -35<br>-50<br>-60 | –<br>–<br>– | 110<br>95<br>85 | mA |
| $I_{CC6}$ | Refresh Current:<br>CBR[2,3,5]<br>Average Power Supply Current | $\overline{RAS}$, $\overline{CAS}$ Cycling<br>$t_{RC}$ = $t_{RC}$ (min.) | -35<br>-50<br>-60 | –<br>–<br>– | 110<br>95<br>85 | mA |

**Notes:**

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the $t_{REF}$ refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each Fast page cycle.
5. Enables on-chip refresh and address counters.

## AC CHARACTERISTICS(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter | -35 | | -50 | | -60 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Random READ or WRITE Cycle Time | 60 | – | 90 | – | 110 | – | ns |
| $t_{RAC}$ | Access Time from $\overline{RAS}$(6, 7) | – | 35 | – | 50 | – | 60 | ns |
| $t_{CAC}$ | Access Time from $\overline{CAS}$(6, 8, 15) | – | 10 | – | 14 | – | 15 | ns |
| $t_{AA}$ | Access Time from Column-Address(6) | – | 18 | – | 25 | – | 30 | ns |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 35 | 10K | 50 | 10K | 60 | 10K | ns |
| $t_{RP}$ | $\overline{RAS}$ Precharge Time | 20 | – | 30 | – | 40 | – | ns |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width(23) | 6 | 10K | 8 | 10K | 10 | 10K | ns |
| $t_{CP}$ | $\overline{CAS}$ Precharge Time(9) | 6 | – | 8 | – | 10 | – | ns |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time (21) | 35 | – | 50 | – | 60 | – | ns |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time(10, 20) | 11 | 28 | 19 | 36 | 20 | 45 | ns |
| $t_{ASR}$ | Row-Address Setup Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{RAH}$ | Row-Address Hold Time | 6 | – | 8 | – | 10 | – | ns |
| $t_{ASC}$ | Column-Address Setup Time(20) | 0 | – | 0 | – | 0 | – | ns |
| $t_{CAH}$ | Column-Address Hold Time(20) | 6 | – | 8 | – | 10 | – | ns |
| $t_{AR}$ | Column-Address Hold Time (referenced to $\overline{RAS}$) | 30 | – | 40 | – | 40 | – | ns |
| $t_{RAD}$ | $\overline{RAS}$ to Column-Address Delay Time(11) | 10 | 20 | 14 | 25 | 15 | 30 | ns |
| $t_{RAL}$ | Column-Address to $\overline{RAS}$ Lead Time | 18 | – | 25 | – | 30 | – | ns |
| $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 8 | – | 14 | – | 15 | – | ns |
| $t_{CLZ}$ | $\overline{CAS}$ to Output in Low-Z(15, 24) | 3 | – | 3 | – | 3 | – | ns |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time(21) | 5 | – | 5 | – | 5 | – | ns |
| $t_{OD}$ | Output Disable Time(19, 24) | 3 | 15 | 3 | 15 | 3 | 15 | ns |
| $t_{OE}$ | Output Enable Time(15, 16) | – | 10 | - | 15 | - | 15 | ns |
| $t_{OES}$ | $\overline{OE}$ LOW to $\overline{CAS}$ HIGH Setup Time | 5 | – | 5 | – | 5 | – | ns |
| $t_{RCS}$ | Read Command Setup Time(17, 20) | 0 | – | 0 | – | 0 | – | ns |
| $t_{RRH}$ | Read Command Hold Time (referenced to $\overline{RAS}$)(12) | 0 | – | 0 | – | 0 | – | ns |
| $t_{RCH}$ | Read Command Hold Time (referenced to $\overline{CAS}$)(12, 17, 21) | 0 | – | 0 | – | 0 | – | ns |
| $t_{WCH}$ | Write Command Hold Time(17) | 5 | – | 8 | – | 10 | – | ns |
| $t_{WCR}$ | Write Command Hold Time (referenced to $\overline{RAS}$)(17) | 30 | – | 40 | – | 50 | – | ns |
| $t_{WP}$ | Write Command Pulse Width(17) | 5 | – | 8 | – | 10 | – | ns |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time(17) | 8 | – | 14 | – | 15 | – | ns |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time(17, 21) | 8 | – | 14 | – | 15 | – | ns |
| $t_{WCS}$ | Write Command Setup Time(14, 17, 20) | 0 | – | 0 | – | 0 | – | ns |
| $t_{DHR}$ | Data-in Hold Time (referenced to $\overline{RAS}$) | 30 | – | 40 | – | 45 | – | ns |

## AC CHARACTERISTICS (Continued)[1,2,3,4,5,6]

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter | -35 Min. | -35 Max. | -50 Min. | -50 Max. | -60 Min. | -60 Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{ACH}$ | Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle | 15 | – | 15 | – | 15 | – | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle[18] | 8 | – | 10 | – | 15 | – | ns |
| $t_{DS}$ | Data-In Setup Time[15, 22] | 0 | – | 0 | – | 0 | – | ns |
| $t_{DH}$ | Data-In Hold Time[15, 22] | 6 | – | 8 | – | 10 | – | ns |
| $t_{RWC}$ | READ-MODIFY-WRITE Cycle Time | 80 | – | 125 | – | 140 | – | ns |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle[14] | 45 | – | 70 | – | 80 | – | ns |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay Time[14, 20] | 25 | – | 34 | – | 36 | – | ns |
| $t_{AWD}$ | Column-Address to $\overline{WE}$ Delay Time[14] | 30 | – | 42 | – | 49 | – | ns |
| $t_{PC}$ | Fast Page Mode READ or WRITE Cycle Time | 12 | – | 20 | – | 25 | – | ns |
| $t_{RASP}$ | Fast Page Mode $\overline{RAS}$ Pulse Width | 35 | 100K | 50 | 100K | 60 | 100K | ns |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge[15] | - | 21 | - | 27 | - | 34 | ns |
| $t_{PRWC}$ | Fast Page Mode READ-WRITE Cycle Time | 40 | – | 47 | – | 56 | – | ns |
| $t_{OFF}$ | Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$[13,15,19, 24] | 3 | 15 | 3 | 15 | 3 | 15 | ns |
| $t_{CSR}$ | $\overline{CAS}$ Setup Time (CBR REFRESH)[20, 25] | 8 | – | 10 | – | 10 | – | ns |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time (CBR REFRESH)[21, 25] | 8 | – | 10 | – | 10 | – | ns |
| $t_{ORD}$ | $\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle | 0 | – | 0 | – | 0 | – | ns |
| $t_{REF}$ | Auto Refresh Period 1,024 Cycles | – | 16 | – | 16 | – | 16 | ms |
| $t_T$ | Transition Time (Rise or Fall)[2, 3] | 1 | 15 | 1 | 50 | 1 | 50 | ns |

## AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF (Vcc = 5.0V + 10%)
One TTL Load and 50 pF (Vcc = 3.3V + 10%)

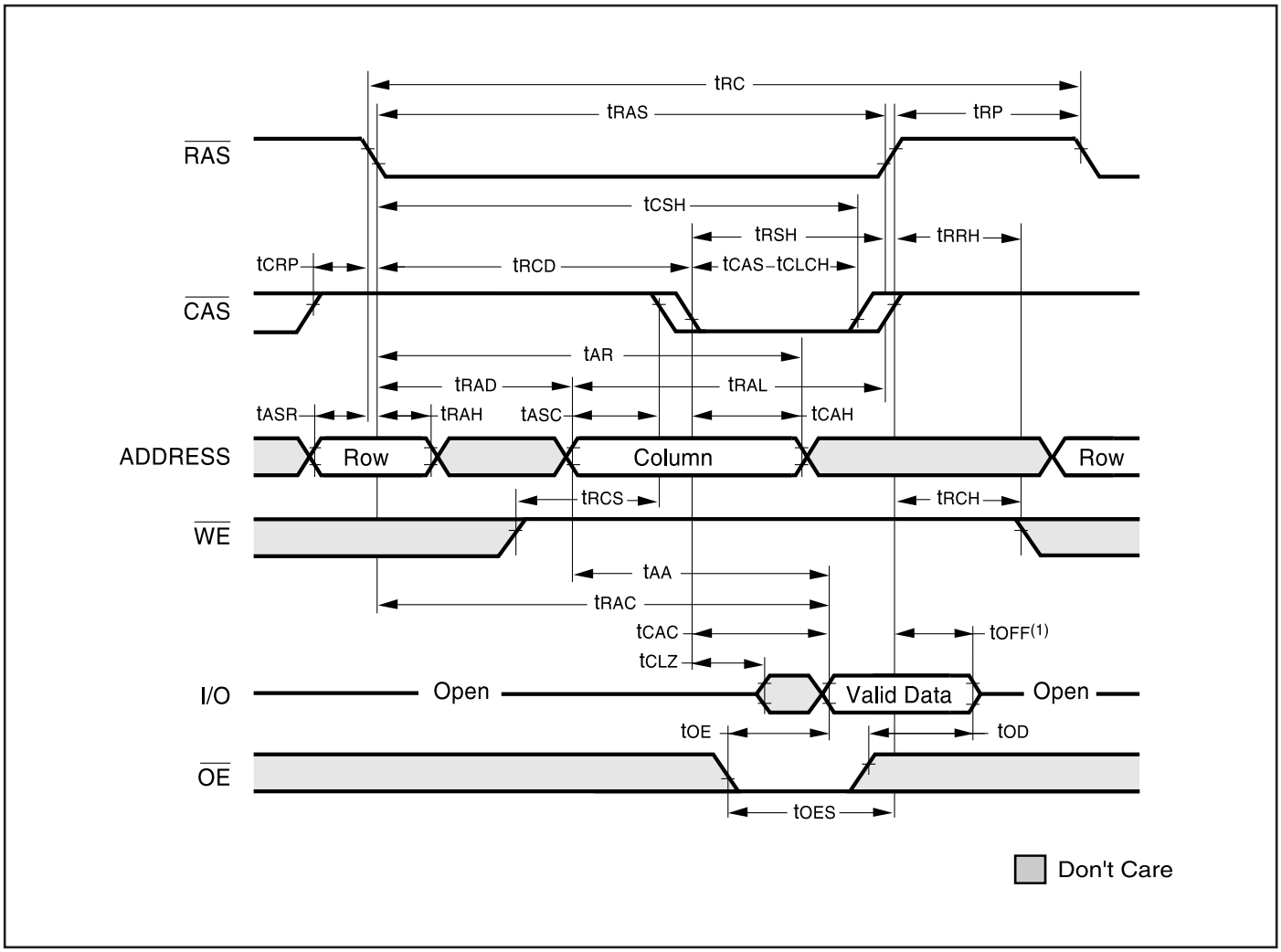
Input timing reference levels: $V_{IH}$ = 2.4V, $V_{IL}$ = 0.8V (Vcc = 5.0V + 10%)
$V_{IH}$ = 2.4V, $V_{IL}$ = 0.8V (Vcc = 3.3V + 10%)

Output timing reference levels: $V_{OH}$ = 2.0V, $V_{OL}$ = 0.8V (Vcc = 5.0V + 10%, 3.3V + 10%)

**Notes:**

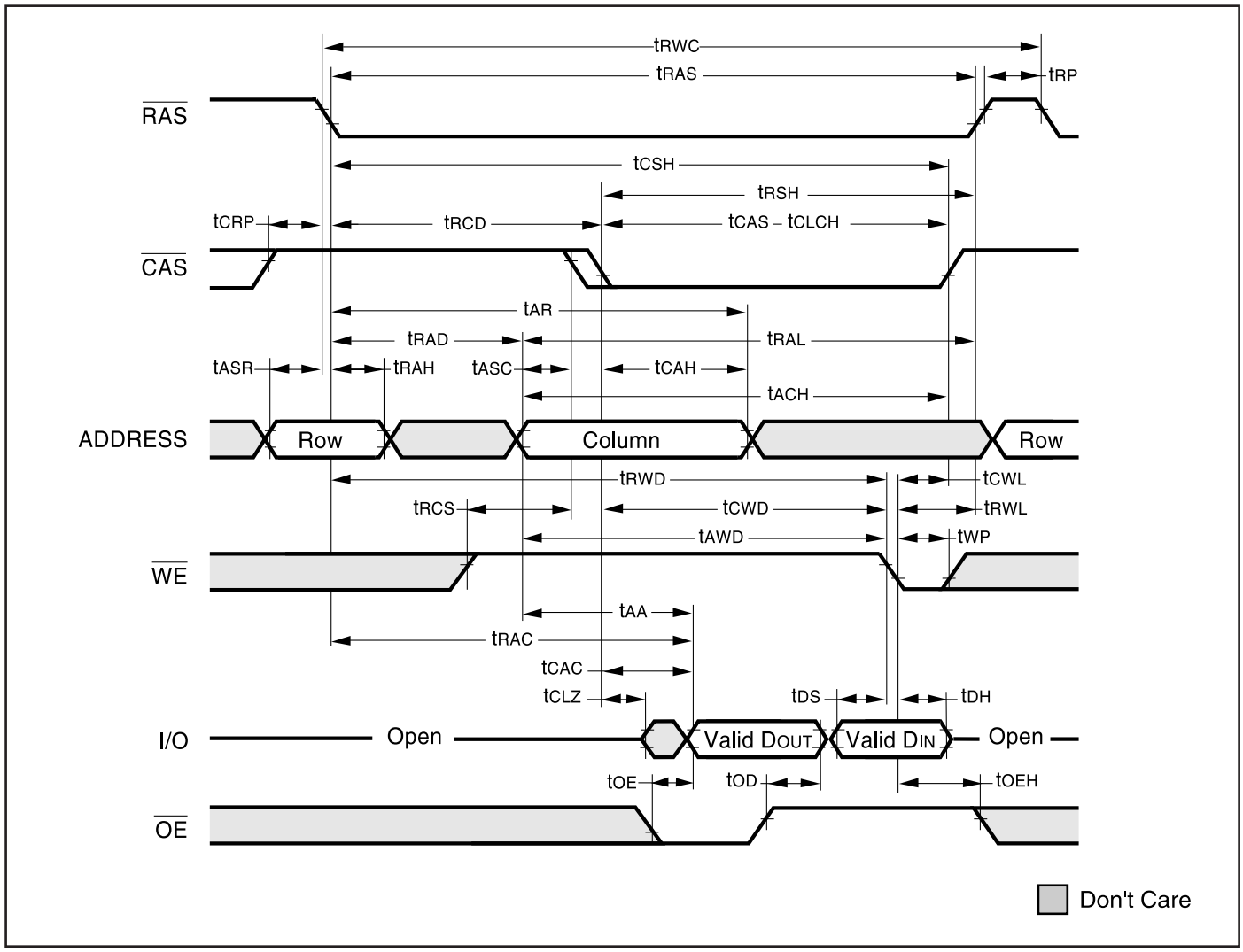
1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the $t_{REF}$ refresh requirement is exceeded.
2. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS}$ = $V_{IH}$, data output is High-Z.
5. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} < t_{RCD}$ (MAX). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.
8. Assumes that $t_{RCD} > t_{RCD}$ (MAX).
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for $t_{CP}$.
10. Operation with the $t_{RCD}$ (MAX) limit ensures that $t_{RAC}$ (MAX) can be met. $t_{RCD}$ (MAX) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (MAX) limit, access time is controlled exclusively by $t_{CAC}$.
11. Operation within the $t_{RAD}$ (MAX) limit ensures that $t_{RCD}$ (MAX) can be met. $t_{RAD}$ (MAX) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (MAX) limit, access time is controlled exclusively by $t_{AA}$.
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a READ cycle.
13. $t_{OFF}$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$.
14. $t_{WCS}$, $t_{RWD}$, $t_{AWD}$ and $t_{CWD}$ are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} > t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWD} > t_{RWD}$ (MIN), $t_{AWD} > t_{AWD}$ (MIN) and $t_{CWD} > t_{CWD}$ (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to $V_{IH}$) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both $t_{OD}$ and $t_{OEH}$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after $t_{OEH}$ is met.
19. The I/Os are in open during READ cycles once $t_{OD}$ or $t_{OFF}$ occur.
20. Determined by falling edge of $\overline{CAS}$.
21. Determined by rising edge of $\overline{CAS}$.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. $\overline{CAS}$ must meet minimum pulse width.
24. The 3 ns minimum is a parameter guaranteed by design.
25. Enables on-chip refresh and address counters.

## READ CYCLE

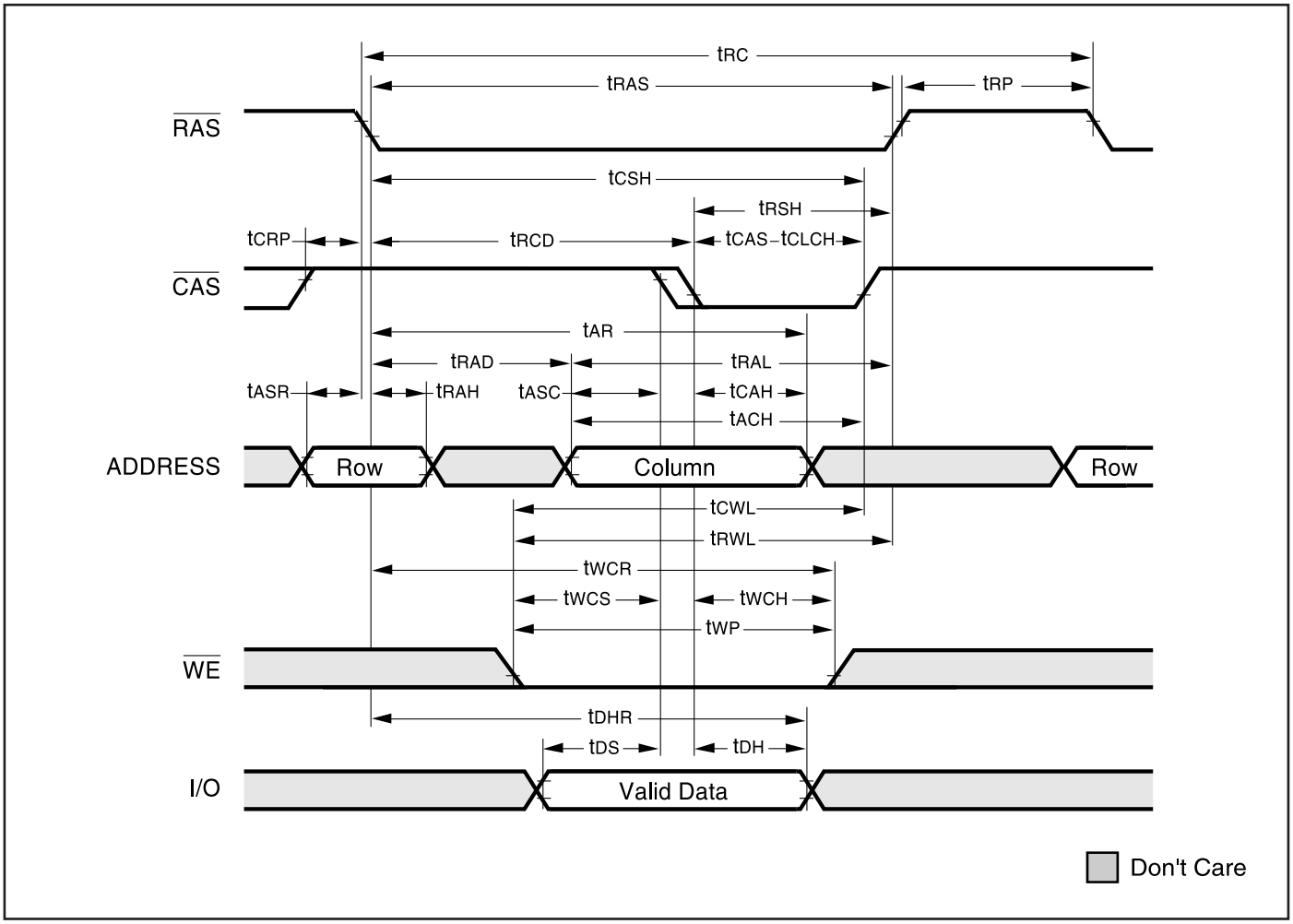



**Note:**
1. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

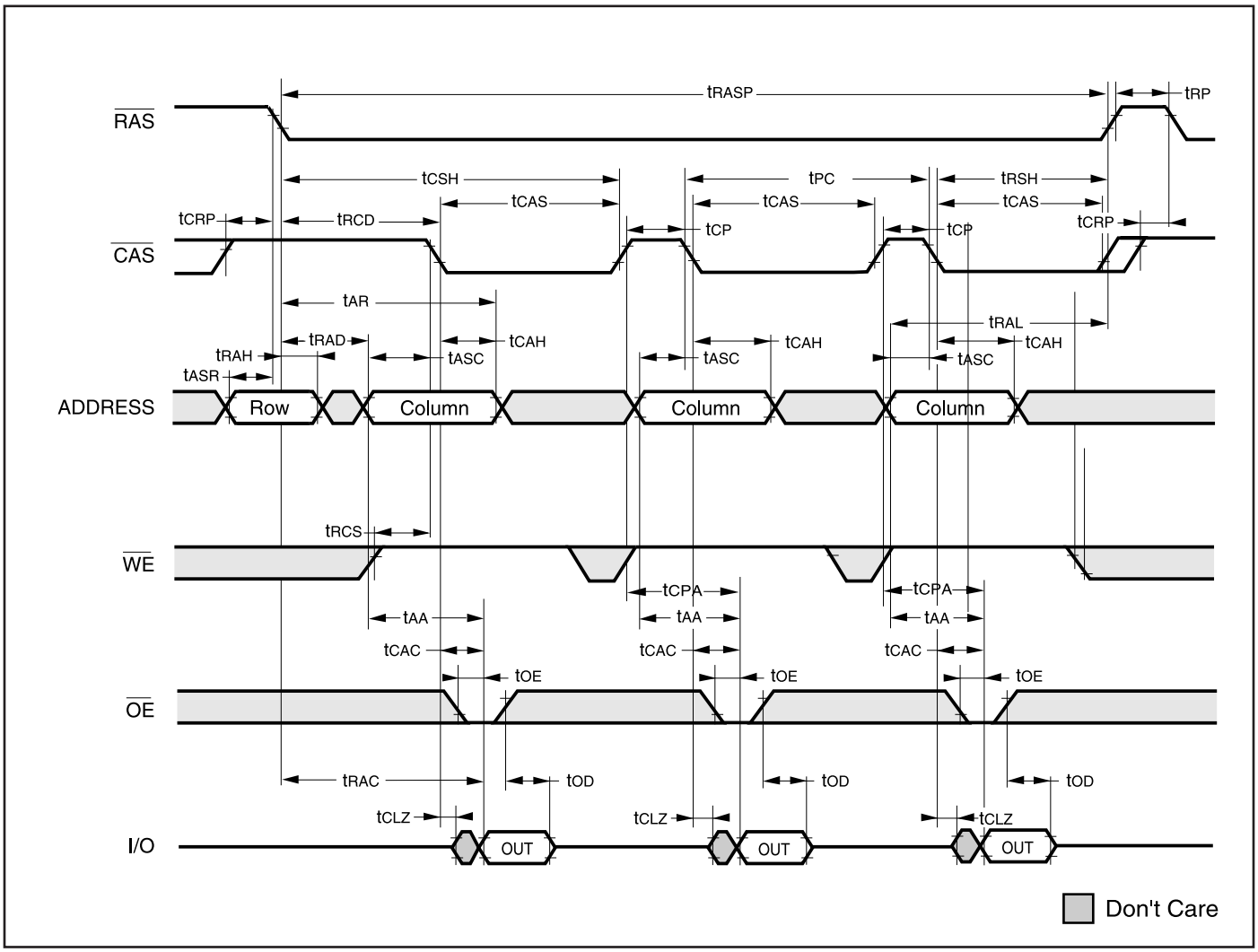
## READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



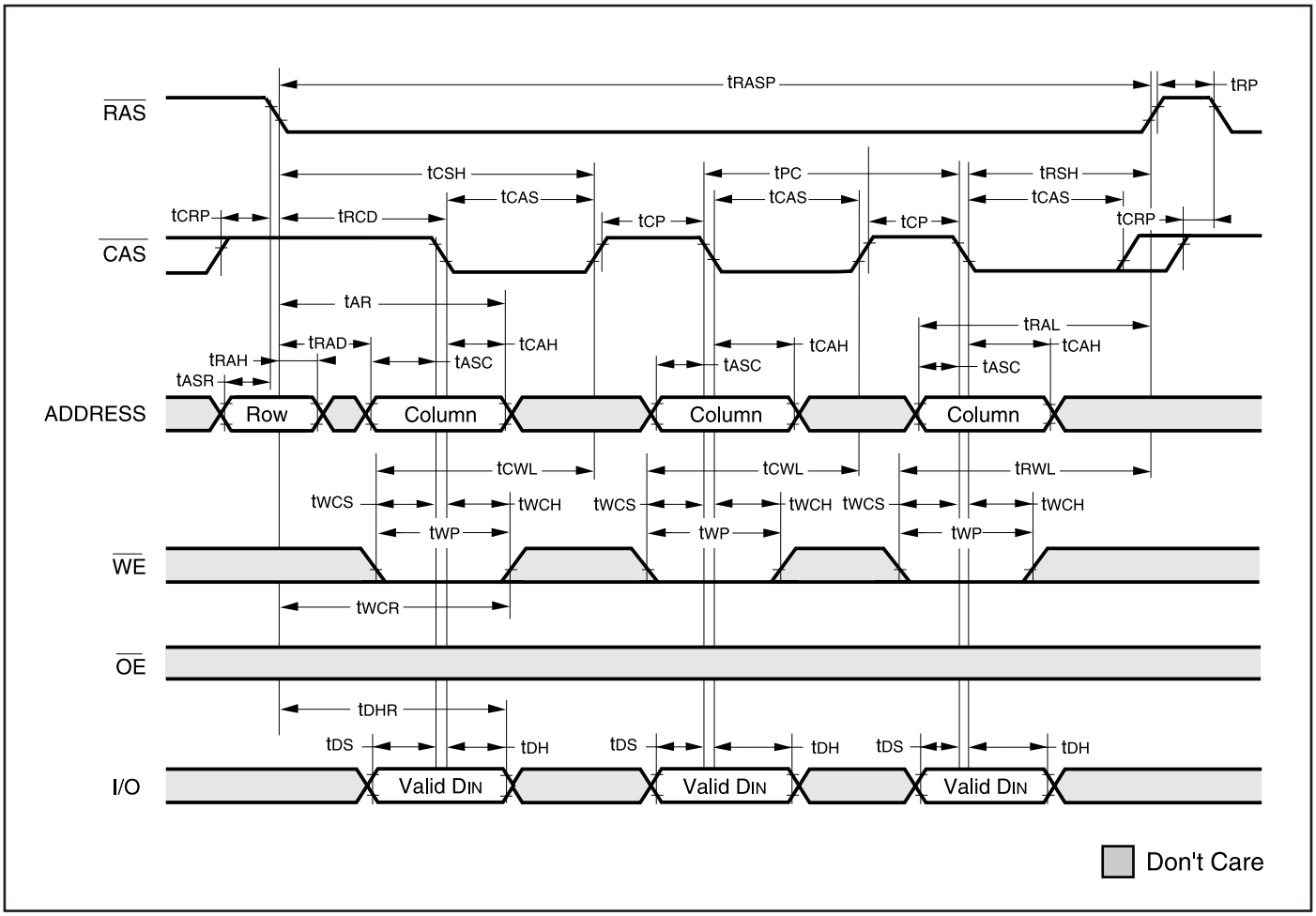
## EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



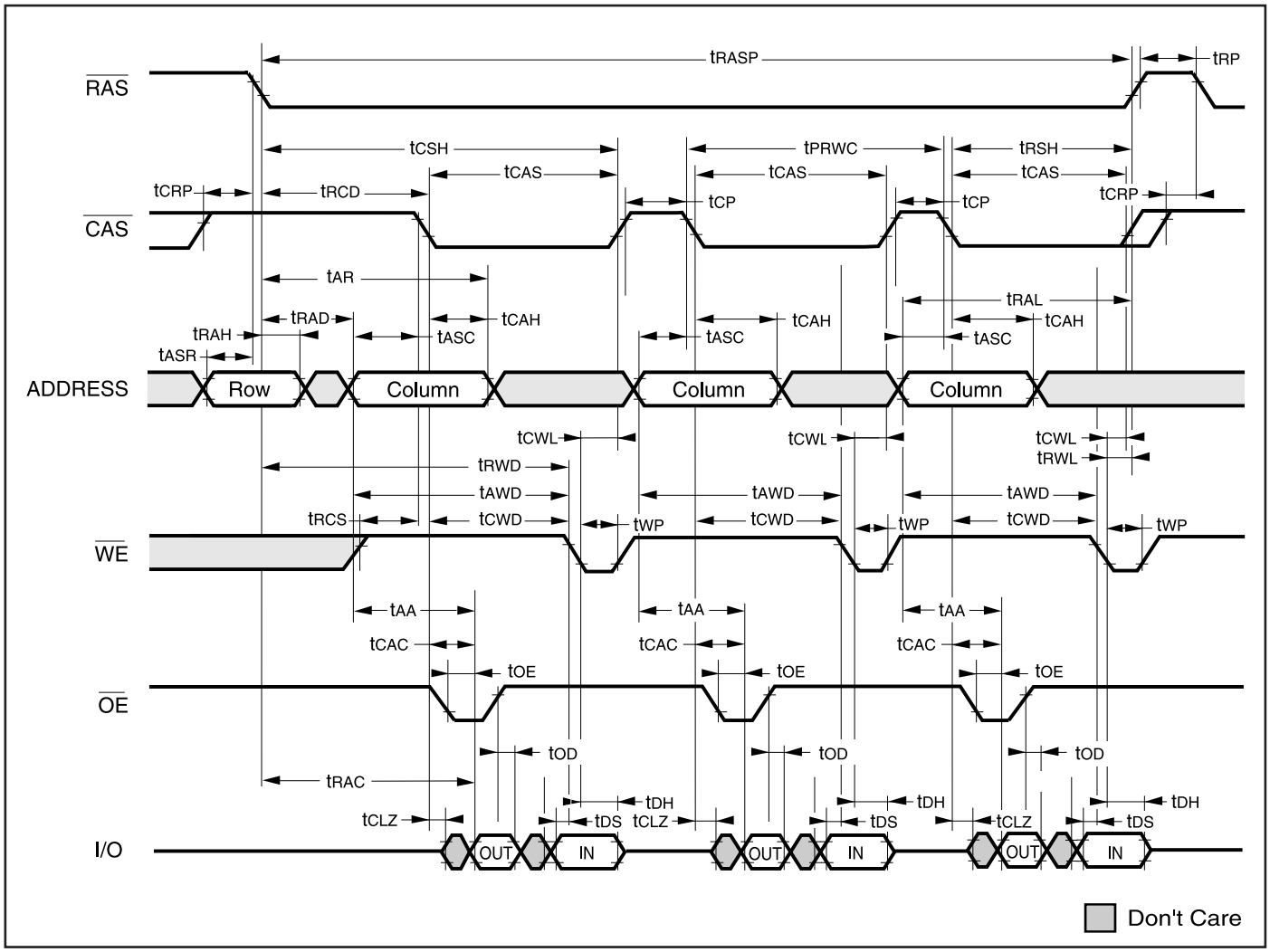
## FAST PAGE MODE READ CYCLE



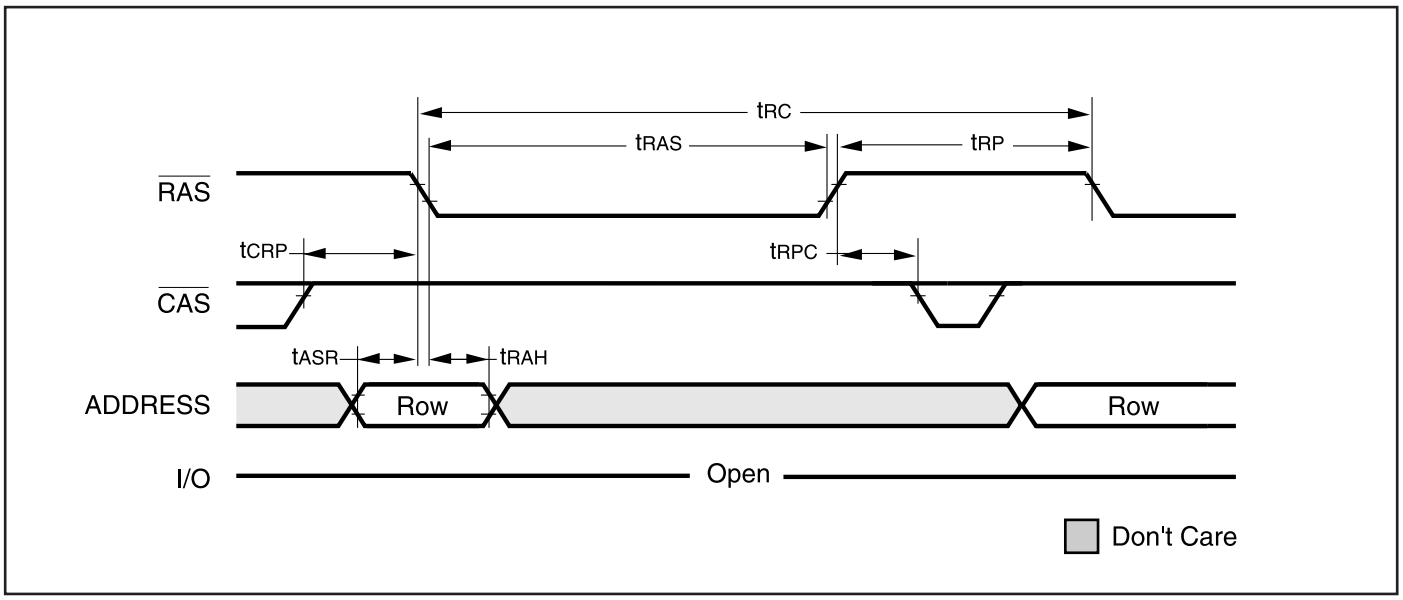
## FAST PAGE MODE EARLY WRITE CYCLE



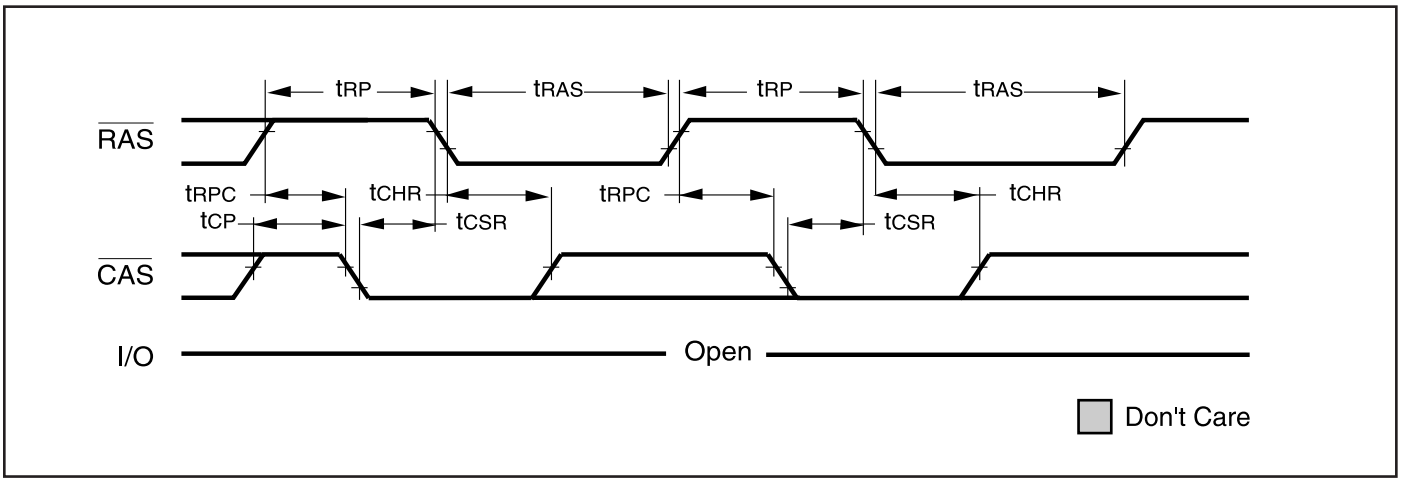
## FAST PAGE MODE READ-MODIFY-WRITE CYCLE



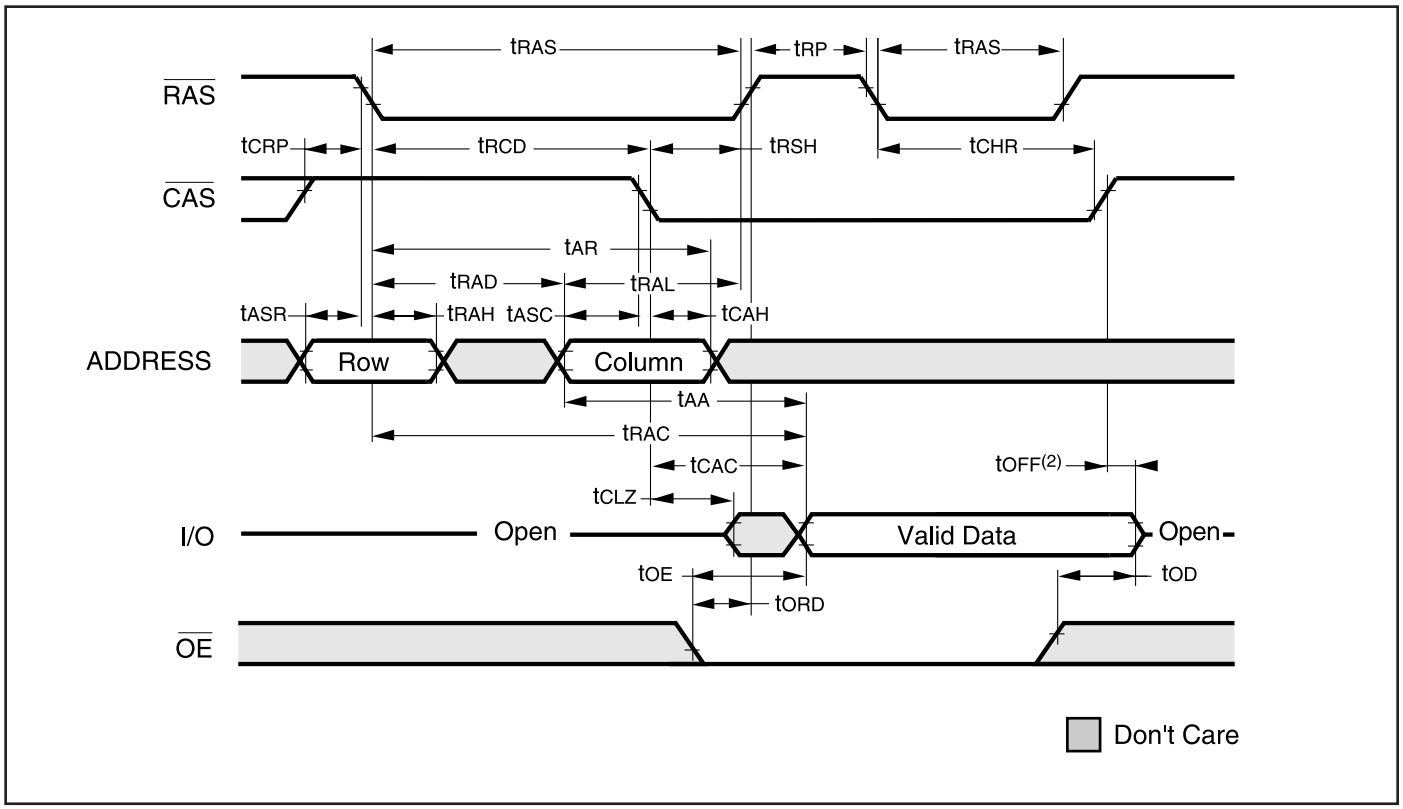

## RAS-ONLY REFRESH CYCLE (OE, WE = DON'T CARE)



## CBR REFRESH CYCLE (Addresses; $\overline{WE}$, $\overline{OE}$ = DON'T CARE)




## HIDDEN REFRESH CYCLE(1) ($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)




**Notes:**
1. A Hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
2. $t_{OFF}$ is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

## ORDERING INFORMATION

### Commercial Range: 0°C to 70°C

### Voltage: 5V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 35 | IC41C4105-35J | 300mil SOJ |
| 35 | IC41C4105-35T | 300mil TSOP-2 |
| 50 | IC41C4105-50J | 300mil SOJ |
| 50 | IC41C4105-50T | 300mil TSOP-2 |
| 60 | IC41C4105-60J | 300-mil SOJ |
| 60 | IC41C4105-60T | 300mil TSOP-2 |

### Voltage: 3.3V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 35 | IC41LV4105-35J | 300mil SOJ |
| 35 | IC41LV4105-35T | 300mil TSOP-2 |
| 50 | IC41LV4105-50J | 300mil SOJ |
| 50 | IC41LV4105-50T | 300mil TSOP-2 |
| 60 | IC41LV4105-60J | 300mil SOJ |
| 60 | IC41LV4105-60T | 300mil TSOP-2 |

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