8Mb (256Kx36 & 512x18) and 4Mb (128Kx36 & 256Kx18) SRAM

Features

- 8Mb: 256K x 36 or 512K x 18 organizations
  4Mb: 128K x 36 or 256K x 18 organizations
- 0.25 Micron CMOS technology
- Synchronous pipeline mode of operation with self-timed late write
- Single differential high-speed transceiver logic (HSTL) Clock
- +3.3V power supply, ground, 2.1V V_{DDQ}, and 1.0V V_{REF}
- HSTL input and output levels
- Registered addresses, write enables, synchronous select, and data-ins
- Registered outputs
- Common I/O
- Asynchronous output enable
- Synchronous power down input
- Boundary scan using limited set of JTAG 1149.1 functions
- Byte write capability and global write enable
- 7 x 17 bump ball grid array package with SRAM JEDEC standard pinout and boundary SCAN order

Description

The 4Mb and 8Mb SRAMs—IBM0436A41DLAB, IBM0418A41DLAB, IBM0418A81DLAB, and IBM0436A81DLAB—are synchronous pipeline mode, high-performance CMOS static random access memories that are versatile, have wide I/O, and can achieve 3ns cycle times. Dual differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K clock, all addresses, write-enables, synchronous select, and data ins are registered internally. Data outs are updated from output registers on the next rising edge of the K clock. An internal write buffer allows write data to follow one cycle after addresses and controls. The SRAM is operated with a single +3.3V power supply and is compatible with HSTL I/O interfaces.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC,SA(8Mb)	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQ19	DQ18	V_{SS}	ZQ	V_{SS}	DQ9	DQb10
E	DQ22	DQ20	V_{SS}	$\overline{SS}$	V_{SS}	DQ11	DQb13
F	V_{DDQ}	DQ21	V_{SS}	$\overline{G}$	V_{SS}	DQ12	V_{DDQ}
G	DQ24	DQ23	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQ14	DQb15
H	DQ25	DQ26	V_{SS}	NC	V_{SS}	DQ17	DQb16
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ34	DQ35	V_{SS}	K	V_{SS}	DQ8	DQ7
L	DQ33	DQ32	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ5	DQ6
M	V_{DDQ}	DQ30	V_{SS}	$\overline{SW}$	V_{SS}	DQ3	V_{DDQ}
N	DQ31	DQ29	V_{SS}	SA0	V_{SS}	DQ2	DQ4
P	DQ28	DQ27	V_{SS}	SA1	V_{SS}	DQ0	DQ1
R	NC	SA	M1[1]	V_{DD}	M2[1]	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

1. M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD}, respectively.

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC,SA(8Mb)	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQ14	NC	V_{SS}	ZQ	V_{SS}	DQ0	NC
E	NC	DQ15	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ1
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ2	V_{DDQ}
G	NC	DQ16	$\overline{SBWb}$	NC	NC	NC	DQ3
H	DQ17	NC	V_{SS}	NC	V_{SS}	DQ4	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ8
L	DQ12	NC	NC	$\overline{K}$	$\overline{SBWa}$	DQ7	NC
M	V_{DDQ}	DQ10	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ11	NC	V_{SS}	SA0	V_{SS}	DQ6	NC
P	NC	DQ9	V_{SS}	SA1	V_{SS}	NC	DQ5
R	NC	SA	M1[1]	V_{DD}	M2[1]	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

1. M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD} respectively.

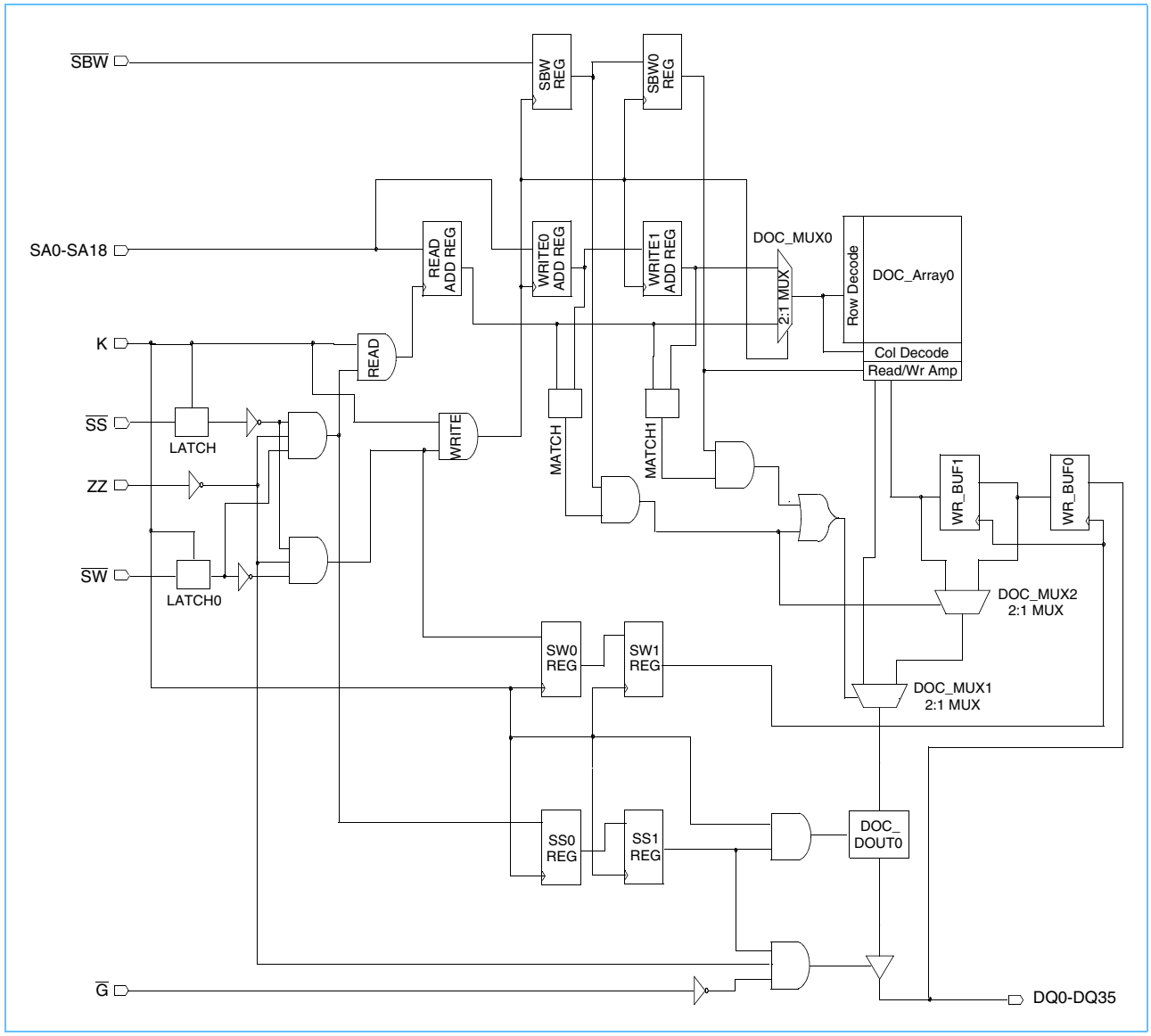
Pin Description

SA0-SA18	Address Input SA0-SA18 for 512K x 18 SA0-SA17 for 256K x 36 SA0-SA17 for 256K x 18 SA0-SA16 for 128K x 36	$\overline{G}$	Asynchronous Output Enable
DQ0-DQ35	Data I/O DQ0-DQ17 for 512K x 18 DQ0-DQ35 for 256K x 36	$\overline{SS}$	Synchronous Select
K, $\overline{K}$	Differential Input Register Clocks	M1, M2	Clock Mode Inputs - Selects Single or Dual Clock Operation.
$\overline{SW}$	Write Enable, Global	V_{REF}(2)	HSTL Input Reference Voltage
$\overline{SBWa}$	Write Enable, Byte a (DQ0-DQ8)	V_{DD}	Power Supply (+3.3V)
$\overline{SBWb}$	Write Enable, Byte b (DQ9-DQ17)	V_{SS}	Ground
$\overline{SBWc}$	Write Enable, Byte c (DQ18-DQ26)	V_{DDQ}	Output Power Supply
$\overline{SBWd}$	Write Enable, Byte d (DQ27-DQ35)	ZZ	Synchronous Sleep Mode
TMS,TDI,TCK	IEEE® 1149.1 Test Inputs (LVTTL levels)	ZQ	Output Driver Impedance Control
TDO	IEEE 1149.1 Test Output (LVTTL level)	NC	No Connect

Ordering Information (All possible types are listed; some may not be qualified.)

Part Number	Organization	Speed	Leads
IBM0418A41DLAB - 3	256K x 18	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0418A41DLAB - 3F	256K x 18	1.8ns Access / 3.3ns Cycle	7 x 17 BGA
IBM0418A41DLAB - 4	256K x 18	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0418A41DLAB - 5	256K x 18	2.25ns Access /5.0ns Cycle	7 x 17 BGA
IBM0436A41DLAB - 3	128K x 36	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0436A41DLAB - 3F	128K x 36	2.0ns Access / 3.3ns Cycle	7 x 17 BGA
IBM0436A41DLAB - 4	128K x 36	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0436A41DLAB - 5	128K x 36	2.25ns Access /5.0ns Cycle	7 x 17 BGA
IBM0418A81DLAB - 3	512K x 18	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0418A81DLAB - 3F	512K x 18	1.8ns Access / 3.3ns Cycle	7 x 17 BGA
IBM0418A81DLAB - 4	512K x 18	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0418A81DLAB - 5	512K x 18	2.25ns Access /5.0ns Cycle	7 x 17 BGA
IBM0436A81DLAB - 3	256K x 36	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0436A81DLAB -3F	256K x 36	1.8ns Access / 3.3ns Cycle	7 x 17 BGA
IBM0436A81DLAB - 4	256K x 36	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0436A81DLAB - 5	256K x 36	2.25ns Access /5.0ns Cycle	7 x 17 BGA

Block Diagram



SRAM Features

Late Write

The late write function allows write data to be registered one cycle after addresses and controls. This feature eliminates one bus-turnaround cycle, necessary when going from a read to a write operation. Late write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. When a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte-by-byte basis. When only one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

Mode Control

Mode control pins M1 and M2 are used to select four different JEDEC-standard read protocols. This SRAM supports a single clock pipeline (M1 = V_{SS}, M2 = V_{DD}). This datasheet only describes single clock pipeline functionality. Mode control inputs must be set at power up and must not change during SRAM operation. This SRAM is tested only in the pipeline mode.

Sleep Mode

Sleep mode is enabled by switching synchronous signal ZZ high. When the SRAM is in sleep mode, the outputs will go to a High-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω, with the tolerance described in Programmable Impedance Output Driver DC Electrical Characteristics on page 9. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The total external capacitance (including wiring) seen by the ZQ ball should be minimized (less than 7.5 pF).

Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation may move the output driver impedance level only one step at a time towards the optimum level. The output driver has 32 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and deselect operations will synchronously switch the SRAM into and out of High-Z, thereby triggering an update. The user may choose to invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold times around the K clock to guarantee the proper update. There are no power-up requirements for the SRAM; however, to guarantee optimum output driver impedance after power up, the SRAM needs 4096 clock cycles followed by a Low-Z to High-Z transition.

Power-Up and Power-Down Sequencing

The power supplies need to be powered up in the following order: V_{DD}, V_{DDQ}, V_{REF}, and inputs. The power-down sequencing must be in the reverse order. V_{DDQ} can be allowed to exceed V_{DD} by no more than 0.6V.

Clock Truth Table

K	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWa}$	$\overline{SBWb}$	$\overline{SBWc}$	$\overline{SBWd}$	DQ (n)	DQ (n+1)	Mode
L→H	L	L	H	X	X	X	X	X	D_{OUT} 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	D_{IN} 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	D_{IN} 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	D_{IN} 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	D_{IN} 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	D_{IN} 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Output Enable Truth Table

Operation (n, n+1)	$\overline{G}$ (n)	DQ (n)	DQ (n+1)
Read	L	D_{OUT} 0-35	D_{OUT} 0-35
Read	H	High-Z	High-Z
Sleep (ZZ = H)	X	High-Z	High-Z
Write ($\overline{SW}$ = L)	X	X	High-Z
Deselect ($\overline{SS}$ = H)	X	X	High-Z

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.3	V	1
Output Power Supply Voltage	V_{DDQ}	-0.5 to 2.825	V	1
Input Voltage	V_{IN}	-0.5 to 4.3	V	1, 2
DQ Input Voltage	V_{DQIN}	-0.5 to 2.825	V	1
Operating Temperature	T_A	0 to 85	°C	1
Junction Temperature	T_J	110	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Excludes DQ inputs.

Recommended DC Operating Conditions (T_A = 0 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.3 - 5%	3.3	3.3 + 5%	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.8	2.1	V	1
Input High Voltage	V_{IH}	V_{REF} +0.1	—	V_{DDQ} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	V_{REF} - 0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.90	1.0	V	1, 6
Clocks Signal Voltage	$V_{IN - CLK}$	-0.3	—	V_{DDQ} + 0.3	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF - CLK}$	0.1	—	V_{DDQ} + 0.6	V	1, 5
Clocks Common Mode Voltage	$V_{CM - CLK}$	0.55	—	1.0	V	1

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3 V, V_{IH}(Max)AC = V_{DDQ} + 0.85 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = -0.3 V, V_{IL}(Min)AC = -1.5 V (pulse width ≤ 4.0ns).
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (K, $\overline{K}$).
5. $V_{DIF-CLK}$ specifies the minimum clock differential voltage required for switching.
6. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - **x36** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD3} I_{DD3F} I_{DD4} I_{DD5}	— —	0.470 0.450 0.420 0.370	A	1, 3
Average Power Supply Operating Current - **x18** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD3} I_{DD3F} I_{DD4} I_{DD5}	— —	0.450 0.430 0.400 0.350	A	1, 3
Power Supply Standby Current ($\overline{SS}$ = V_{IH}, ZZ = V_{IL}. All other inputs = V_{IH} or V_{IH}, I_{IH} = 0)	I_{SBSS}	—	120	mA	1
Power Supply Sleep Current (ZZ = V_{IH}, All other inputs = V_{IH} or V_{IL}, I_{OUT} = 0)	I_{SBZZ}	—	65	mA	1, 5
Input Leakage Current, any input (except JTAG) (V_{IN} = V_{SS} or V_{DD})	I_{LI}	-2	+2	µA	
Output Leakage Current (V_{OUT} = V_{SS} or V_{DD}, DQ in High-Z)	I_{LO}	-5	+5	µA	
Output “High” Level Voltage (I_{OH} = -8mA)	V_{OH}	V_{DDQ} -.4	V_{DDQ}	V	2, 4
Output “Low” Level Voltage (I_{OL} = +8mA)	V_{OL}	V_{SS}	V_{SS}+.4	V	2, 4
JTAG Leakage Current (V_{IN} = V_{SS} or V_{DD})	I_{LIJTAG}	-50	+10	µA	6

1. I_{OUT} = Chip Output Current.
2. Minimum Impedance Output Driver.
3. The numeric suffix indicates part operating at speed indicated in AC Characteristics on page 11 (that is, I_{DD3} indicates 3ns cycle time).
4. JEDEC Standard JESD8-6 Class 1 Compatible.
5. When ZZ = high, specification is guaranteed at 75°C junction temperature.
6. For JTAG inputs only.

PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	RΘJC	1	°C/W

Capacitance (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%, f = 1MHz)

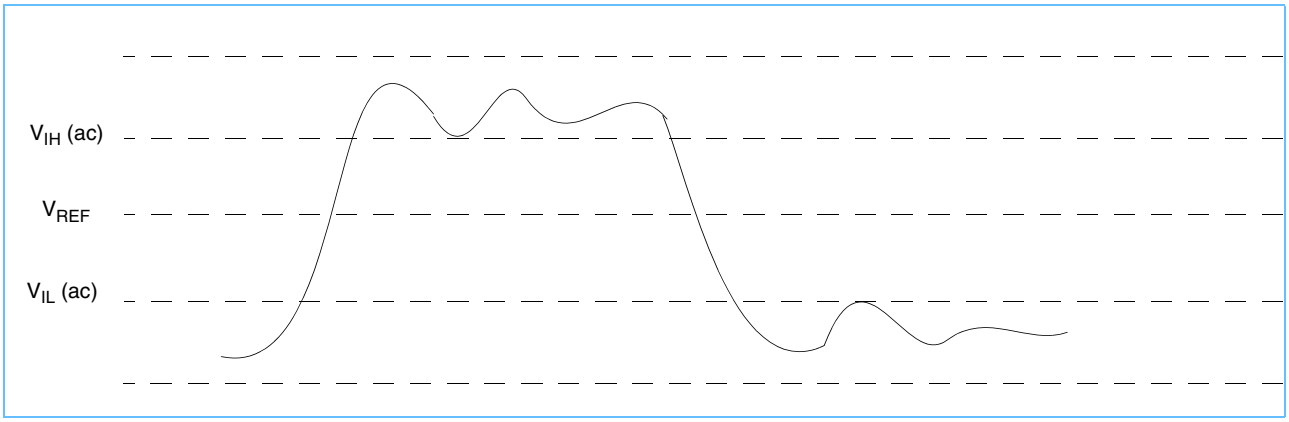
Parameter	Symbol	Test Condition	Max.	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	4	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	4	pF

AC Input Characteristics

Item	Symbol	Min.	Max.	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 04V		3
AC Input Logic Low	V_{IL} (ac)		V_{REF} - 0.4V	3
Clock Input Differential Voltage	V_{DIF} (ac)	0.7V		2
V_{REF} peak-to-peak ac Voltage	V_{REF} (ac)		5% V_{REF} (dc)	1

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the AC Input Definition figure below.

AC Input Definition



Programmable Impedance Output Driver DC Electrical Characteristics

(T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%, V_{DDQ} = 1.5V)

Parameter	Symbol	Min.	Max.	Units	Notes
Output “High” Level Voltage	V_{OH}	V_{DDQ} / 2	V_{DDQ}	V	1, 3
Output “Low” Level Voltage	V_{OL}	V_{SS}	V_{DDQ} / 2	V	2, 3

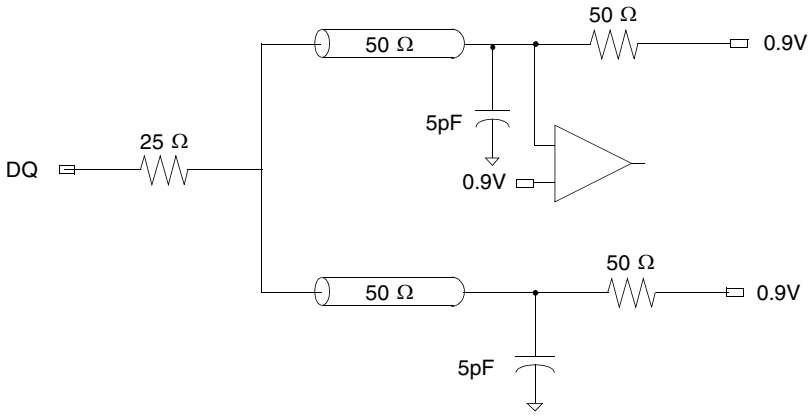
1. For $175\Omega \le RQ \le 350\Omega$, $I_{OH} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5} + 5\right)$ ± 15% @ $V_{OH} = V_{DDQ} / 2$.
2. For $175\Omega \le RQ \le 350\Omega$, $I_{OL} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right)$ ± 15% @ $V_{OL} = V_{DDQ} / 2$.
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5V.

AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%, V_{DDQ} = 1.8V)

Parameter	Symbol	Conditions	Units	Notes
Output Driver Supply Voltage	V_{DDQ}	1.8		
Input High Level	V_{IH}	1.5	V	
Input Low Level	V_{IL}	0.3	V	
Input Reference Voltage	V_{REF}	0.90	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.75	V	
Clocks Common Mode Voltage	V_{CM-CLK}	0.9	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level (except K, C Clocks)		0.9	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1, 2

1. See the AC Test Loading figure below.
2. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.8V.

AC Test Loading

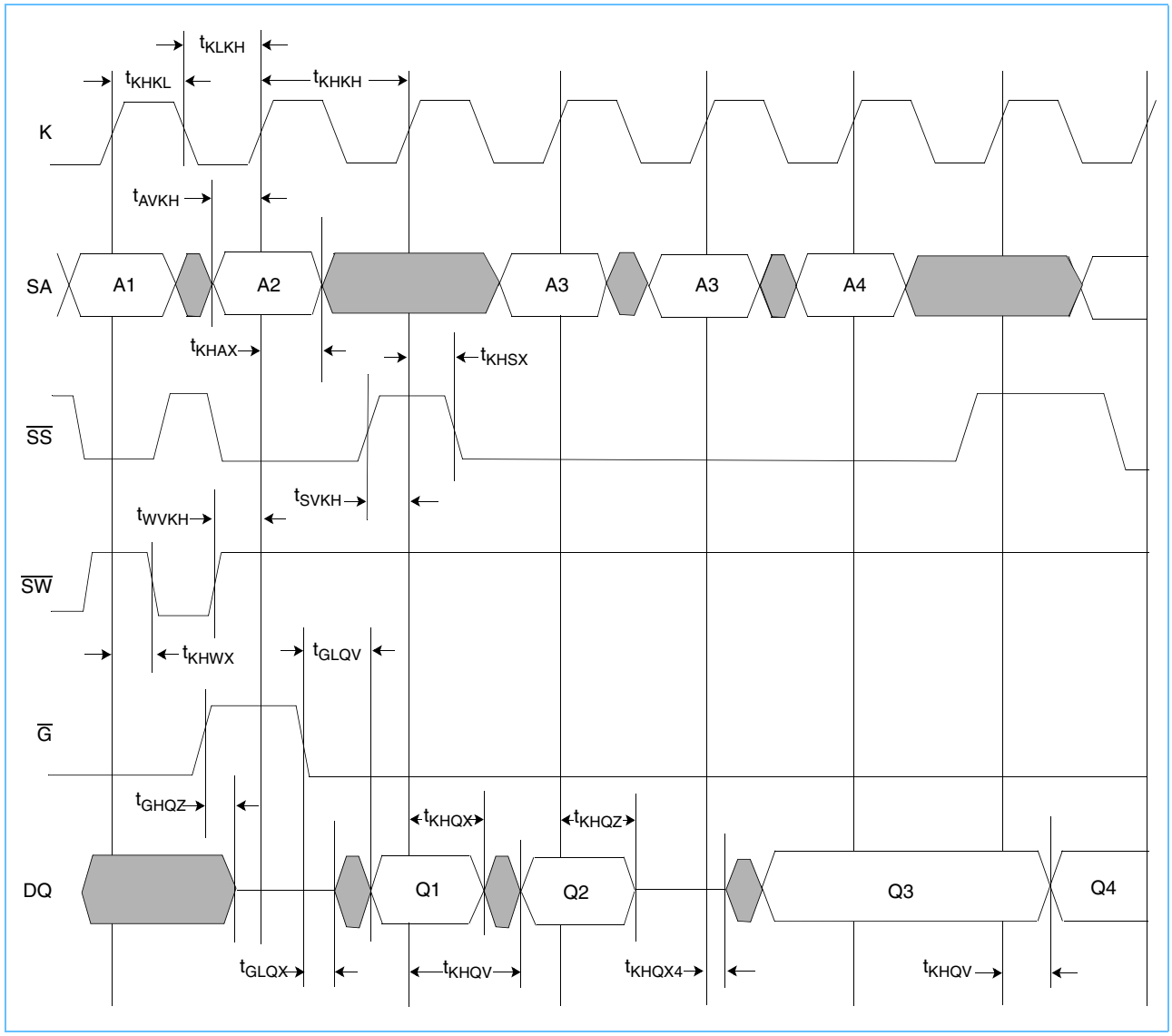


AC Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%)

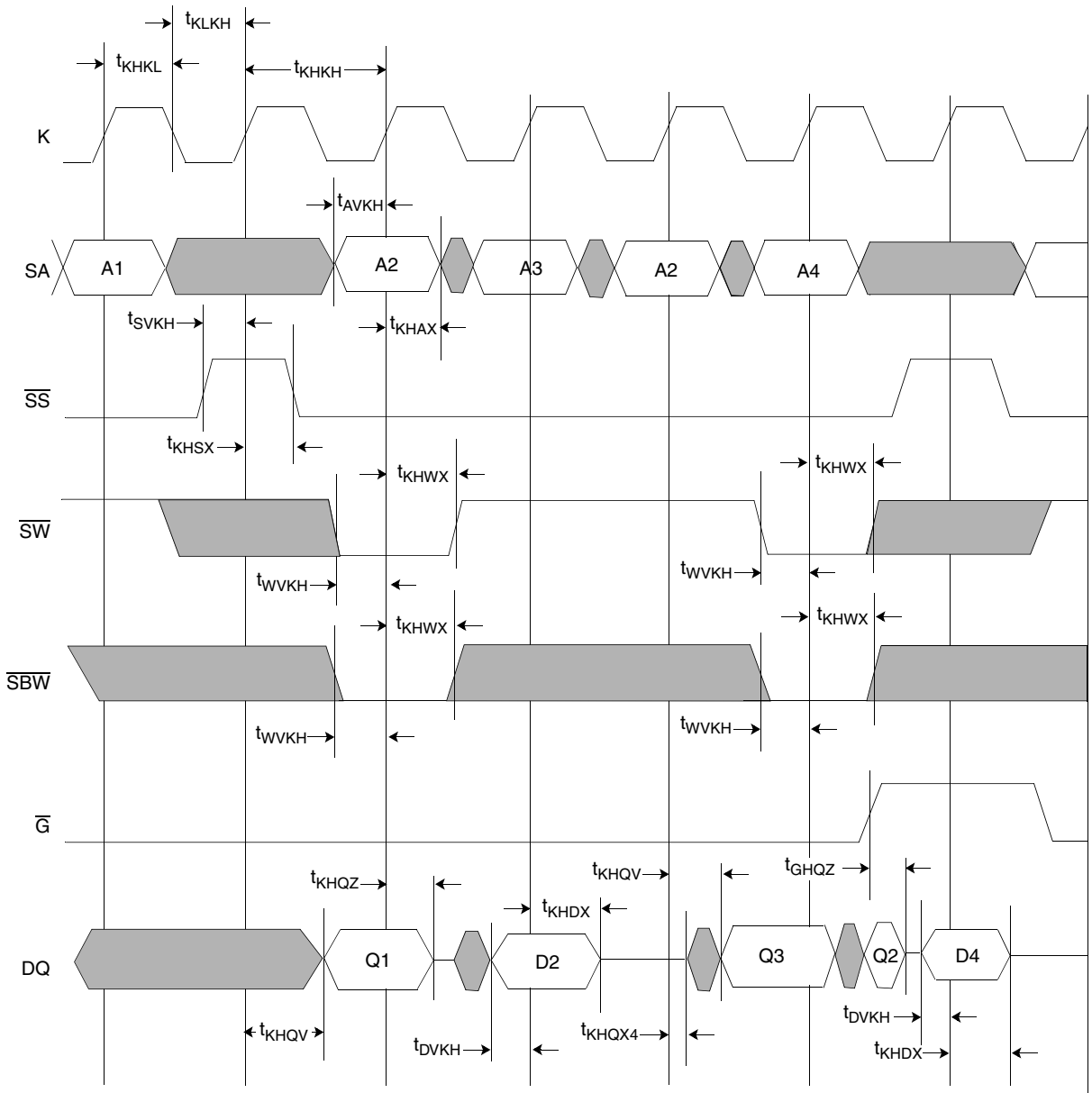
Parameter	Symbol	3		3F		4		5		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	3.0	—	3.3	—	4.0	—	5.0	—	ns	
Clock High Pulse Width	t_{KHKL}	1.2	—	1.5	—	1.5	—	1.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	1.2	—	1.5	—	1.5	—	1.5	—	ns	
Clock to Output Valid	t_{KHQV}	—	1.7	—	1.8	—	2.0	—	2.25	ns	1
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3
Address Hold Time	t_{KHAX}	0.5	—	0.5	—	0.5	—	1.0	—	ns	3
Sync Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3
Sync Select Hold Time	t_{KHSX}	0.5	—	0.5	—	0.5	—	1.0	—	ns	3
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3
Write Enables Hold Time	t_{KHWX}	0.5	—	0.5	—	0.5	—	1.0	—	ns	3
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	3
Data In Hold Time	t_{KHDX}	0.5	—	0.5	—	0.5	—	1.0	—	ns	3
Data Out Hold Time	t_{KHQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output High-Z	t_{KHQZ}	—	2.25	—	2.25	—	2.25	—	2.5	ns	1
Clock High to Output Active	t_{KHQX4}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable to High-Z	t_{GHQZ}	—	2.0		2.0		2.0	—	2.5	ns	1
Output Enable to Low-Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable to Output Valid	t_{GLQV}	—	2.0	—	2.0	—	2.0	—	2.5	ns	1
Output Enable Setup Time	t_{GHKH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable Hold TIme	t_{KHGX}	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 2
Sleep Mode Setup Time	t_{ZVKH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Sleep Mode Hold Time	t_{KHZX}	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Sleep Mode Recovery TIme	t_{ZZR}	200	—	200	—	200	—	200	—	ns	4
Sleep Mode Enable TIme	t_{ZZE}	—	6	—	6.6	—	8	—	10	ns	

1. See the AC Test Loading figure on page 10.
2. Output driver impedance update specifications for $\overline{G}$ induced updates. Write and deselect cycles will also induce output driver updates during High-Z.
3. During normal operation, V_{IH}, V_{IL}, T_{RISE}, and T_{FALL} of inputs must be within 20% of V_{IH}, V_{IL}, T_{RISE}, and T_{FALL} of clock.
4. For t_{ZZR} < 200ns, access time will be equal to twice t_{KHQV}.

Read and Deselect Cycles Timing Diagram

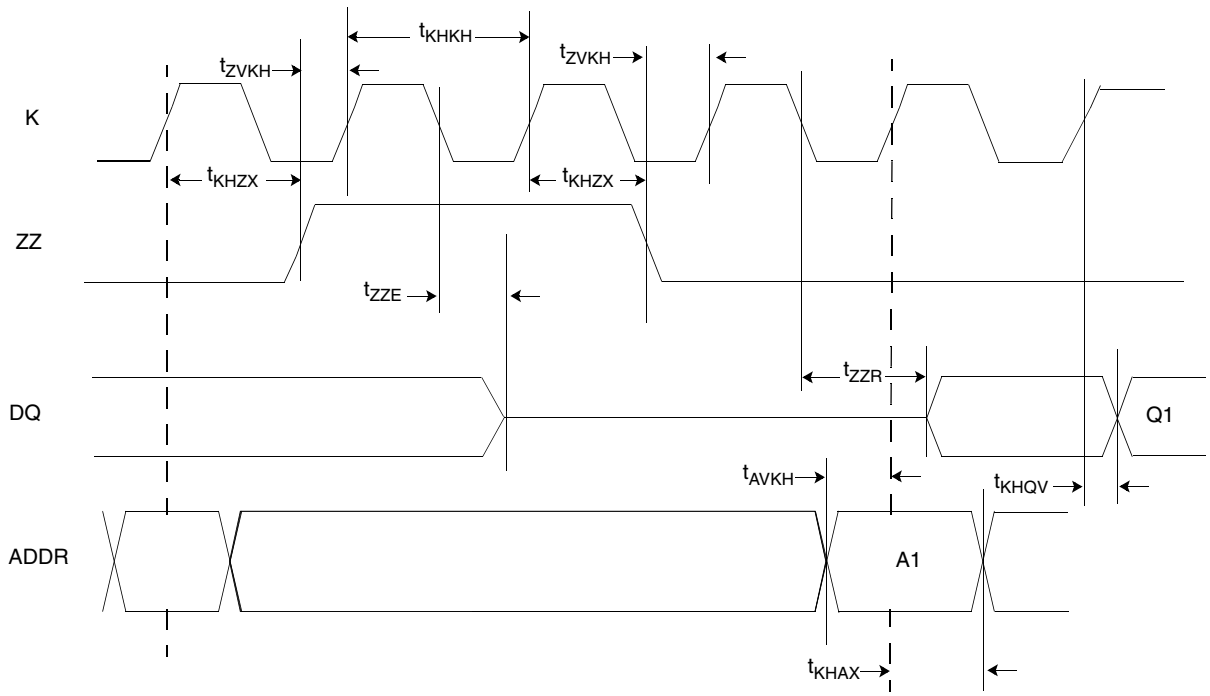


Read Write Cycles Timing Diagram



Notes:
1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Synchronous Sleep Mode Timing Diagram



Note: For t_{ZZR} < 200ns, access time will be equal to 2 x t_{KHQV}.

IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit-board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG DC Operating Characteristics (T_A = 0 to +85°C)

Operates with JEDEC Standard JESD8A (3.3V) logic signal levels

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	—	V_{DD} + 0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	—	—	V	1, 2
JTAG Output Low Level	V_{OL1}	—	—	0.4	V	1, 3

1. All JTAG inputs and outputs are LVTTL compatible only.
2. $I_{OH1} \geq$ -I8mAI.
3. $I_{OL1} \geq$ +I8mAI.

JTAG AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH1}	3.0	V	
Input Pulse Low Level	V_{IL1}	0.0	V	
Input Rise Time	T_{R1}	2.0	ns	
Input Fall Time	T_{F1}	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

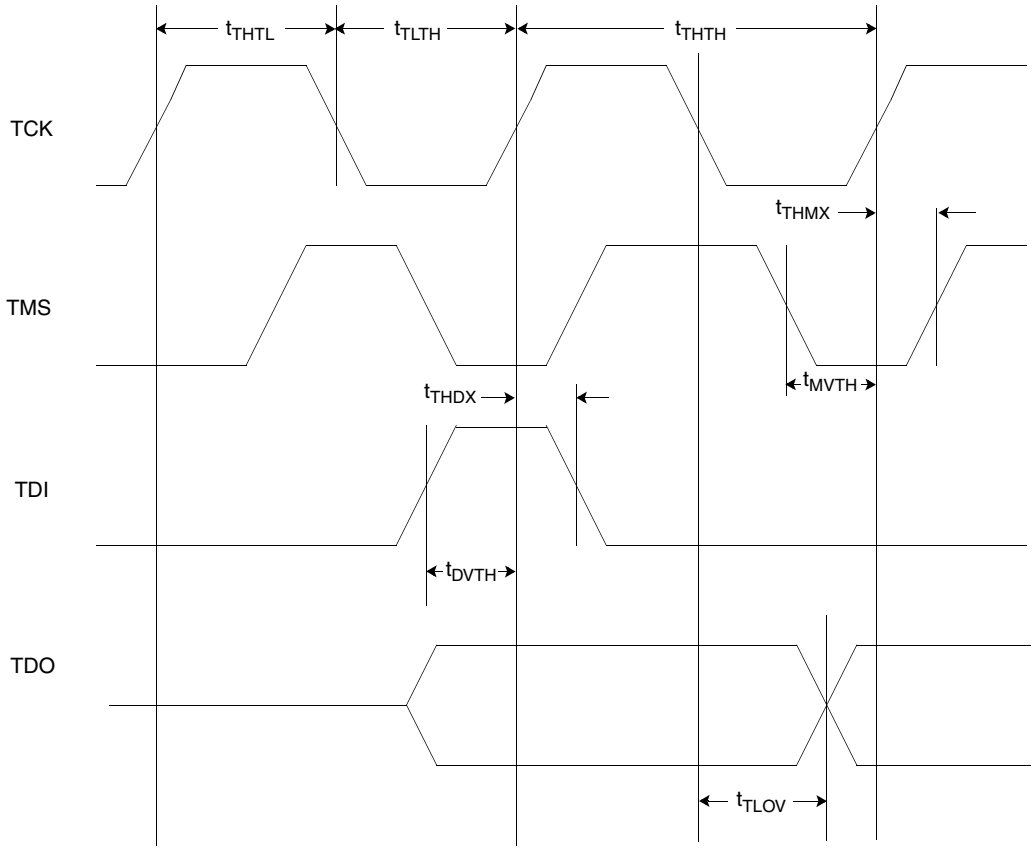
1. See the AC Test Loading figure on page 10.

JTAG AC Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +5%)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{THTL}	7	—	ns	
TCK Low Pulse Width	t_{TLTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See the AC Test Loading figure on page 10.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan[1, 2]	51	70

1. The boundary scan chain consists of the following bits:
   - 36 or 18 bits for data inputs, depending on x18 or x36 configuration
   - 18 bits for SA0 - SA14 in x36, 19 bits for SA0 - SA15 in x18
   - 4 bits for $\overline{\text{SBWa}}$ - $\overline{\text{SBWd}}$ in x36, 2 bits for $\overline{\text{SBWa}}$ and $\overline{\text{SBWb}}$ in x18
   - 9 bits for K, $\overline{\text{K}}$, ZQ, $\overline{\text{SS}}$, $\overline{\text{G}}$, $\overline{\text{SW}}$, ZZ, M1 and M2
   - 3 bits for place holders for 8 Mb, 4 bits for place holders for 4Mb
2. K and $\overline{\text{K}}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for boundary scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacturer JEDEC Code (11:1)	Start Bit(0)
128K x 36	xxxx	011 010 1100	xxxxxx	000 101 001 00	1
256K x 18	xxxx	011 100 1011	xxxxxx	000 101 001 00	1
512K x 18	xxxx	101 111 0011	xxxxxx	000 101 001 00	1
256K x 36	xxxx	101 101 0100	xxxxxx	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1, 2
001	IDCODE	
010	SAMPLE-Z	1, 2
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. The BYPASS register is initiated to V_{SS} when the BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. The SAMPLE instruction does not place DQs in High-Z.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

This part is not designed to comply with the following sections of IEEE 1149.1:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

Boundary Scan Order (128K x 36), (256K x 36) (PH = Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ12	6F	49	DQ26	2H
2	SA	4P	26	DQ13	7E	50	DQ25	1H
3	SA	4T	27	DQ11	6E	51	$\overline{\text{SBW}}$c	3G
4	SA	6R	28	DQ10	7D	52	ZQ	4D
5	SA	5T	29	DQ9	6D	53	$\overline{\text{SS}}$	4E
6	ZZ	7T	30	SA	6A	54	PH[1]	4G
7	DQ0	6P	31	SA	6C	55	PH[2]	4H
8	DQ1	7P	32	SA	5C	56	$\overline{\text{SW}}$	4M
9	DQ2	6N	33	SA	5A	57	$\overline{\text{SBW}}$d	3L
10	DQ4	7N	34	PH[1](4Mb), SA(8Mb)	6B	58	DQ34	1K
11	DQ3	6M	35	SA	5B	59	DQ35	2K
12	DQ5	6L	36	SA	3B	60	DQ33	1L
13	DQ6	7L	37	PH[1]	2B	61	DQ32	2L
14	DQ8	6K	38	SA	3A	62	DQ30	2M
15	DQ7	7K	39	SA	3C	63	DQ29	1N
16	$\overline{\text{SBW}}$a	5L	40	SA	2C	64	DQ31	2N
17	$\overline{\text{K}}$	4L	41	SA	2A	65	DQ28	1P
18	K	4K	42	DQ18	2D	66	DQ27	2P
19	G	4F	43	DQ19	1D	67	SA	3T
20	$\overline{\text{SBW}}$b	5G	44	DQ20	2E	68	SA	2R
21	DQ16	7H	45	DQ22	1E	69	SA	4N
22	DQ17	6H	46	DQ21	2F	70	M1	3R
23	DQ15	7G	47	DQ23	2G			
24	DQ14	6G	48	DQ24	1G			

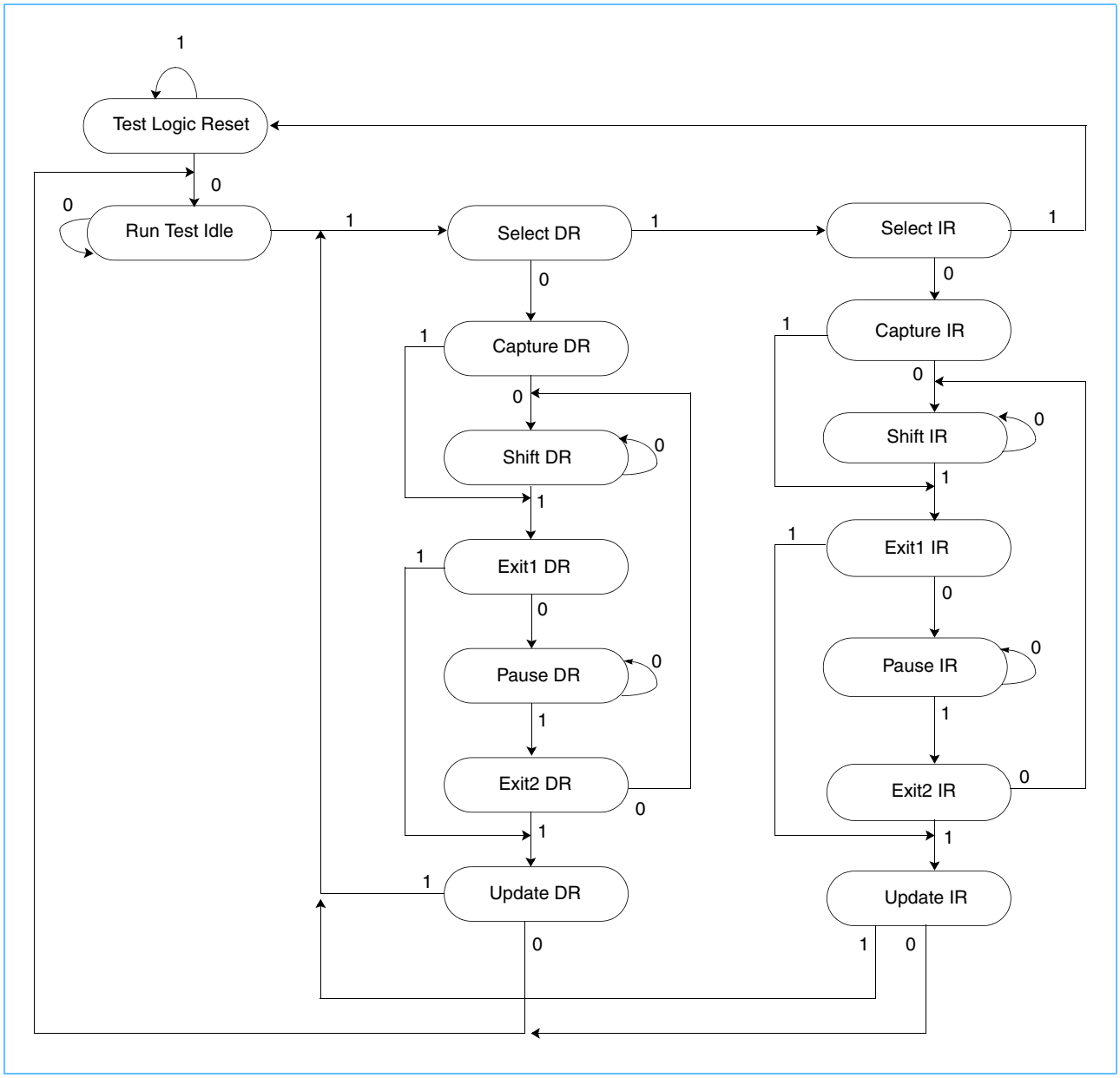
1. Input of PH register connected to V_{SS}.
2. Input of PH register connected to V_{DD}.

Boundary Scan Order **(256K x 18), (512K x 18)** (PH = Place Holder)

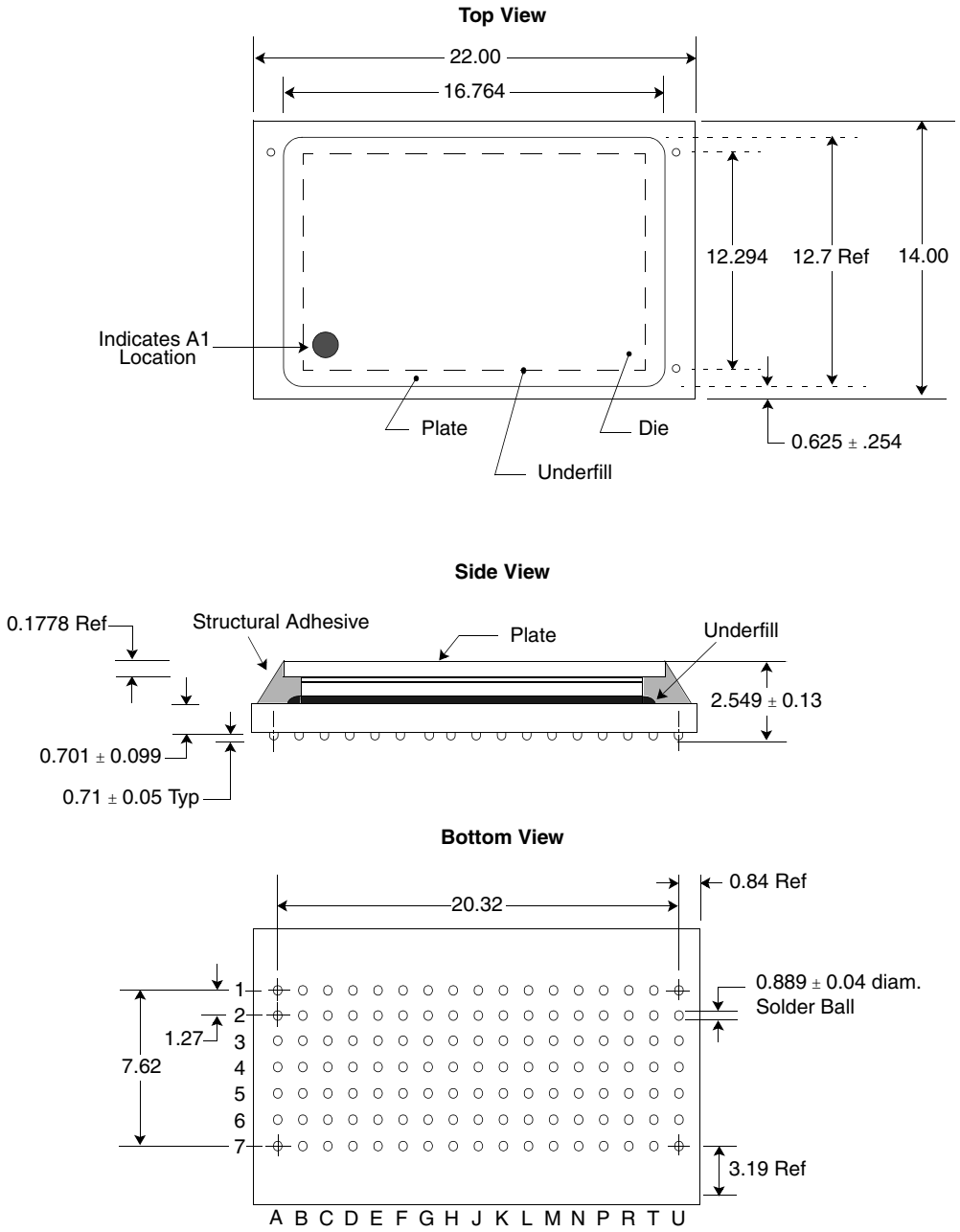
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	**27**	PH[1]	2B
2	SA	6T	**28**	SA	3A
3	SA	4P	**29**	SA	3C
4	SA	6R	**30**	SA	2C
5	SA	5T	**31**	SA	2A
6	ZZ	7T	**32**	DQ14	1D
7	DQ5	7P	**33**	DQ15	2E
8	DQ6	6N	**34**	DQ16	2G
9	DQ7	6L	**35**	DQ17	1H
10	DQ8	7K	**36**	$\overline{\text{SBWb}}$	3G
11	$\overline{\text{SBWa}}$	5L	**37**	ZQ	4D
12	$\overline{\text{K}}$	4L	**38**	$\overline{\text{SS}}$	4E
13	K	4K	**39**	PH[1]	4G
14	$\overline{\text{G}}$	4F	**40**	PH[2]	4H
15	DQ4	6H	**41**	$\overline{\text{SW}}$	4M
16	DQ3	7G	**42**	DQ13	2K
17	DQ2	6F	**43**	DQ12	1L
18	DQ1	7E	**44**	DQ10	2M
19	DQ0	6D	**45**	DQ11	1N
20	SA	6A	**46**	DQ9	2P
21	SA	6C	**47**	SA	3T
22	SA	5C	**48**	SA	2R
23	SA	5A	**49**	SA	4N
24	PH[1](4Mb), SA(8Mb)	6B	**50**	SA	2T
25	SA	5B	**51**	M1	3R
26	SA	3B			

1. Input of PH register connected to V_{SS}.
2. Input of PH register connected to V_{DD}.

TAP Controller State Machine



7 x17 BGA Dimensions



Note: All dimensions are in millimeters.

References

The following document provides recommendations, restrictions, and limitations for the second-level attachment process:

Double Sided 4Mb SRAM Coupled Cap PBGA Card Assembly Guide

Qualification information, including the scope of application conditions qualified, is available from your marketing representative.

Revision Log

Revision	Contents of Modification
9/1998	Initial release.
11/1998	Updated package diagram. Changed part numbers from Rev A to B.
2/16/1999	See Programmable Impedance Output Driver DC Electrical Characteristics: $I_{OH} = (V_{DDQ} \div 2) \div ((RQ \div 5) + 5) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$. $I_{OL} = (V_{DDQ} \div 2) \div (RQ \div 5) \pm 15\%$ @ $V_{OL} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
7/13/1999	Corrected 7 x17 BGA Dimensions on page 22. Added 3F speed sort.
9/30/1999	In Recommended DC Operating Conditions on page 7: - V_{DDQ} max changed from 1.9V to 2.0V
2/9/2000	Replaced Sleep Mode Timing Diagram on page 14. Added Sleep Mode Setup Time and Sleep Mode Hold Time to AC Characteristics on page 11. Replaced BGA dimensions diagram on page 22.
5/09/2000	In Recommended DC Operating Conditions on page 7: - V_{DDQ} max changed to 2.1V.
12/05/2000	Made various minor editorial changes and format refinements.
02/07/2001	Removed the document's Preliminary labels and statements. In Recommended DC Operating Conditions on page 7: - $V_{CM - CLK}$ max changed to 1.0V.
01/08/2002	Indicated that the programmable impedance multiplier is 5X.
04/19/2002	Matched the DQ BGA pinout on page 2 with Boundary Scan Order on pages 19 and 20.
June 12, 2002	Changed footers, and minor changes to wording and formatting.

The following are trademarks of International Business Machines Corporation in the United States, or other countries, or both.
IBM IBM Logo

IEEE and IEEE 802 are registered trademarks in the United States, owned by the Institute of Electrical and Electronics Engineers.

Other company, product and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in implantation, life support, space, nuclear, or military applications where malfunction may result in injury or death to persons. The information contained in this document does not affect or change IBM product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN “AS IS” BASIS. In no event will IBM be liable for damages arising directly or indirectly from any use of the information contained in this document.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351

The IBM home page can be found at http://www.ibm.com

The IBM Microelectronics Division home page can be found at http://www.chips.ibm.com

crrh3319.10
June 12, 2002