Preliminary

1Mb (32Kx36 & 64Kx18) SRAM

Features

- 32Kx36 or 64Kx18 organizations
- 0.25 Micron CMOS technology
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write
- Single Differential Extended HSTL Clock
- +3.3V Power Supply, Ground, 1.5V V_{DDQ}, and 0.75V V_{REF} or 1.8V V_{DDQ}, and 0.9V V_{REF}
- HSTL Input and Outputs
- Registered Addresses, Write Enables, Synchronous Select, and Data Ins
- Registered Outputs
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability and Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers
- Synchronous Sleep Mode

Description

IBM0436A11QLAA and IBM0418A11QLAA are 1Mb Synchronous Pipeline Mode, high-performance CMOS Static Random Access Memories (SRAM). These SRAMs are versatile, have a wide input/output (I/O) interface, and can achieve cycle times as short as 3ns. Differential K clocks are used to initiate the read/write operation; all internal operations are self-timed. At the rising edge of the K clock, all address, write-enables, sync select, and data input signals are registered internally. Data outputs are updated from output registers off the next rising edge of the K clock. An internal write buffer allows write data to follow one cycle after addresses and controls. The device is operated with a single +3.3V power supply and is compatible with HSTL I/O interfaces.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA10	SA9	NC	SA3	SA4	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA11	SA8	V_{DD}	SA2	SA5	NC
D	DQ23	DQ18	V_{SS}	ZQ	V_{SS}	DQ9	DQ14
E	DQ19	DQ24	V_{SS}	$\overline{SS}$	V_{SS}	DQ15	DQ10
F	V_{DDQ}	DQ20	V_{SS}	$\overline{G}$	V_{SS}	DQ11	V_{DDQ}
G	DQ21	DQ25	$\overline{SBWc}$	$\overline{C}$*	$\overline{SBWb}$	DQ16	DQ12
H	DQ26	DQ22	V_{SS}	C*	V_{SS}	DQ13	DQ17
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ35	DQ31	V_{SS}	K	V_{SS}	DQ4	DQ8
L	DQ30	DQ34	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ7	DQ3
M	V_{DDQ}	DQ29	V_{SS}	$\overline{SW}$	V_{SS}	DQ2	V_{DDQ}
N	DQ28	DQ33	V_{SS}	SA0	V_{SS}	DQ6	DQ1
P	DQ32	DQ27	V_{SS}	SA1	V_{SS}	DQ0	DQ5
R	NC	SA14	M1*	V_{DD}	M2*	SA6	NC
T	NC	NC	SA13	SA12	SA7	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

* M1 and M2 are read protocol mode pins. For this application, M1 and M2 must be connected to V_{SS} and V_{DD}, respectively. C-clocks must be left floating for all single-clock read protocols.

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA10	SA9	NC	SA3	SA4	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA11	SA8	V_{DD}	SA2	SA5	NC
D	DQ14	NC	V_{SS}	ZQ	V_{SS}	DQ0	NC
E	NC	DQ15	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ1
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ2	V_{DDQ}
G	NC	DQ16	$\overline{SBWb}$	$\overline{C}$*	V_{SS},NC	NC	DQ3
H	DQ17	NC	V_{SS}	C*	V_{SS}	DQ4	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ8
L	DQ12	NC	V_{SS},NC	$\overline{K}$	$\overline{SBWa}$	DQ7	NC
M	V_{DDQ}	DQ11	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ10	NC	V_{SS}	SA0	V_{SS}	DQ6	NC
P	NC	DQ9	V_{SS}	SA1	V_{SS}	NC	DQ5
R	NC	SA14	M1	V_{DD}	M2	SA6	NC
T	NC	SA15	SA13	NC	SA7	SA12	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

* M1 and M2 are read protocol mode pins. For this application, M1 and M2 must be connected to V_{SS} and V_{DD} respectively. C-clocks must be left floating for all single-clock read protocols.

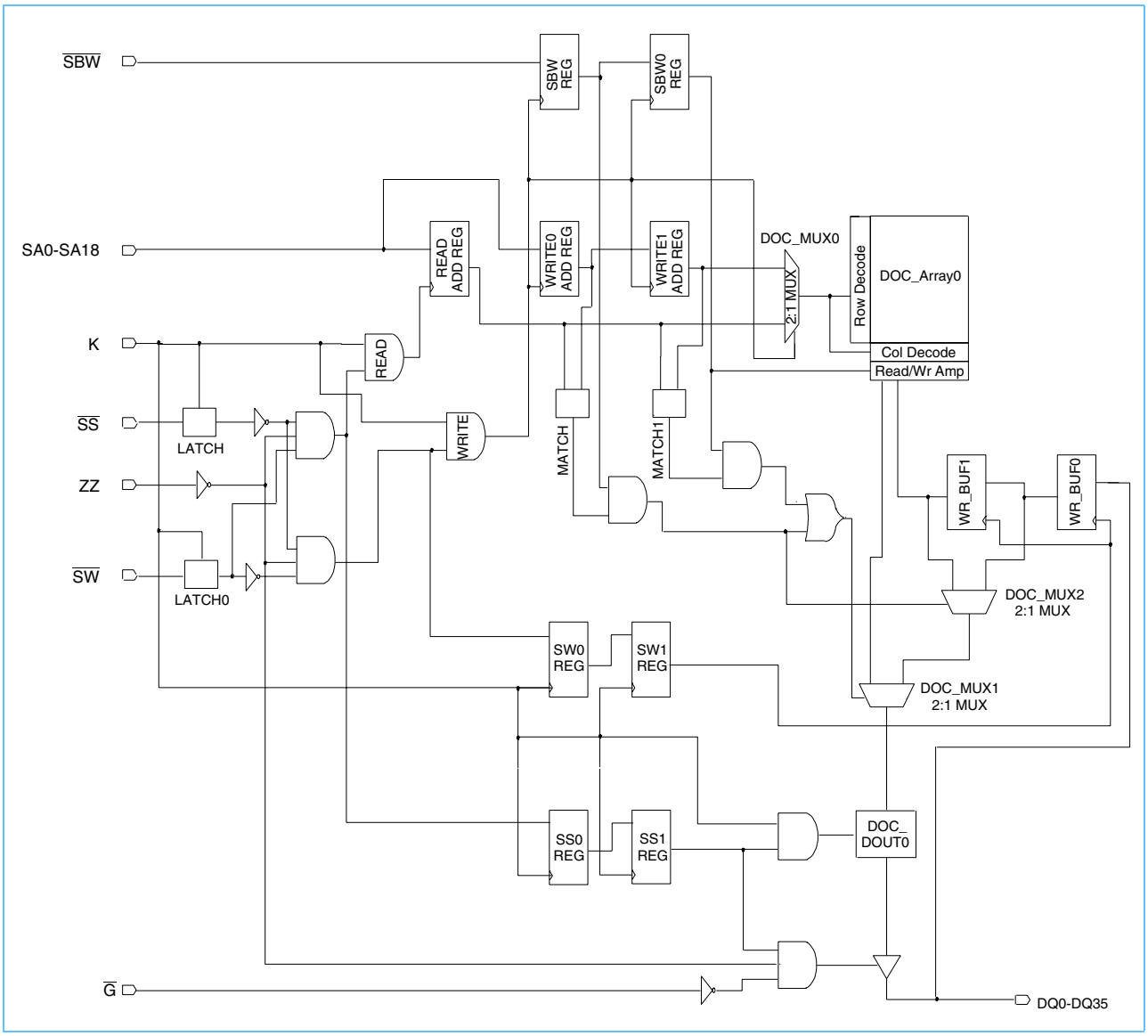
Pin Description

SA0-SA15	Address Input	$\overline{G}$	Asynchronous Output Enable
DQ0-DQ35	Data I/O	$\overline{SS}$	Synchronous Select
K, $\overline{K}$	Differential Input-Register Clocks	M1, M2	Mode Inputs. Selects Read Protocol Operation.
$\overline{SW}$	Write Enable, Global	V_{REF}(2)	GTL/HSTL Input Reference Voltage
$\overline{SBWa}$	Write Enable, Byte a (DQ0-DQ8)	V_{DC}	Power Supply (+3.3V)
$\overline{SBWb}$	Write Enable, Byte b (DQ9-DQ17)	V_{SS}	Ground
$\overline{SBWc}$	Write Enable, Byte c (DQ18-DQ26)	V_{DDQ}	Output Power Supply
$\overline{SBWd}$	Write Enable, Byte d (DQ27-DQ35)	ZZ	Synchronous Sleep Mode
TMS,TDI,TCK	IEEE® 1149.1 Test Inputs (LVTTL levels)	ZQ	Output Driver Impedance Control
TDO	IEEE 1149.1 Test Output (LVTTL level)	NC	No Connect

Ordering Information

Part Number	Organization	Speed	Leads
IBM0418A11QLAA - 3	64Kx18	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0418A11QLAA - 3N	64Kx18	1.85ns Access / 3.7ns Cycle	7 x 17 BGA
IBM0418A11QLAA - 4	64Kx18	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0436A11QLAA - 3	32Kx36	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0436A11QLAA - 3N	32Kx36	1.85ns Access / 3.7ns Cycle	7 x 17 BGA
IBM0436A11QLAA - 4	32Kx36	2.0ns Access / 4.0ns Cycle	7 x 17 BGA

Block Diagram



SRAM Features

Late Write

The Late Write function allows for write data to be registered one cycle after addresses and controls. This feature eliminates one bus-turnaround cycle, necessary when going from a read to a write operation. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. When a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array is updated with address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte-by-byte basis. When only one byte is written during a write cycle, read data from the last written address has new byte data from the write buffer and remaining bytes from the SRAM array.

Mode Control

Mode control pins M1 and M2 are used to select four different JEDEC-standard read protocols. This SRAM supports single clock, pipeline operation (M1 = V_{SS}, M2 = V_{DD}). This datasheet describes single clock pipeline functionality only. Mode control inputs must be set at power up and must not change during SRAM operation. This SRAM is tested only in the pipeline mode.

Sleep Mode

The sleep mode is enabled by switching the synchronous ZZ signal High. When the SRAM is in the sleep mode, the outputs go to a High-Z state and the SRAM draws standby current. SRAM data is preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM; each SRAM requires a dedicated RQ. The allowable range of RQ to ensure impedance matching is between 175Ω and 350Ω, with the tolerance described in Programmable Impedance Output Driver DC Electrical Characteristics on page 9. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The total external capacitance (including wiring) seen by the ZQ ball should be minimized (less than 7.5 pF).

Programmable Impedance/Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation can only move the output driver impedance level one step at a time towards the optimum level. The output driver has 32 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, triggering an update. The user can invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold about the K clock to ensure the proper update. There are no power-up requirements for programmable impedance initialization of the SRAM; however, to ensure optimum output driver impedance after power up, the SRAM needs 4096 clock cycles followed by a Low-Z to High-Z transition.

Power-Up/Power-Down Sequencing

The power supplies must be powered up in the following order: V_{DD}, V_{DDQ}, V_{REF}, and Inputs. The power-down sequence must be in the reverse order. V_{DDQ} may not exceed V_{DD} by more than 0.6V at any time.

Clock Truth Table

K	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWa}$	$\overline{SBWb}$	$\overline{SBWc}$	$\overline{SBWd}$	DQ (n)	DQ (n+1)	Mode
LH	L	L	H	X	X	X	X	X	D_{OUT} 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	D_{IN} 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	D_{IN} 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	D_{IN} 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	D_{IN} 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	D_{IN} 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Output Enable Truth Table

Operation (n, n+1)	$\overline{G}$ (n)	DQ (n)	DQ (n+1)
Read	L	D_{OUT} 0-35	D_{OUT} 0-35
Read	H	High-Z	High-Z
Sleep (ZZ = H)	X	High-Z	High-Z
Write ($\overline{SW}$ = L)	X	X	High-Z
Deselect ($\overline{SS}$ = H)	X	X	High-Z

Absolute Maximum Rating s

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.3	V	1
Output Power Supply Voltage	V_{DDQ}	-0.5 to 2.825	V	1
Input Voltage	V_{IN}	-0.5 to 4.3	V	1, 2
DQ Input Voltage	V_{DQIN}	-0.5 to 2.825	V	1
Operating Temperature	T_A	0 to 85	°C	1
Junction Temperature	T_J	110	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Excludes DQ inputs.

Recommended DC Operating Conditions (T_A = 0 to + 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.3 - 5%	3.3	3.3 + 5%	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	1.9	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.1	—	V_{DDQ} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	V_{REF} - 0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	0.9	V	1, 6
Clocks Signal Voltage	$V_{IN - CLK}$	-0.3	—	V_{DDQ} + 0.3	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF - CLK}$	0.1	—	V_{DDQ} + 0.6	V	1, 5
Clocks Common Mode Voltage	$V_{CM - CLK}$	0.55	—	0.90	V	1
Output Current	I_{OUT}	—	5	8	mA	

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3 V, V_{IH}(Max)AC = V_{DDQ} + 0.85 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC = -1.5 V (pulse width ≤ 4.0ns).
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (K, $\overline{K}$).
5. $V_{DIF-CLK}$ specifies the minimum Clock differential voltage required for switching.
6. Peak to Peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current- **x36** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD3} I_{DD3N} I_{DD4}	— —	0.470 0.435 0.420	A	1, 3
Average Power Supply Operating Current - **x18** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD3} I_{DD3N} I_{DD4}	— —	0.450 0.415 0.400	A	1, 3
Power Supply Standby Current ($\overline{SS}$ = V_{IH}, ZZ = V_{IH}. All other inputs = V_{IH} or V_{IH}, I_{IH} = 0)	I_{SBSS}	—	125	mA	1
Power Supply Sleep Current (ZZ = V_{IH}, All other inputs = V_{IH} or V_{IL}, I_{OUT} = 0)	I_{SBZZ}	—	65	mA	1, 5
Input Leakage Current, any input (except JTAG) (V_{IN} = V_{SS} or V_{DDQ})	I_{LI}	-2	+2	µA	
Output Leakage Current (V_{OUT} = V_{SS} or V_{DDQ}, DQ in High-Z)	I_{LO}	-5	+5	µA	
Output “High” Level Voltage (I_{OH} = -8mA)	V_{OH}	V_{DDQ} -.4	V_{DDQ}	V	2, 4
Output “Low” Level Voltage (I_{OL} = +8mA)	V_{OL}	V_{SS}	V_{SS} + .4	V	2, 4
JTAG Leakage Current (V_{IN} = V_{SS} or V_{DD})	I_{LIJTAG}	-50	+10	µA	6

1. I_{OUT} = Device Output Current.
2. Minimum Impedance Output Driver.
3. The numeric suffix indicates part operating at speed as indicated in AC Characteristics on page 12: that is, I_{DD3} indicates 3ns cycle time.
4. JEDEC Standard JESD8-6 Class 1 Compatible.
5. When ZZ = High, spec is guaranteed at 75°C Junction Temperature.
6. For JTAG inputs only.

PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	RΘJC	tbd	°C/W

Capacitance (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%, f = 1MHz)

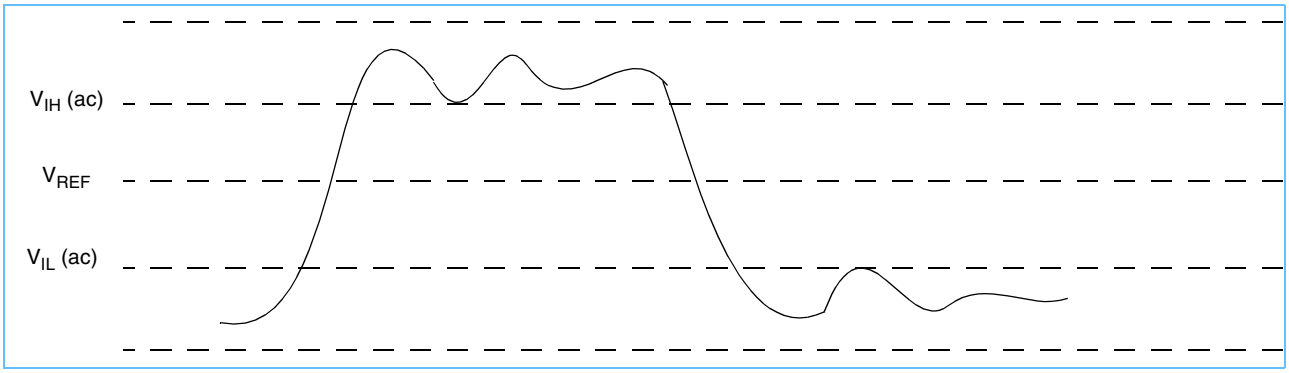
Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	4	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	5	pF

AC Input Characteristics

Item	Symbol	Min	Max	Notes
AC Input Logic High	V_{IH} (ac)	0.4v + V_{REF}		3
AC Input Logic Low	V_{IL} (ac)		V_{REF} - 0.4V	3
Clock Input Differential Voltage	V_{DIF} (ac)	0.7V		2
V_{REF} Peak to Peak ac Voltage	V_{REF} (ac)		5% V_{REF} (dc)	1

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function on V_{IH} and V_{IL} levels to clock inputs.
3. See AC Input Definition figure below.

AC Input Definition



Programmable Impedance Output Driver DC Electrical Characteristics

(T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%, V_{DDQ} = 1.5V)

Parameter	Symbol	Min.	Max.	Units	Notes
Output “High” Level Voltage	V_{OH}	$V_{DDQ / 2}$	V_{DDQ}	V	1, 3
Output “Low” Level Voltage	V_{OL}	V_{SS}	$V_{DDQ / 2}$	V	2, 3

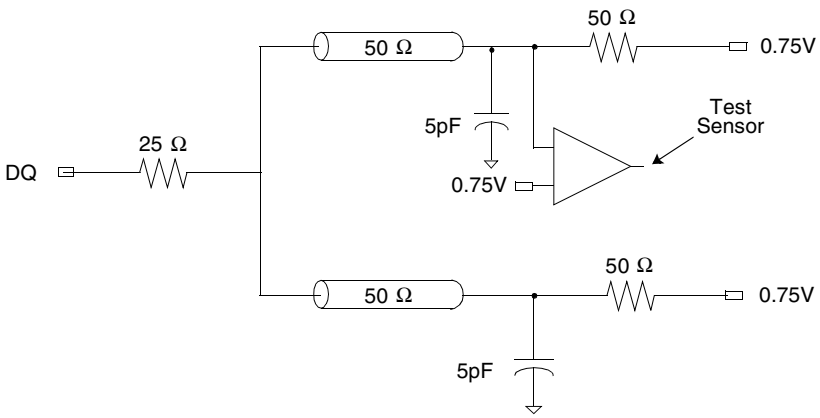
1. $I_{OH} = (V_{DDQ}/2)/ (RQ/5 +5) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ For: $175\Omega \le RQ \le 350\Omega$.
2. $I_{OL} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right) \pm 15\%$ @ $V_{OL} = V_{DDQ} / 2$ For: $175\Omega \le RQ \le 350\Omega$.
3. Parameter tested with $RQ = 250\Omega$ and V_{DDQ} = 1.5V or 1.8V.

AC Test Conditions (T_A = 0 to + 85°C, V_{DD} = 3.3V -5%, +10%, V_{DDQ} = 1.5V)

Parameter	Symbol	Conditions	Units	Notes
Output Driver Supply Voltage	V_{DDQ}	1.5		
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Reference Voltage	V_{REF}	0.75	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.75	V	
Clocks Common Mode Voltage	V_{CM-CLK}	0.75	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level (except K, C Clocks)		0.75	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1, 2

1. See AC Test Loading figure below.
2. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5V.

AC Test Loading

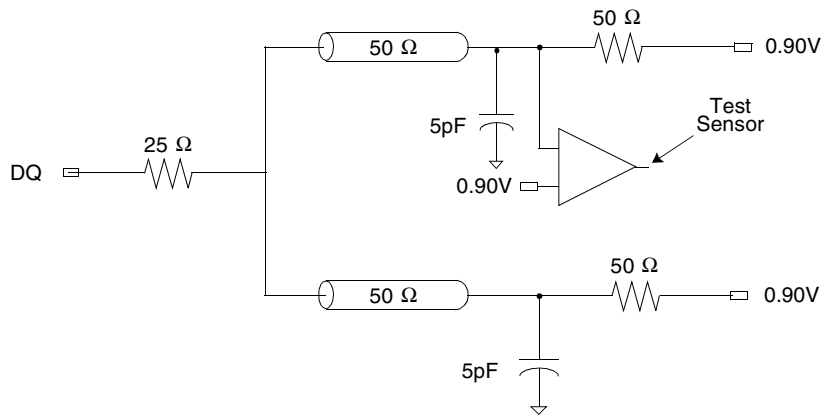


AC Test Conditions (T_A = 0 to + 85°C, V_{DD} = 3.3V -5%, +10%, V_{DDQ} = 1.8V)

Parameter	Symbol	Conditions	Units	Notes
Output Driver Supply Voltage	V_{DDQ}	1.8		
Input High Level	V_{IH}	1.5	V	
Input Low Level	V_{IL}	0.3	V	
Input Reference Voltage	V_{REF}	0.90	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.90	V	
Clocks Common Mode Voltage	V_{CM-CLK}	0.90	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level (except K, C Clocks)		0.90	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1, 2

1. See AC Test Loading figure below.
2. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.8V.

AC Test Loading

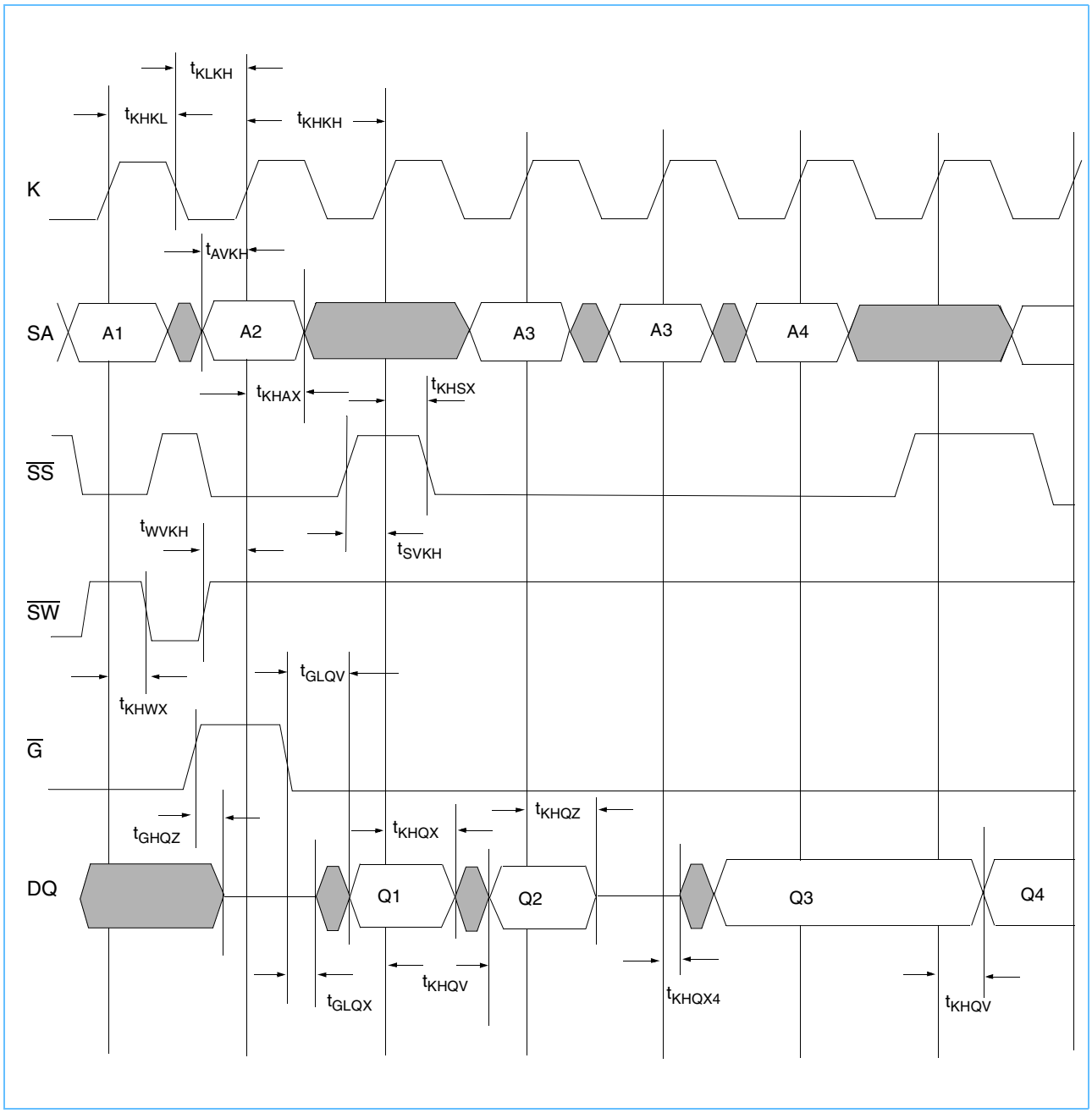


AC Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%, VDDQ = 1.5 or 1.8V)

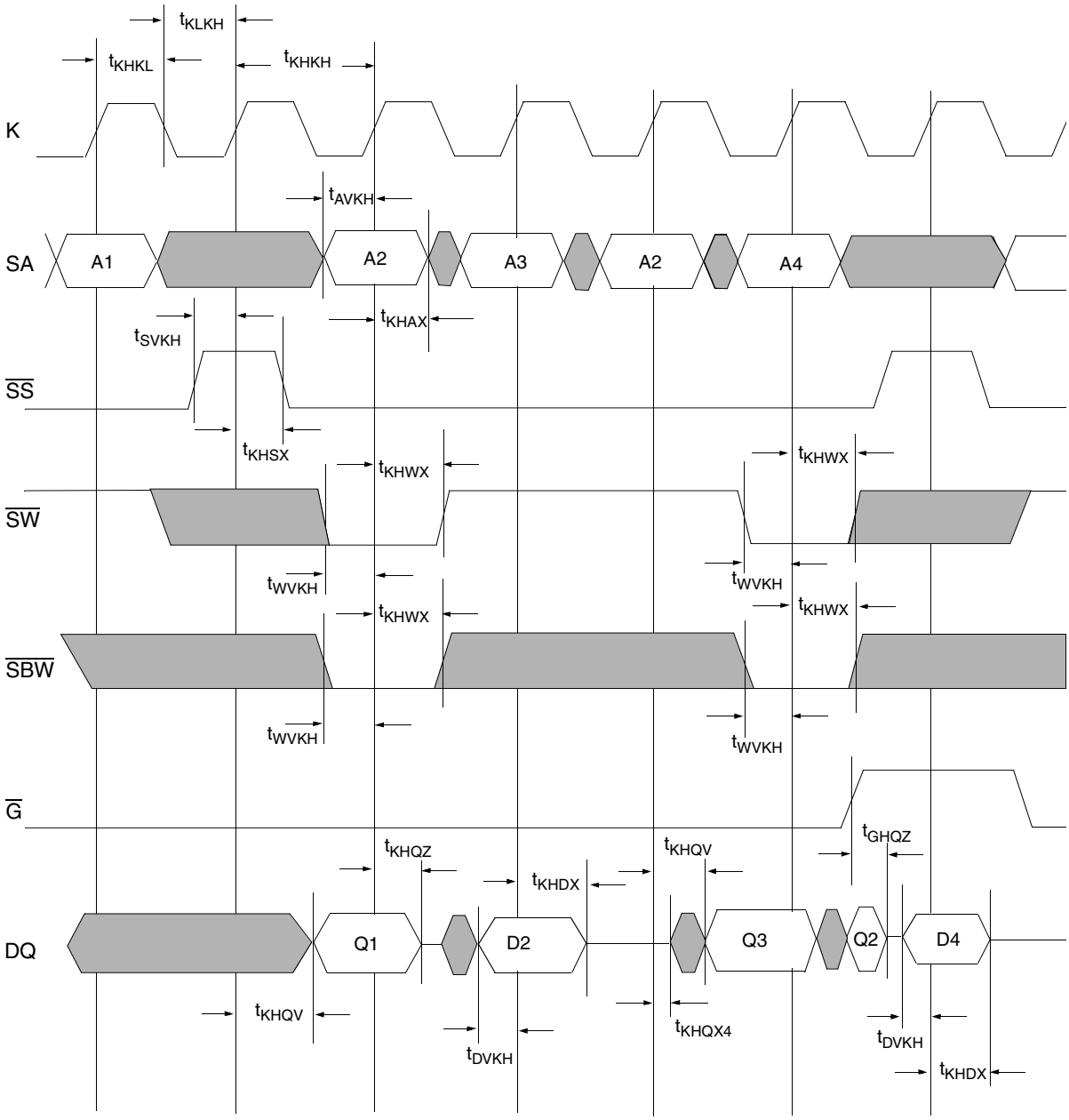
Parameter	Symbol	3		3N		4		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	3.0	—	3.7	—	4.0	—	ns	
Clock High Pulse Width	t_{KHKL}	1.2	—	1.5	—	1.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	1.2	—	1.5	—	1.5	—	ns	
Clock to Output Valid	t_{KHQV}	—	1.7	—	1.85	—	2.0	ns	1
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	ns	3
Address Hold Time	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	3
Sync Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	ns	3
Sync Select Hold Time	t_{KHSX}	0.5	—	0.5	—	0.5	—	ns	3
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	ns	3
Write Enables Hold Time	t_{KHWX}	0.5	—	0.5	—	0.5	—	ns	3
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	ns	3
Data In Hold Time	t_{KHDX}	0.5	—	0.5	—	0.5	—	ns	3
Data Out Hold Time	t_{KHQX}	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output High-Z	t_{KHQZ}	—	2.25	—	2.25	—	2.25	ns	1, 4
Clock High to Output Active	t_{KHQX4}	0.5	—	0.5	—	0.5	—	ns	1, 4
Output Enable to High-Z	t_{GHQZ}	—	2.0		2.0		2.0	ns	1, 4
Output Enable to Low-Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	ns	1
Output Enable to Output Valid	t_{GLQV}	—	2.0	—	2.0	—	2.0	ns	1
Output Enable Setup Time	t_{GHKH}	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable Hold TIme	t_{KHGX}	1.5	—	1.5	—	1.5	—	ns	1, 2
Sleep Mode Recovery TIme	t_{ZZR}	200	—	200	—	200	—	ns	
Sleep Mode Enable TIme	t_{ZZE}	—	6	—	7.4	—	8	ns	

1. See AC Test Loading figures on page 10 and page 11.
2. Output Driver Impedance update specifications for $\overline{G}$ induced updates. Write and Deselect cycles will also induce Output Driver updates during High-Z.
3. In use conditions V_{IH},V_{IL},T_{RISE}, T_{FALL} of inputs must be within 20% of V_{IH}, V_{IL}, T_{RISE}, T_{FALL} of Clock.
4. Verified by design and tested without guardbands.

Read and Deselect Cycles Timing Diagram



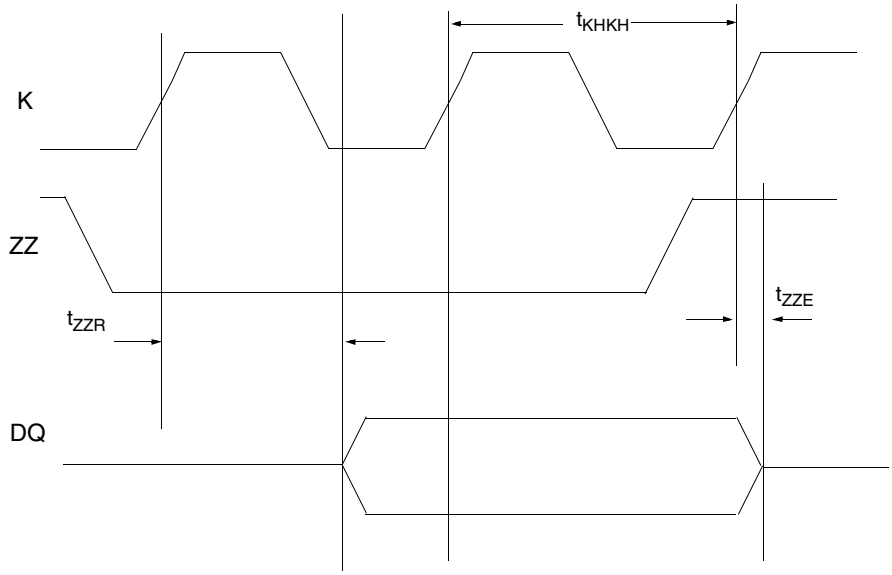
Read and Write Cycles Timing Diagram



Notes:

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Synchronous Sleep Mode Timing Diagram



The t_{ZZR} is timed from the first rising K clock edge after the fall of ZZ.

The t_{ZZE} is timed from the first rising K clock edge after the rise of ZZ.

IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions as defined in the IEEE Standard 1149.1 that are intended to test the interconnection between the SRAM I/Os and the printed circuit board traces or other components. There is no multiplexer in the path from the I/O pins to the SRAM core.

In conformance with the IEEE std. 1149.1, the SRAM contains a test access port (TAP) controller, instruction register, boundary scan register, bypass register, and an ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, a test reset (TRST) signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG DC Operating Characteristics (T_A = 0 to +85°C)

Operates with JEDEC Standard JESD8A (3.3V) logic signal levels

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	—	V_{DD} + 0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	—	—	V	1, 2
JTAG Output Low Level	V_{OL1}	—	—	0.4	V	1, 3

1. All JTAG Inputs/Outputs are LVTTL Compatible only.
2. $I_{OH1} \geq$ -I8mAI.
3. $I_{OL1} \geq$ +I8mAI.

JTAG AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

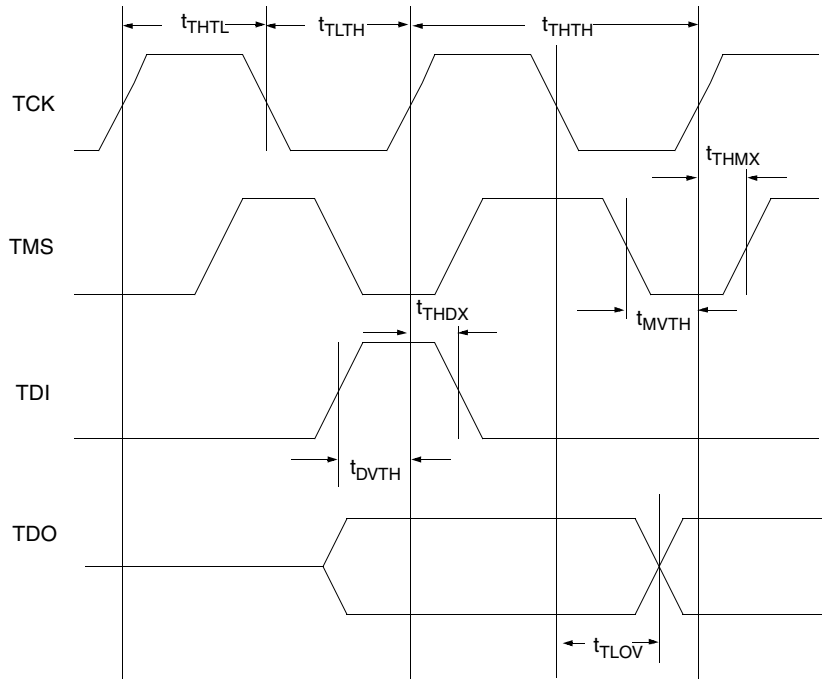
Parameter	Symbol	Conditions	Units
Input Pulse High Level	V_{IH1}	3.0	V
Input Pulse Low Level	V_{IL1}	0.0	V
Input Rise Time	T_{R1}	2.0	ns
Input Fall Time	T_{F1}	2.0	ns
Input and Output Timing Reference Level		1.5	V

JTAG AC Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{THTL}	7	—	ns	
TCK Low Pulse Width	t_{TLTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See AC Test Loading on page 10.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

* The Boundary Scan chain consists of the following bits:
- 36 or 18 bits for Data Inputs, depending on x18 or x36 configuration
- 15 bits for SA0 - SA14in x36, 16 bits for SA0 - SA15 in x18
- 4 bits for $\overline{\text{SBWa}}$ - $\overline{\text{SBWd}}$ in x36, 2 bits for $\overline{\text{SBWa}}$ and $\overline{\text{SBWb}}$ in x18
- 9 bits for K, $\overline{\text{K}}$, ZQ, $\overline{\text{SS}}$, $\overline{\text{G}}$, $\overline{\text{SW}}$, ZZ, M1 and M2
- 6 bits for Place Holders

* K and $\overline{\text{K}}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacturer JEDEC Code (11:1)	Start Bit(0)
32Kx36	X111	0001100100	100000	000 101 001 00	1
64Kx18	X111	0010000011	100000	000 101 001 00	1

Note: X is don't care for bit 31. It can be either logic "0" or "1".

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	
010	SAMPLE-Z	1
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	2, 3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

List of IEEE 1149.1 Standard Violations

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

Boundary Scan Order (x36) (PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	**25**	DQ11	6F	**49**	DQ22	2H
2	SA1	4P	**26**	DQ10	7E	**50**	DQ26	1H
3	SA12	4T	**27**	DQ15	6E	**51**	$\overline{\text{SBWc}}$	3G
4	SA6	6R	**28**	DQ14	7D	**52**	ZQ	4D
5	SA7	5T	**29**	DQ9	6D	**53**	$\overline{\text{SS}}$	4E
6	ZZ	7T	**30**	SA4	6A	**54**	PH[1]	4G
7	DQ0	6P	**31**	SA5	6C	**55**	PH[2]	4H
8	DQ5	7P	**32**	SA2	5C	**56**	$\overline{\text{SW}}$	4M
9	DQ6	6N	**33**	SA3	5A	**57**	$\overline{\text{SBWd}}$	3L
10	DQ1	7N	**34**	PH[1]	6B	**58**	DQ35	1K
11	DQ2	6M	**35**	PH[1]	5B	**59**	DQ31	2K
12	DQ7	6L	**36**	PH[1]	3B	**60**	DQ30	1L
13	DQ3	7L	**37**	PH[1]	2B	**61**	DQ34	2L
14	DQ4	6K	**38**	SA9	3A	**62**	DQ29	2M
15	DQ8	7K	**39**	SA8	3C	**63**	DQ28	1N
16	$\overline{\text{SBWa}}$	5L	**40**	SA11	2C	**64**	DQ33	2N
17	$\overline{\text{K}}$	4L	**41**	SA10	2A	**65**	DQ32	1P
18	K	4K	**42**	DQ18	2D	**66**	DQ27	2P
19	$\overline{\text{G}}$	4F	**43**	DQ23	1D	**67**	SA13	3T
20	$\overline{\text{SBWb}}$	5G	**44**	DQ24	2E	**68**	SA14	2R
21	DQ17	7H	**45**	DQ19	1E	**69**	SA0	4N
22	DQ13	6H	**46**	DQ20	2F	**70**	M1	3R
23	DQ12	7G	**47**	DQ25	2G			
24	DQ16	6G	**48**	DQ21	1G			

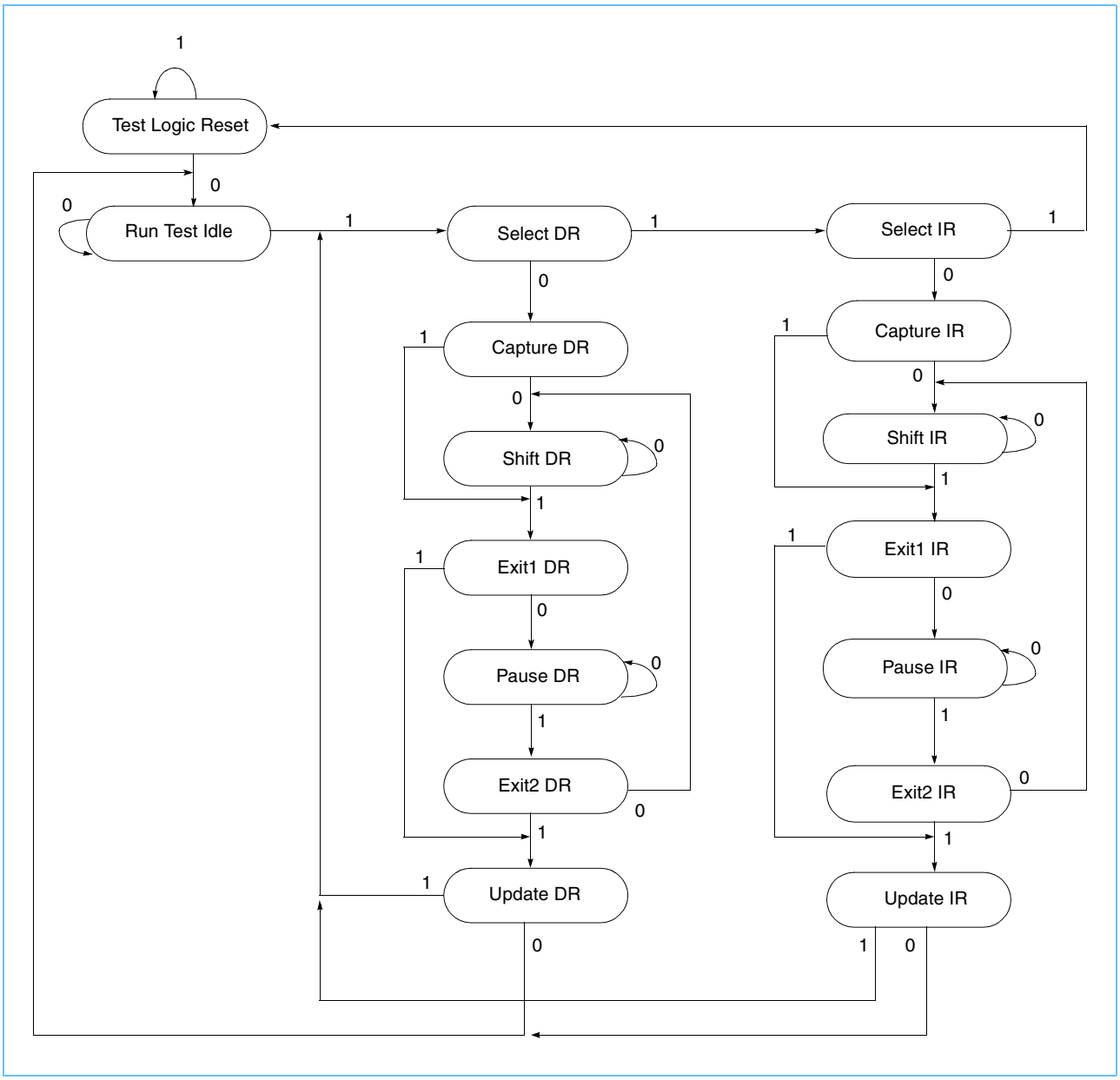
1. Input of PH register connected to V_{SS}.
2. Input of PH register connected to V_{DD}.

Boundary Scan Order (x18) (PH =Place Holder)

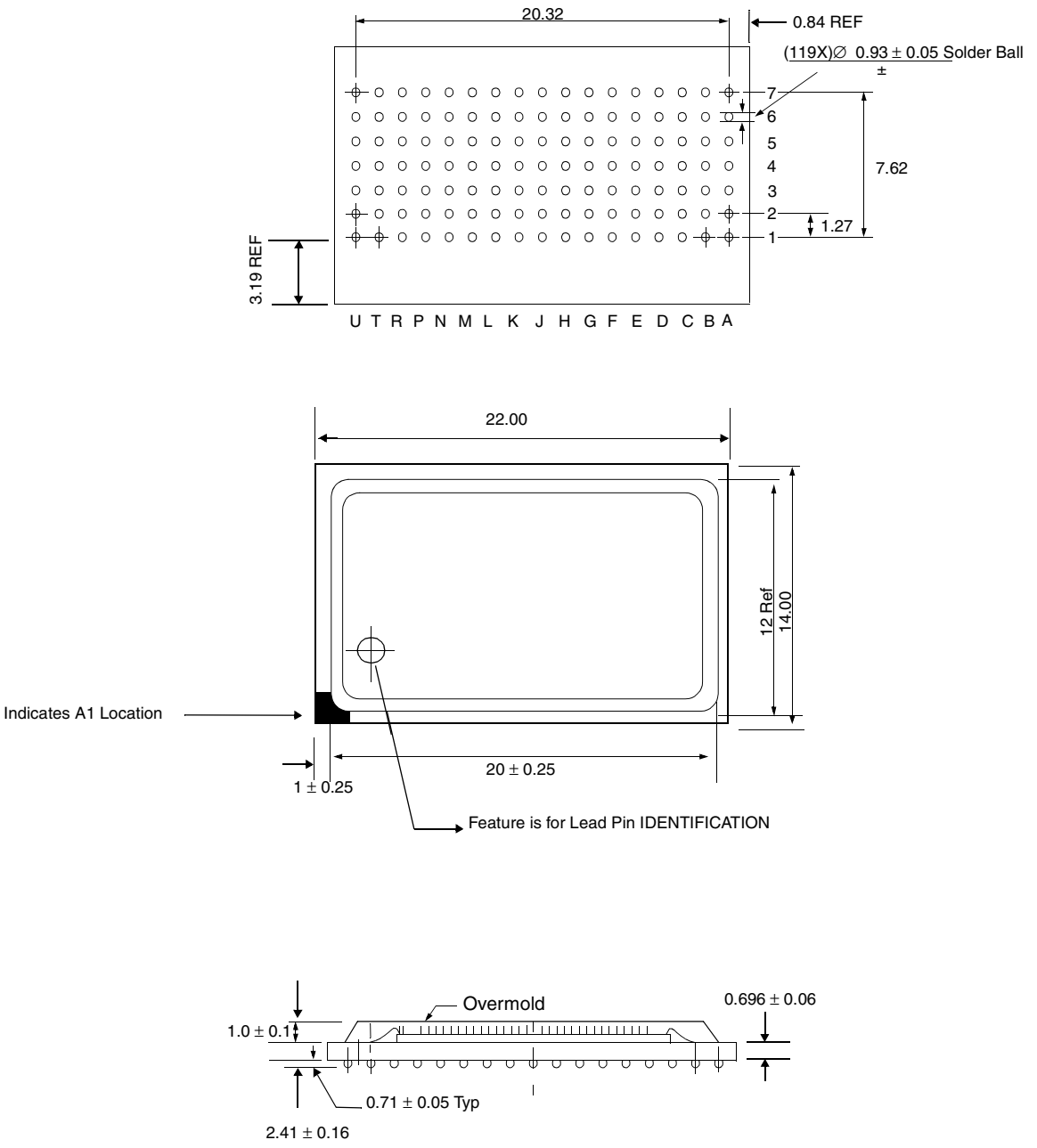
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	**27**	PH[1]	2B
2	SA12	6T	**28**	SA9	3A
3	SA1	4P	**29**	SA8	3C
4	SA6	6R	**30**	SA11	2C
5	SA7	5T	**31**	SA10	2A
6	ZZ	7T	**32**	DQ14	1D
7	DQ5	7P	**33**	DQ15	2E
8	DQ6	6N	**34**	DQ16	2G
9	DQ7	6L	**35**	DQ17	1H
10	DQ8	7K	**36**	$\overline{\text{SBWb}}$	3G
11	$\overline{\text{SBWa}}$	5L	**37**	ZQ	4D
12	$\overline{\text{K}}$	4L	**38**	$\overline{\text{SS}}$	4E
13	K	4K	**39**	PH[1]	4G
14	$\overline{\text{G}}$	4F	**40**	PH[2]	4H
15	DQ4	6H	**41**	$\overline{\text{SW}}$	4M
16	DQ3	7G	**42**	DQ13	2K
17	DQ2	6F	**43**	DQ12	1L
18	DQ1	7E	**44**	DQ11	2M
19	DQ0	6D	**45**	DQ10	1N
20	SA4	6A	**46**	DQ9	2P
21	SA5	6C	**47**	SA13	3T
22	SA2	5C	**48**	SA14	2R
23	SA3	5A	**49**	SA0	4N
24	PH[1]	6B	**50**	SA15	2T
25	PH[1]	5B	**51**	M1	3R
26	PH[1]	3B			

1. Input of PH register connected to V_{SS}.
2. Input of PH register connected to V_{DD}.

TAP Controller State Machine



7 x 17 BGA Dimensions



Note: All dimensions in millimeters

References

The following documents give recommendations, restrictions, and limitations for 2nd level attach process:

Double Sided 4Mb SRAM Coupled Cap PBGA Card Assembly Guide

Qualification information, including the scope of application conditions qualified, is available from your IBM sales representative.

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Revision Log

Revision	Contents of Modification
3/06/99	Initial release.
8/05/99	Updated pinouts with SA# and DQ#s for clarification.
10/01/99	Updated package diagram
05/23/2000	Included 1.8V V_{DDQ} levels. Updated package diagram for correct bga ball size.
8/03/01	Revision 01, edited for release to the web.

Printed in the United States of America August 2001

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nrrh3316.01
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