

## Document Title

**256K x16 bit 2.3 ~ 2.7V Super Low Power FCMOS Slow SRAM**

## Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Initial Draft	Dec.20.2000	Preliminary
01	Changed Logo	Mar.23.2001	Preliminary
02	Changed lsb1 values Changed part No Q -> L	Jun.07.2001	Preliminary
03	Changed Package Size (6.1mm -> 6.0mm)	Aug.07.2001	Preliminary

**DESCRIPTION**

The HY62LF16406D is a high speed, super low power and 4Mbit full CMOS SRAM organized as 256K words by 16bits. The HY62LF16406D uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

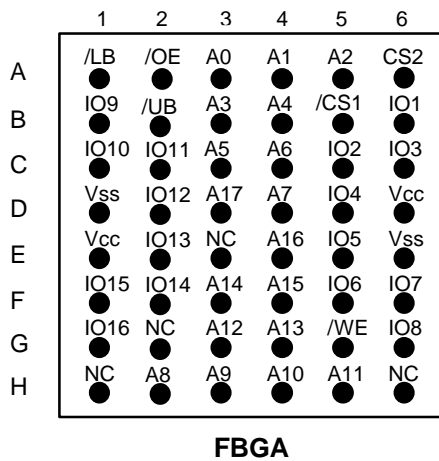
**FEATURES**

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup
  - 1.5V(min) data retention
- Standard pin configuration
  - 48-ball FBGA

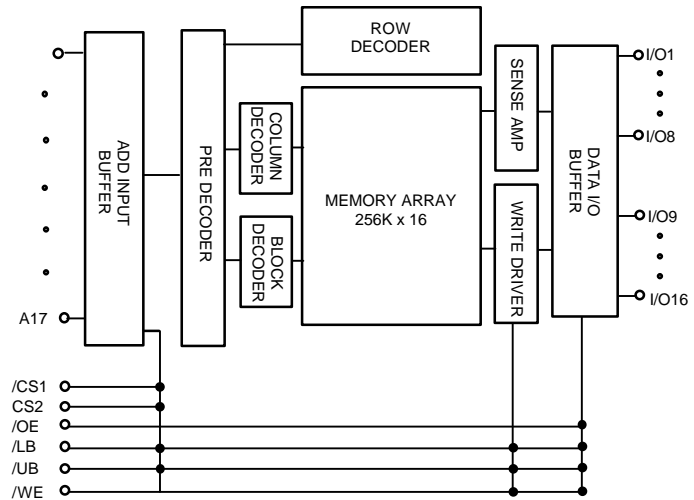
Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)		Temperature (°C)
				LL	SL	
HY62LF16406C-I	2.3~2.7	70/85	3	10	5	-40~85

Note 1. Blank : Commercial, I : Industrial  
 2. Current value is max.

**PIN CONNECTION**



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Pin Name	Pin Function	Pin Name	Pin Function
/CS1, CS2	Chip Select	I/O1~I/O16	Data Inputs/Outputs
/WE	Write Enable	A0~A17	Address Inputs
/OE	Output Enable	Vcc	Power (2.3~2.7V)
/LB	Lower Byte Control (I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control (I/O9~I/O16)	NC	No Connection

**ORDERING INFORMATION**

Part No.	Speed	Power	Temp	Package
HY62LF16406D-DF(I)	70/85	LL-part	I	FBGA
HY62LF16406D-SF(I)	70/85	SL-part	I	FBGA

Note 1. Blank : Commercial, I : Industrial

**ABSOLUTE MAXIMUM RATINGS (1)**

Symbol	Parameter	Rating	Unit	Remark
V <sub>IN</sub> , V <sub>OUT</sub>	Input/Output Voltage	-0.3 to 3.0	V	
V <sub>CC</sub>	Power Supply	-0.3 to 4.0	V	
T <sub>A</sub>	Operating Temperature	-40 to 85	°C	HY62LF16406D-I
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C	
P <sub>D</sub>	Power Dissipation	1.0	W	
T <sub>SO</sub> LDER	Ball Soldering Temperature & Time	260 • 10	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**TRUTH TABLE**

/CS1	CS2	/WE	/OE	/LB	/UB	Mode	I/O Pin		Power
							I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	X	Deselected	Hi-Z	Hi-Z	Standby
X	L	X	X	X	X				
X	X	X	X	H	H				
L	H	H	H	L	X	Output Disabled	Hi-Z	Hi-Z	Active
				X	L				
L	H	H	L	L	H	Read	DOUT	Hi-Z	Active
				H	L		Hi-Z	DOUT	
				L	L		DOUT	DOUT	
L	H	L	X	L	H	Write	DIN	Hi-Z	Active
				H	L		Hi-Z	DIN	
				L	L		DIN	DIN	

Note:

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care (V<sub>IL</sub> or V<sub>IH</sub>)
- /UB, /LB(Upper, Lower Byte enable)  
 These active LOW inputs allow individual bytes to be written or read.  
 When /LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.  
 When /UB is LOW, data is written or read to the upper byte, I/O 9 -I/O 16.

**RECOMMENDED DC OPERATING CONDITION**

Symbol	Parameter	Min.	Typ	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.3	2.5	2.7	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>1</sup>	-	0.6	V

Note : 1. Undershoot : V<sub>IL</sub> = -1.5V for pulse width less than 30ns  
 2. Undershoot is sampled, not 100% tested.

**DC ELECTRICAL CHARACTERISTICS**

 T<sub>A</sub> = -40°C to 85°C

Sym	Parameter	Test Condition	Min	Typ <sup>1</sup>	Max	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	1	uA
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , /CS1 = V <sub>IH</sub> or CS2=V <sub>IL</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub> or /UB = V <sub>IH</sub> , /LB = V <sub>IH</sub>	-1	-	1	uA
I <sub>CC</sub>	Operating Power Supply Current	/CS1 = V <sub>IL</sub> , CS2=V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA			3	mA
I <sub>CC1</sub>	Average Operating Current	/CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Cycle Time = Min, 100% Duty, I <sub>I/O</sub> = 0mA			25	mA
		/CS1 ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V, Cycle Time = 1us, 100% Duty, I <sub>I/O</sub> = 0mA			3	mA
I <sub>SB</sub>	Standby Current (TTL Input)	/CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or /UB, /LB = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.3	mA
I <sub>SB1</sub>	Standby Current (CMOS Input)	/CS1 ≥ V <sub>CC</sub> - 0.2V or CS2 ≤ V <sub>SS</sub> + 0.2V or /UB, /LB ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V	SL	0.2	5	uA
			LL	0.2	10	uA
V <sub>OL</sub>	Output Low	I <sub>OL</sub> = 0.5mA	-	-	0.4	V
V <sub>OH</sub>	Output High	I <sub>OH</sub> = -0.5mA	2.0	-	-	V

Note

1. Typical values are at V<sub>CC</sub> = 2.5V T<sub>A</sub> = 25°C
2. Typical values are not 100% tested

**CAPACITANCE**

(Temp = 25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance (Add, /CS1,CS2,/LB,/UB, /WE, /OE)	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance (I/O)	V <sub>I/O</sub> = 0V	10	pF

Note : These parameters are sampled and not 100% tested

### AC CHARACTERISTICS

T<sub>A</sub> = -40°C to 85°C, unless otherwise specified

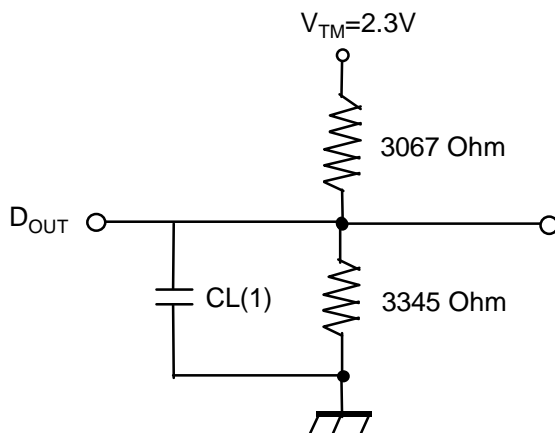
#	Symbol	Parameter	70ns		85ns		Unit
			Min.	Max.	Min.	Max.	
READ CYCLE							
1	t <sub>RC</sub>	Read Cycle Time	70	-	85	-	ns
2	t <sub>AA</sub>	Address Access Time	-	70	-	85	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	70	-	85	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	35	-	40	ns
5	t <sub>BA</sub>	/LB, /UB Access Time	-	70	-	85	ns
6	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	ns
7	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	ns
8	t <sub>BLZ</sub>	/LB, /UB Enable to Output in Low Z	10	-	10	-	ns
9	t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	30	0	30	ns
10	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	30	0	30	ns
11	t <sub>BHZ</sub>	/LB, /UB Disable to Output in High Z	0	30	0	30	ns
12	t <sub>OH</sub>	Output Hold from Address Change	10	-	10	-	ns
WRITE CYCLE							
13	t <sub>WC</sub>	Write Cycle Time	70	-	85	-	ns
14	t <sub>CW</sub>	Chip Selection to End of Write	60	-	70	-	ns
15	t <sub>AW</sub>	Address Valid to End of Write	60	-	70	-	ns
16	t <sub>BW</sub>	/LB, /UB Valid to End of Write	60	-	70	-	ns
17	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	ns
18	t <sub>WP</sub>	Write Pulse Width	50	-	60	-	ns
19	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	ns
20	t <sub>WHZ</sub>	Write to Output in High Z	0	20	0	25	ns
21	t <sub>DW</sub>	Data to Write Time Overlap	30	-	35	-	ns
22	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	ns
23	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	ns

### AC TEST CONDITIONS

T<sub>A</sub> = -40°C to 85°C, unless otherwise specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.1V
Output Load	t <sub>CLZ</sub> , t <sub>OLZ</sub> , t <sub>BLZ</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>BHZ</sub> , t <sub>WHZ</sub> , t <sub>OW</sub>
	Others
	CL = 5pF + 1TTL Load
	CL = 30pF + 1TTL Load

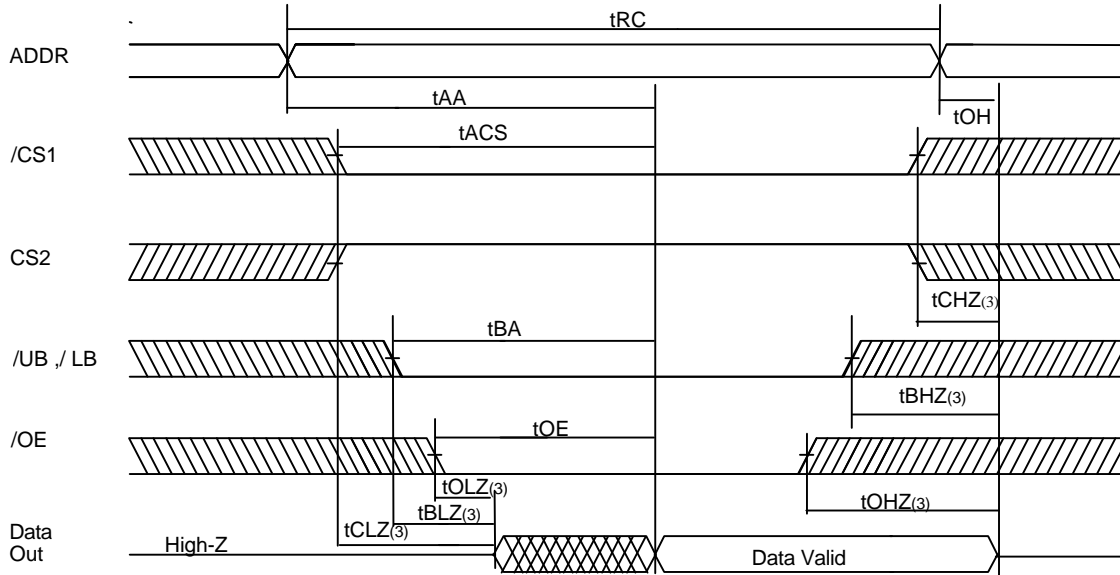
### AC TEST LOADS



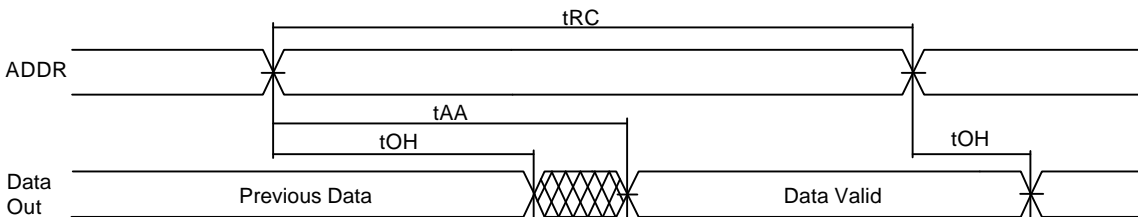
Note 1. Including jig and scope capacitance:

**TIMING DIAGRAM**

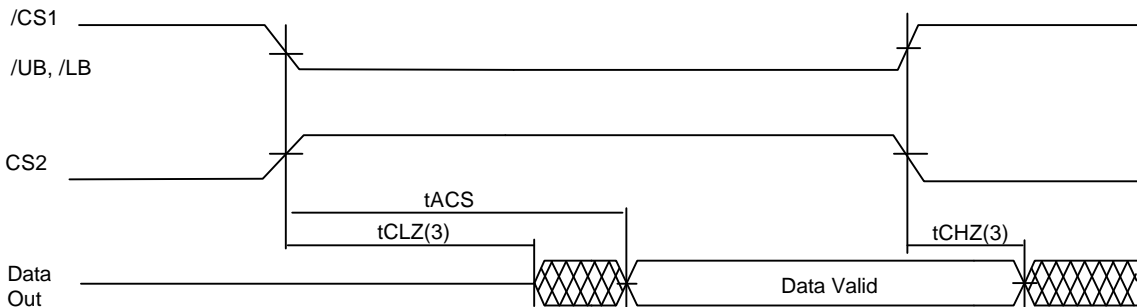
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 1,2,4)



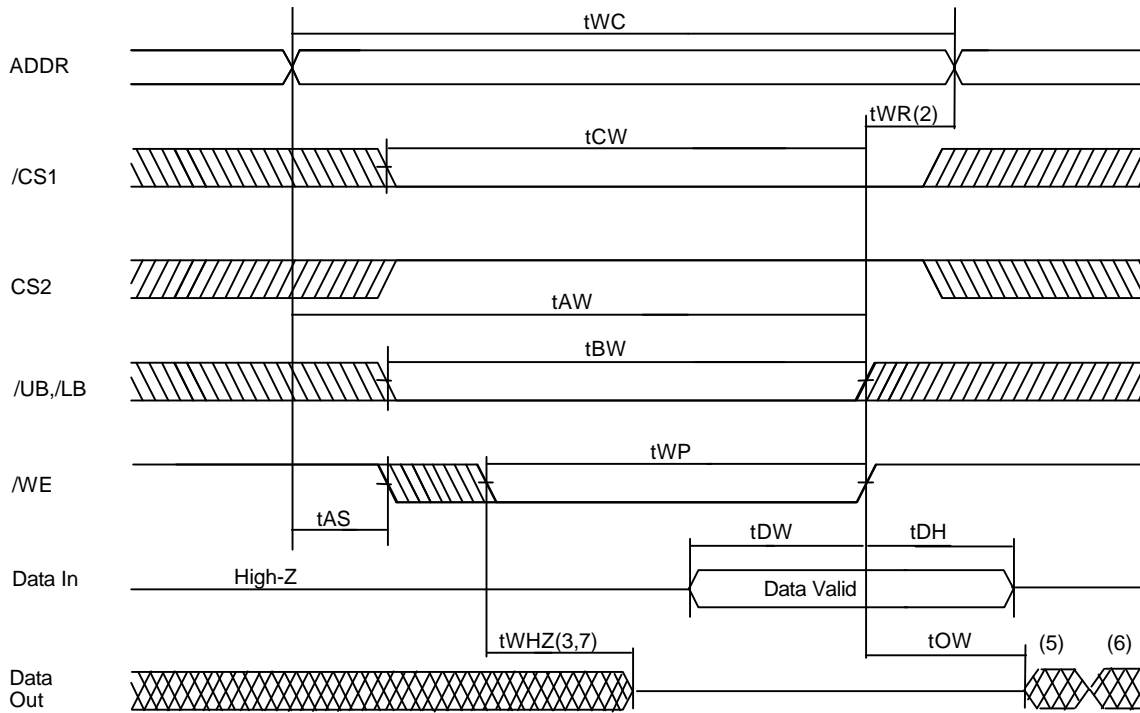
READ CYCLE 3(Note 1,2,4)



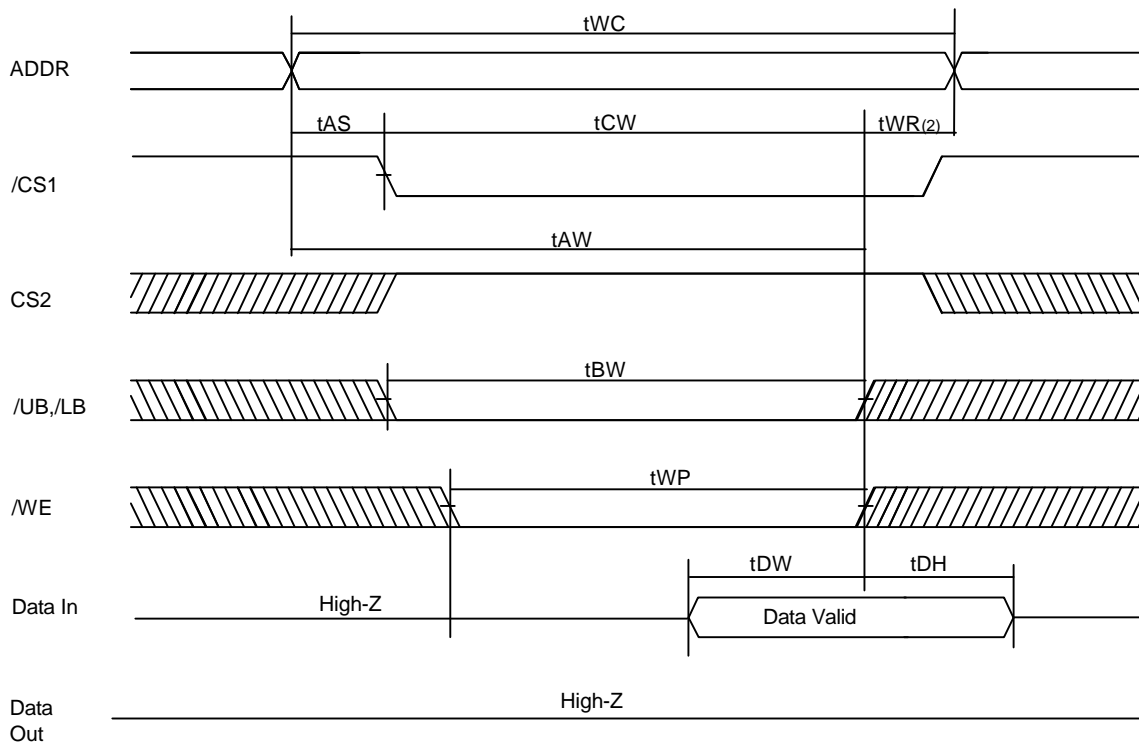
Notes:

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /UB and/or /LB and /CS1 and CS2 are in active status.
2. /OE = V<sub>IL</sub>
3. Transition is measured ± 200mV from steady state voltage. This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active. /UB and /LB in high for the standby, low for active

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,8) (/CS1, CS2 Controlled)



**Notes:**

1. A write occurs during the overlap of a low /WE, a low /CS1, a high CS2 and a low /UB and/or /LB .
2. tWR is measured from the earlier of /CS1, /LB, /UB, or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, /LB and /UB low transition and CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured  $\pm 200\text{mV}$  from steady state.  
This parameter is sampled and not 100% tested.
8. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active.  
/UB and /LB in high for the standby, low for active.

**DATA RETENTION ELECTRIC CHARACTERISTIC**
 $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ 

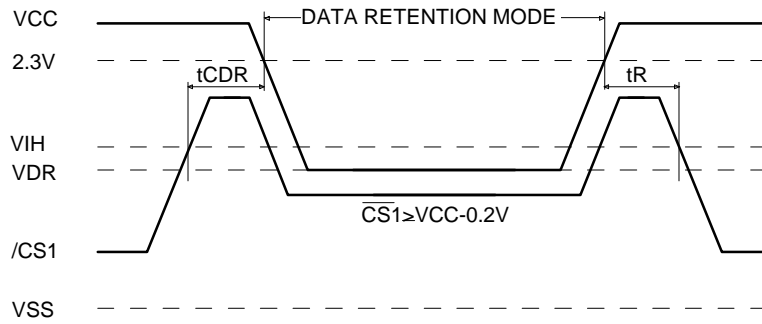
Symbol	Parameter	Test Condition	Min	Typ <sup>1</sup>	Max	Unit	
VDR	Vcc for Data Retention	/CS1 $\geq V_{cc} - 0.2\text{V}$ or CS2 $\leq V_{ss} + 0.2\text{V}$ or /UB, /LB $\geq V_{cc} - 0.2\text{V}$ , VIN $\geq V_{cc} - 0.2\text{V}$ or VIN $\leq V_{ss} + 0.2\text{V}$	1.5	-	2.7	V	
Iccdr	Data Retention Current	Vcc=1.5V, /CS1 $\geq V_{cc} - 0.2\text{V}$ or CS2 $\leq V_{ss} + 0.2\text{V}$ or /UB, /LB $\geq V_{cc} - 0.2\text{V}$ VIN $\geq V_{cc} - 0.2\text{V}$ or VIN $\leq V_{ss} + 0.2\text{V}$	SL	-	0.2	6	$\mu\text{A}$
			LL	-	0.2	12	$\mu\text{A}$
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns	
tR	Operating Recovery Time		tRC	-	-	ns	

**Notes:**

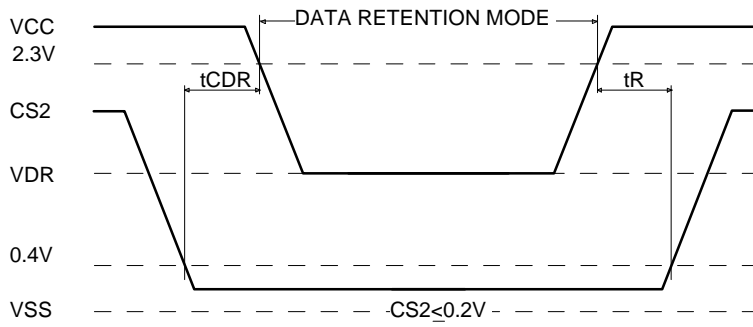
1. Typical values are under the condition of  $T_A = 25^\circ\text{C}$ .
2. Typical Value are sampled and not 100% tested



**DATA RETENTION TIMING DIAGRAM 1**

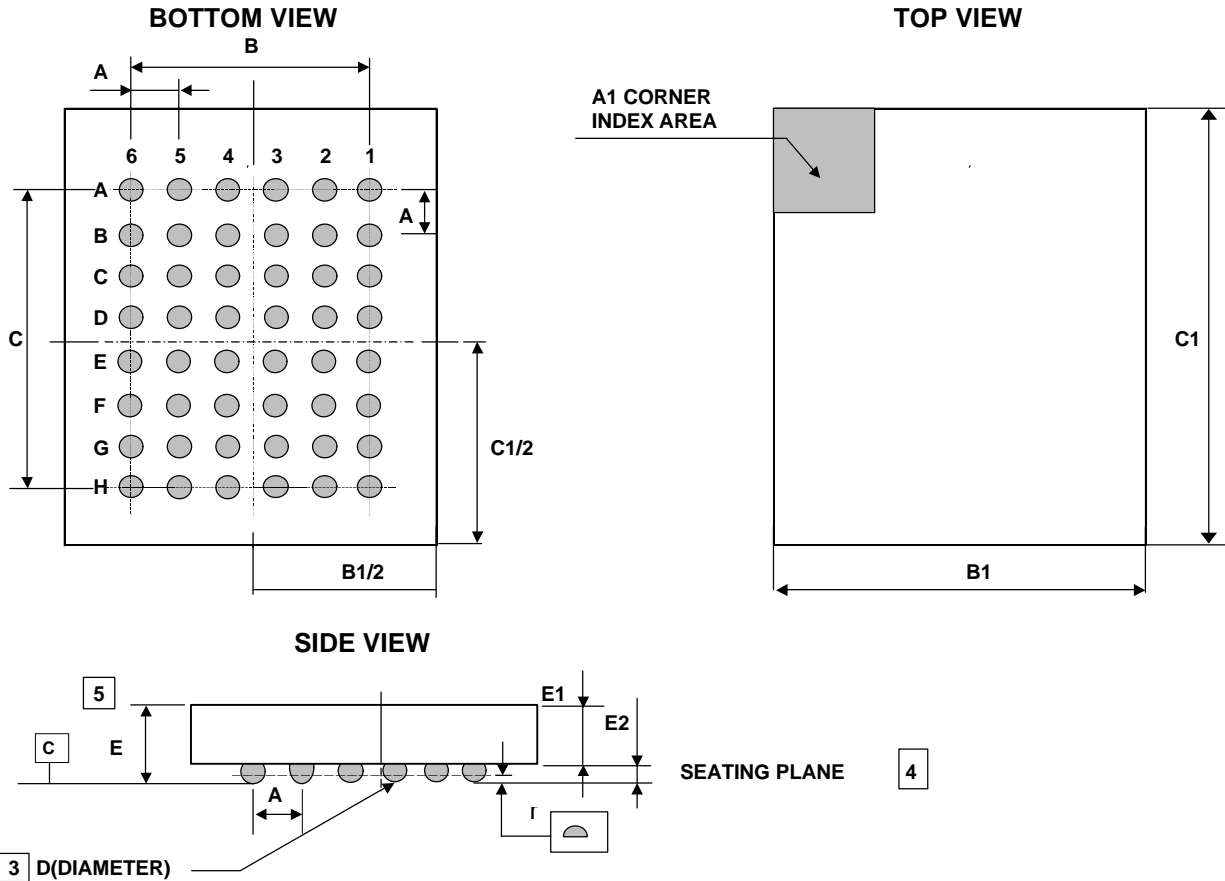


**DATA RETENTION TIMING DIAGRAM 2**



**PACKAGE INFORMATION**

48ball Fine Pitch Ball Grid Array Package (F)

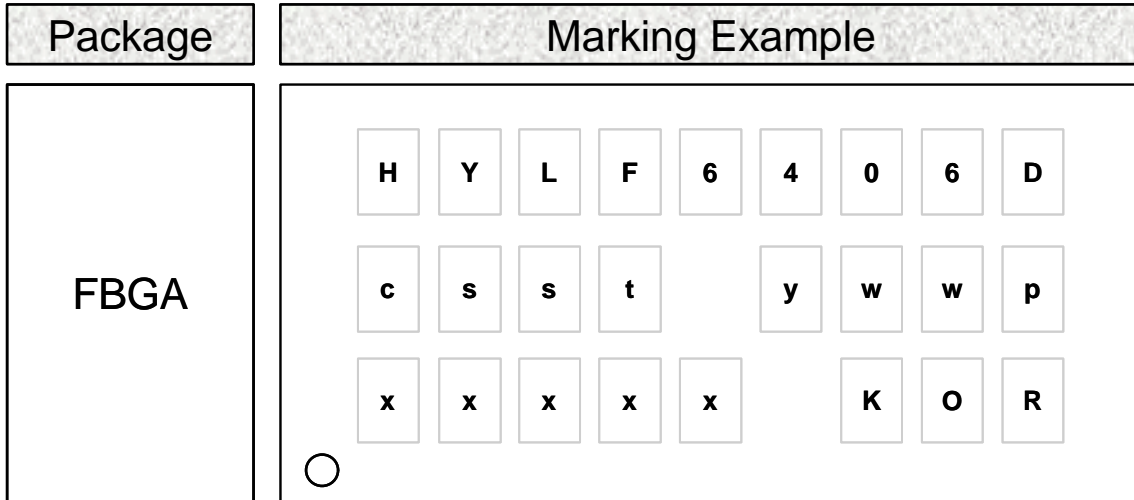


Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1	5.9	6.0	6.1
C	-	5.25	-
C1	7.9	8.0	8.1
D	0.3	0.35	0.4
E	0.9	1.0	1.10
E1	-	0.75	-
E2	0.20	0.25	0.30
r	-	-	0.08

**Note**

1. DIMENSIONING AND TOLERANCING PER ASME Y14. 5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION "D" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

MARKING INFORMATION



Index

• <b>HYQF6406D</b>	: Part Name
• <b>c</b>	: Power Consumption
	- D : Low Low Power
	- S : Super Low Power
• <b>ss</b>	: Speed
	- 70 : 70ns
	- 85 : 85ns
• <b>t</b>	: Temperature
	- I : Industrial ( -40 ~ 85 °C )
• <b>y</b>	: Year ( ex : 0 = year 2000, 1= year 2001 )
• <b>ww</b>	: Work Week ( ex : 12 = work week 12 )
• <b>p</b>	: Process Code
• <b>xxxxx</b>	: Lot No.
• <b>KOR</b>	: Origin Country
<b>Note</b>	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item