# 512Mb DDR2 SDRAM
## HY5PS12421(L)F
## HY5PS12821(L)F
## HY5PS121621(L)F

## REVISION HISTORY

| Rev. No. | Rev. Date | Page of Rev. | Description of Change |
|---|---|---|---|
| 0.2 | Jun.2002 | page3 | added tCK on the operating frequency table |
| 0.3 | July.2002 | All | Changed master page |
| 0.4 | Aug.2002 | All | corrected typos and change some descriptions |
| 0.5 | Aug.2002 | All | corrected typos and wrong definiotions and changed some items |
| 0.51 | Oct.2002 | Page7,52 | page7:modify Package Dimension, page52 change TA to TC, etc. |
| 0.52 | Nov.2002 | | corrected typos, Add x16 part and update Package dimensions |
| 0.53 | Dec.2002 | Page1,6,7,29 | corrected typos and delete page29 tRAS programming definition |
| 0.6 | Apr.2003 | Page9,10 | Changed Package dimensions<br>Changed Part Number<br>Added 667 Speed bin |

## KEY FEATURES

**Preliminary**

- VDD = 1.8V, 2.5V (Optional)
- VDDQ = 1.8V +/- 0.1V
- All inputs and outputs are compatible with SSTL_18 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS, $\overline{DQS}$)
- Differential Data Strobe (DQS, $\overline{DQS}$)
- Data outputs on DQS, $\overline{DQS}$ edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ, $\overline{DQS}$ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 3, 4 and 5 supported
- Programmable Additive latency 0, 1, 2, 3, 4 and 5 supported
- Programmable burst length 4 / 8 with both nibble sequential and interleave mode
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- Programmable tRAS supported
- 8K refresh cycles / 64ms
- JEDEC standard 60ball FBGA(x4/x8) & 84bal FBGA(x16)l
- Full strength driver option controlled by EMRS
- On Die Termination supported
- Off Chip Driver Impedance Adjustment supported
- Read Data Strobe supported (x8 only)

## ORDERING INFORMATION

| Part No. | Configuration | Package |
|---|---|---|
| HY5PS12421(L)F-X* | 128Mx4 | 60 Ball FBGA |
| HY5PS12821(L)F-X* | 64Mx8 | |
| HY5PS121621(L)F -X* | 32Mx16 | 84Ball FBGA |

* X means speed grade

## OPERATING FREQUENCY

| Grade | tCK(ns) | CL | tRCD | tRP | Unit |
|---|---|---|---|---|---|
| -E3 | 5 | 3 | 3 | 3 | Clk |
| -E4 | 5 | 4 | 4 | 4 | Clk |
| -C4 | 3.75 | 4 | 4 | 4 | Clk |
| -C5 | 3.75 | 5 | 5 | 5 | Clk |
| -Y5 | 3 | 5 | 5 | 5 | Clk |
| -Y6 | 3 | 6 | 6 | 6 | Clk |

## 128Mx4 DDR2 PIN CONFIGURATION

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NC | VSS | A | VSSQ | $\overline{DQS}$ | VDDQ |
| NC | VSSQ | DM | B | DQS | VSSQ | NC |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| NC | VSSQ | DQ3 | D | DQ2 | VSSQ | NC |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{WE}$ | F | $\overline{RAS}$ | $\overline{CK}$ | ODT |
| BA2,NC | BA0 | BA1 | G | $\overline{CAS}$ | $\overline{CS}$ | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

## ROW AND COLUMN ADDRESS TABLE

| ITEMS | 128Mx4 |
|---|---|
| **Organization** | 32M x 4 x 4banks |
| **Row Address** | A0 - A13 |
| **Column Address** | A0-A9, A11 |
| **Bank Address** | BA0, BA1 |
| **Auto Precharge Flag** | A10 |
| **Refresh** | 8K |

## 64Mx8 DDR2 PIN CONFIGURATION

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NU, $\overline{RDQS}$ | VSS | A | VSSQ | $\overline{DQS}$ | VDDQ |
| DQ6 | VSSQ | DM, RDQS | B | DQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | D | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{WE}$ | F | $\overline{RAS}$ | $\overline{CK}$ | ODT |
| BA2,NC | BA0 | BA1 | G | $\overline{CAS}$ | $\overline{CS}$ | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

## ROW AND COLUMN ADDRESS TABLE

| ITEMS | 64Mx8 |
|---|---|
| **Organization** | 16M x 8 x 4banks |
| **Row Address** | A0 - A13 |
| **Column Address** | A0-A9 |
| **Bank Address** | BA0, BA1 |
| **Auto Precharge Flag** | A10 |
| **Refresh** | 8K |

## 32Mx16 DDR2 PIN CONFIGURATION

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NC | VSS | A | VSSQ | $\overline{\text{UDQS}}$ | VDDQ |
| DQ14 | VSSQ | UDM | B | UDQS | VSSQ | DQ15 |
| VDDQ | DQ9 | VDDQ | C | VDDQ | DQ8 | VDDQ |
| DQ12 | VSSQ | DQ11 | D | DQ10 | VSSQ | DQ13 |
| VDD | NC | VSS | A | VSSQ | $\overline{\text{LDQS}}$ | VDDQ |
| DQ6 | VSSQ | LDM | B | LDQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | D | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{\text{WE}}$ | F | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$ | ODT |
| BA2,NC | BA0 | BA1 | G | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$ | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

## ROW AND COLUMN ADDRESS TABLE

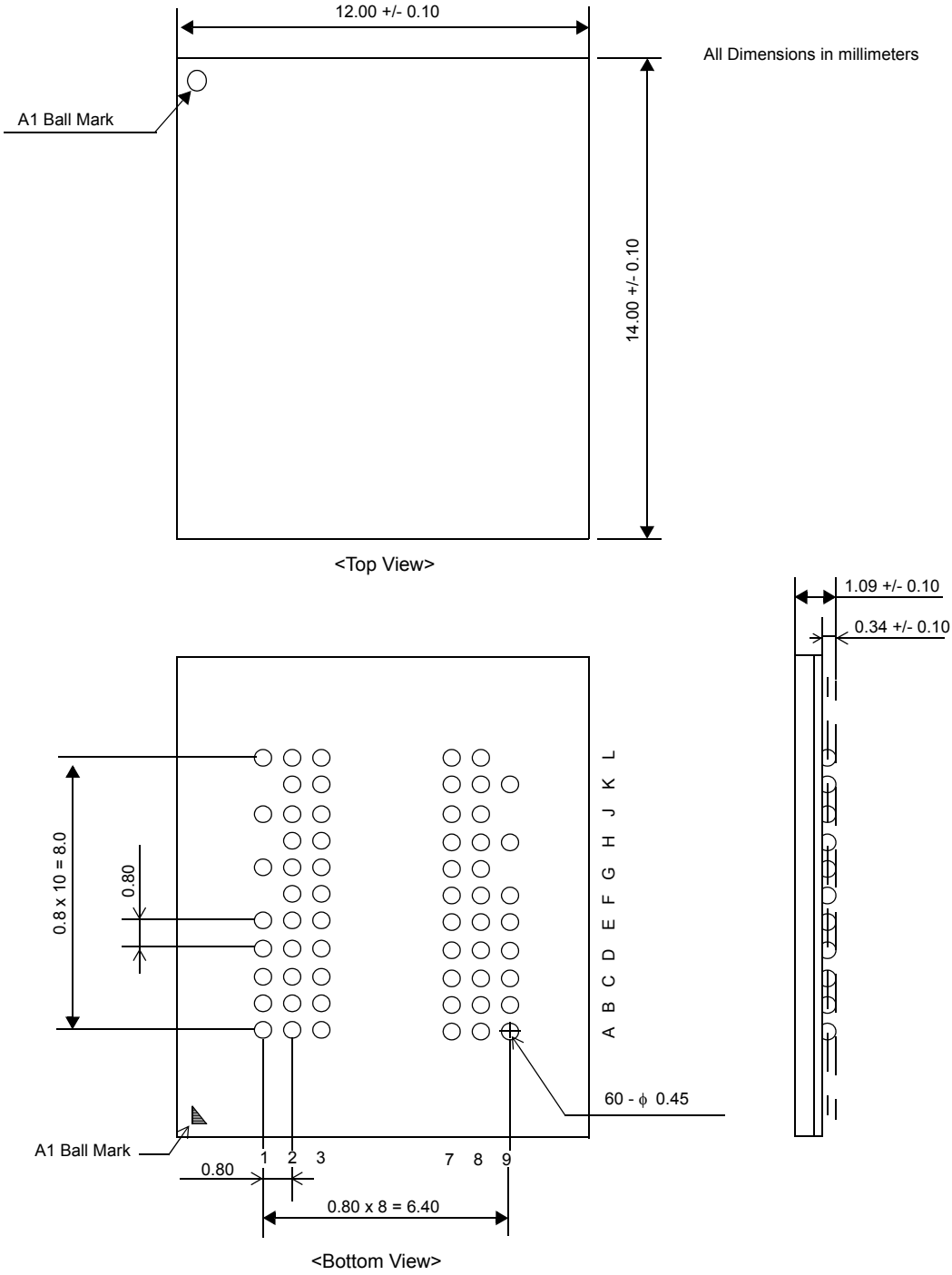
| ITEMS | 32Mx16 |
|---|---|
| **Organization** | 8M x 16 x 4banks |
| **Row Address** | A0 - A12 |
| **Column Address** | A0-A9 |
| **Bank Address** | BA0, BA1 |
| **Auto Precharge Flag** | A10 |
| **Refresh** | 8K |

## PIN DESCRIPTION

| PIN | TYPE | DESCRIPTION |
|---|---|---|
| CK, $\overline{CK}$ | Input | Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing). |
| CKE | Input | Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_18 input, but will detect an LVCMOS LOW level after Vdd is applied. |
| $\overline{CS}$ | Input | Chip Select : Enables or disables all inputs except CK, $\overline{CK}$, CKE, DQS and DM. All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. |
| BA0, BA1 | Input | Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied. |
| A0 ~ A13 | Input | Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered. |
| ODT | Input | On Die Termination Control : ODT enables on die termination resistance internal to the DDR2 SDRAM. When enabled, on die termination is only applied to DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM. |
| DM, RDQS<br>NC, $\overline{RDQS}$<br>(LDM, UDM) | Input | Input Data Mask : DM is an input mask signal for write data. Input Data is masked when DM is sampled High along with that input data during a WRITE access. DM is sampled on both edges of DQS, Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-7; UDM corresponds to the data on DQ8-15.<br>Read Data Strobe for x8 Device : DM signal is muxed with RDQS. When read data strobe option is enabled by EMRS, this muxed pin is used for read data strobe. |
| DQS, $\overline{DQS}$ | I/O | Differential Data Strobe Pair : Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. Strobe options - Differential or single ended is selected by EMRS. For the x16, LDQS corresponds to the data on DQ0-7; UDQS corresponds to the data on DQ8-15. |
| DQ | I/O | Data input / output pin : Data bus |
| $V_{DD}/V_{SS}$ | Supply | Power supply for internal circuits and input buffers. |
| $V_{DDQ}/V_{SSQ}$ | Supply | Power supply for output buffers for noise immunity. |
| VDDL/VSSDL | Supply | Power supply for DLL circuits |
| $V_{REF}$ | Supply | Reference voltage for inputs for SSTL interface. |
| NC | NC | No connection. |

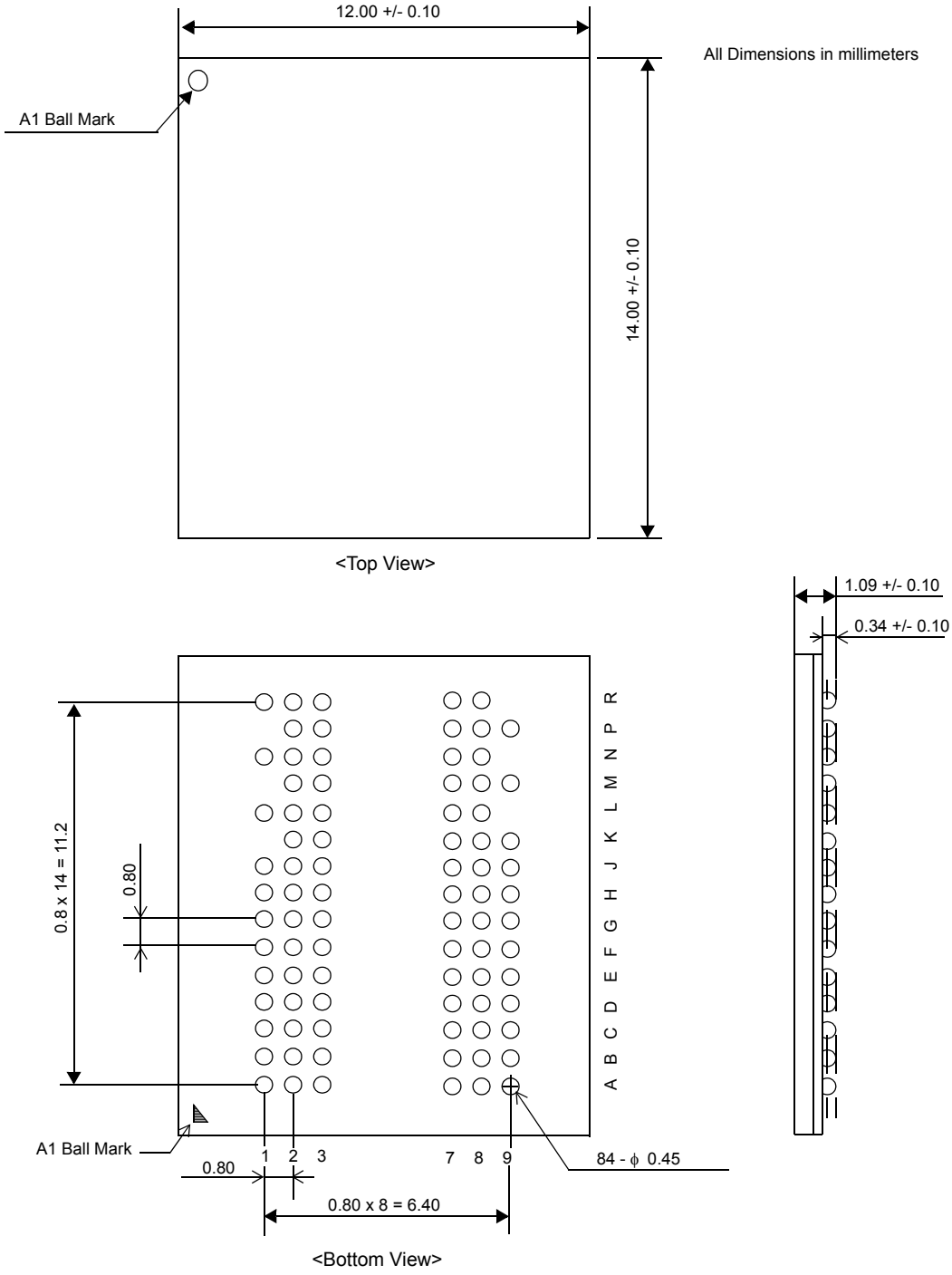
## PACKAGE Dimension (x4/x8)

### 60Ball Fine Pitch Ball Grid Array Outline



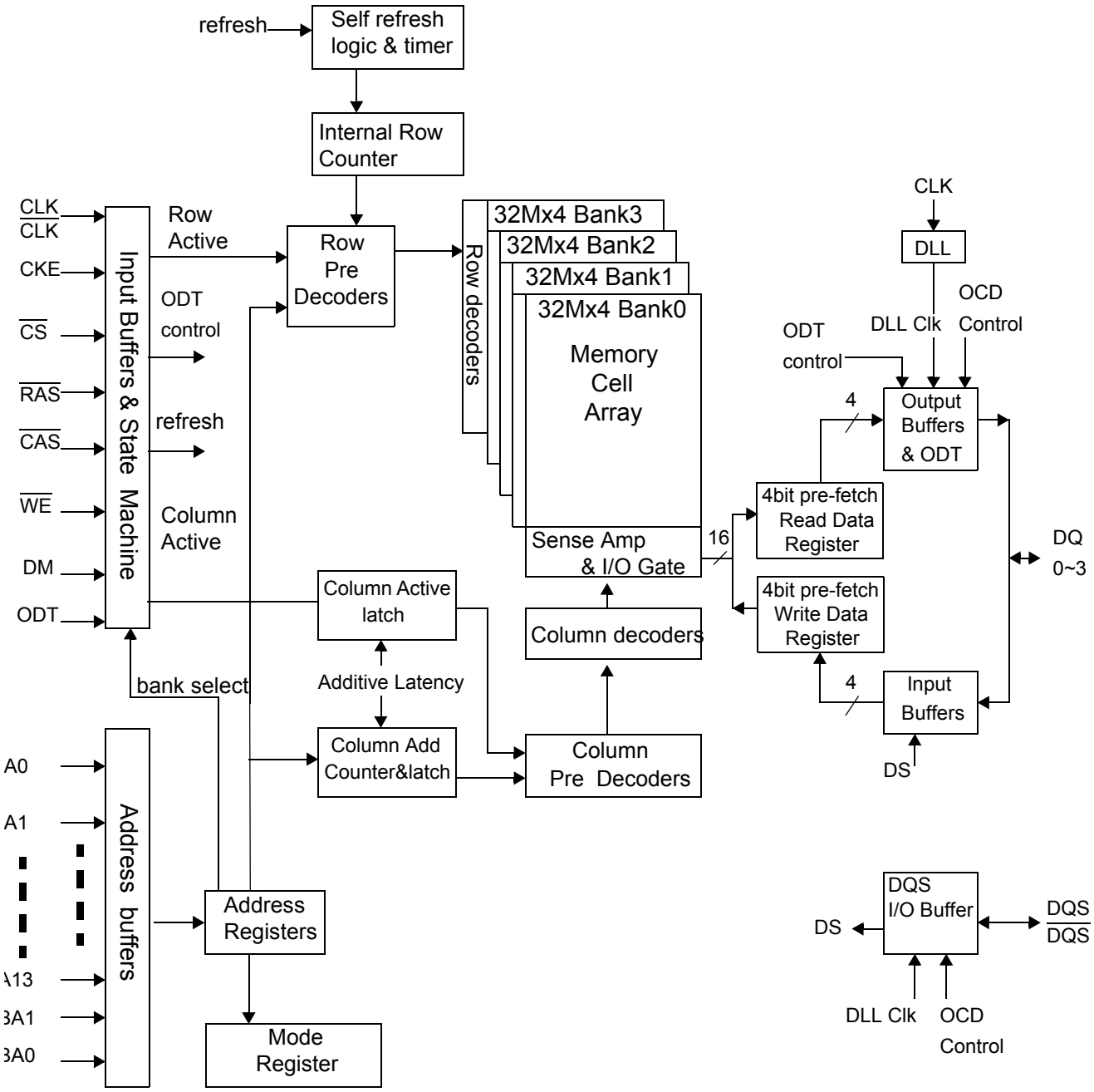
## PACKAGE Dimension (x16)

### 84Ball Fine Pitch Ball Grid Array Outline



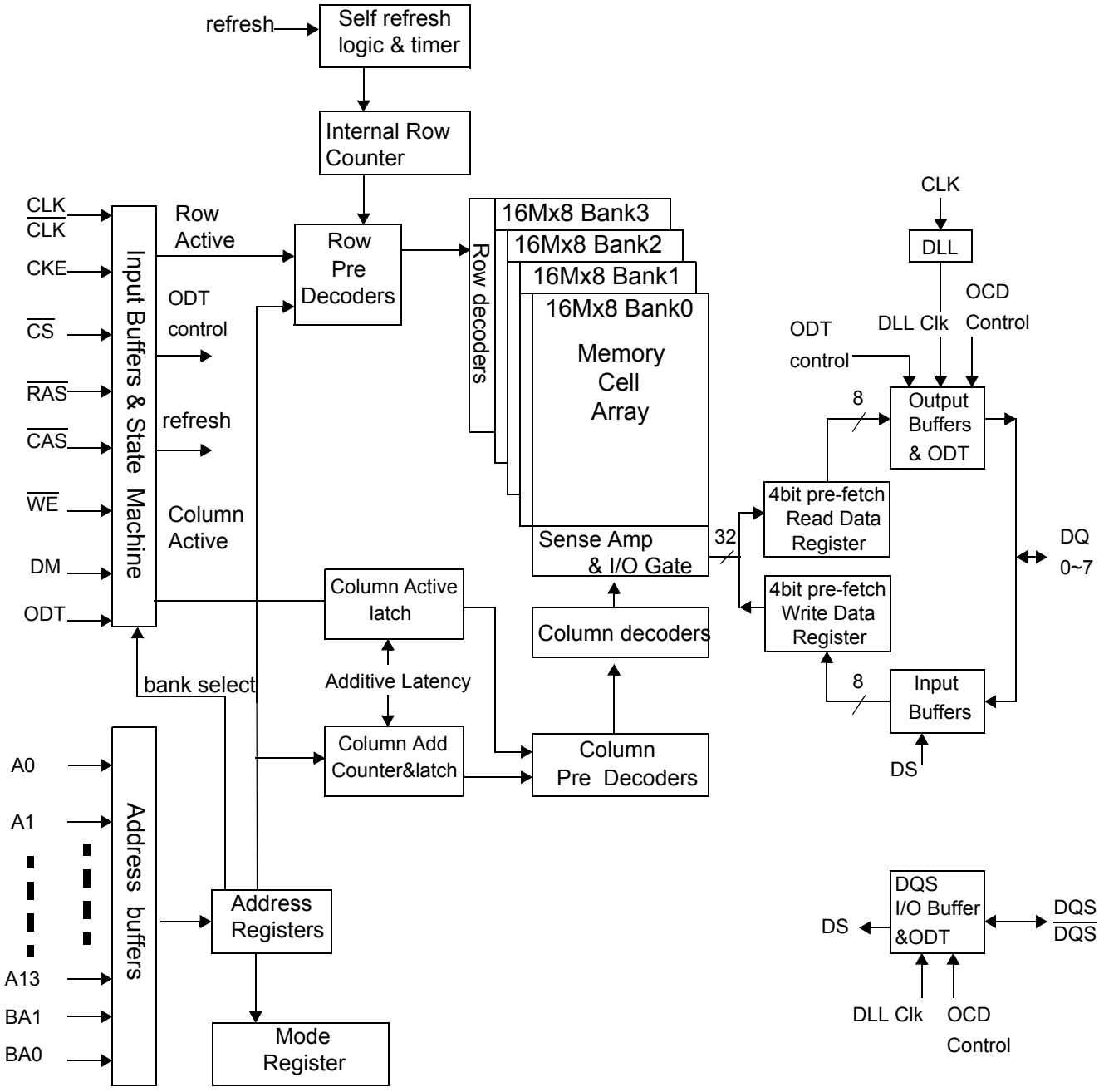
## FUNCTIONAL BLOCK DIAGRAM (128Mx4)

4Banks x 32Mbit x 4 I/O DDR2 SDRAM



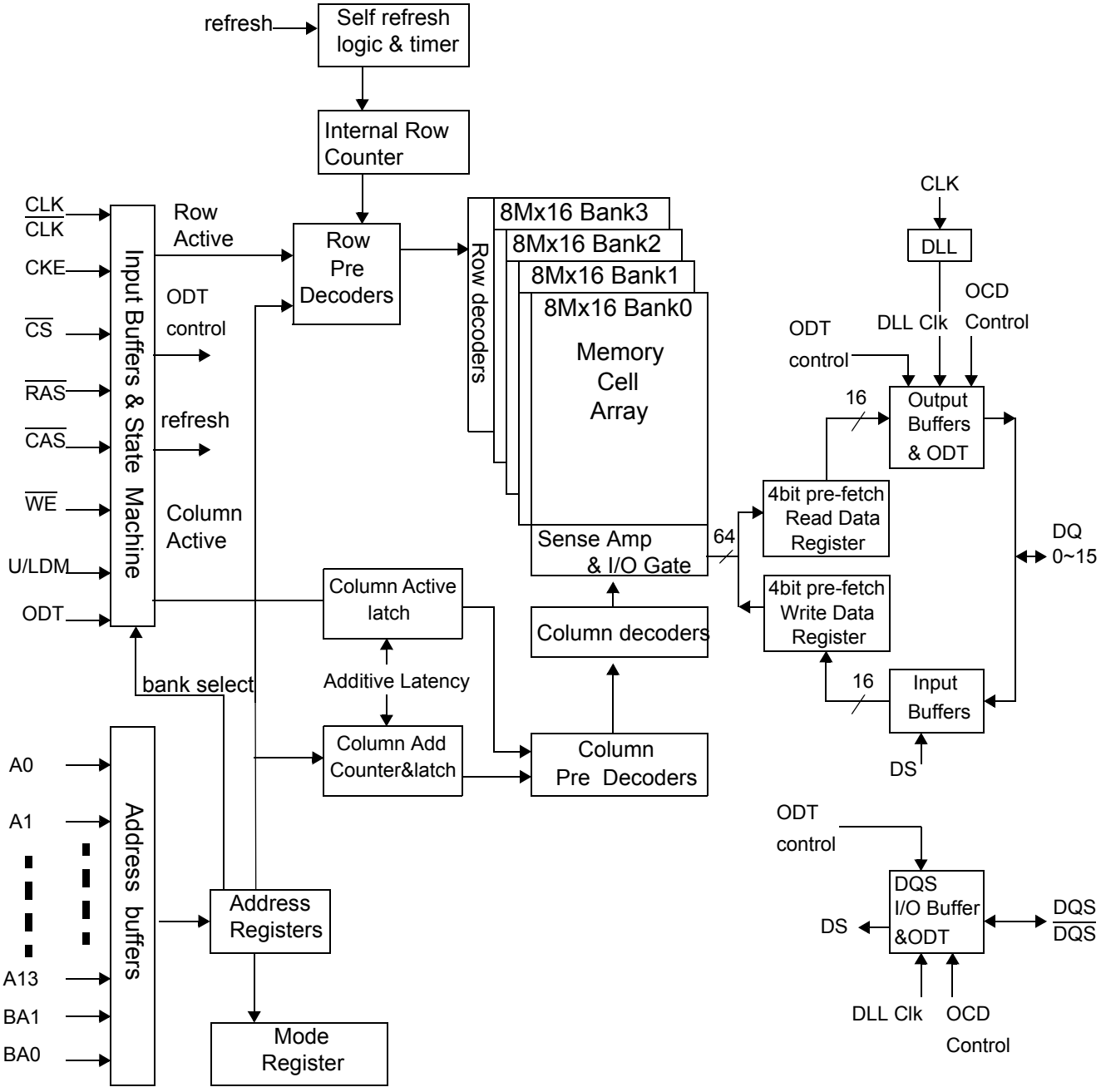
## FUNCTIONAL BLOCK DIAGRAM (64Mx8)

4Banks x 16Mbit x 8 I/O DDR2 SDRAM



## FUNCTIONAL BLOCK DIAGRAM (32Mx16)

4Banks x 8Mbit x 16 I/O DDR2 SDRAM



## SIMPLIFIED COMMAND TRUTH TABLE

| Command | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDR | A10/AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Extended Mode Register Set | | H | H | L | L | L | L | OP code | | | 1,2 |
| Mode Register Set | | H | H | L | L | L | L | OP code | | | 1,2 |
| Device Deselect | | H | X | H | X | X | X | X | | | 1 |
| No Operation | | | | L | H | H | H | | | | |
| Bank Active | | H | H | L | L | H | H | RA | | V | 1 |
| Read | | H | H | L | H | L | H | CA | L | V | 1 |
| Read with Autoprecharge | | | | | | | | | H | | 1,3 |
| Write | | H | H | L | H | L | L | CA | L | V | 1 |
| Write with Autoprecharge | | | | | | | | | H | | 1,4 |
| Precharge All Banks | | H | H | L | L | H | L | X | H | X | 1,5 |
| Precharge selected Bank | | | | | | | | | L | V | 1 |
| Auto Refresh | | H | H | L | L | L | H | X | | | 1 |
| Self Refresh | Entry | H | L | L | L | L | H | X | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | |
| Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | 1 |

( H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation )

**Note :**

1. All DDR2 commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Registers.
3. Burst reads or writes at BL=4 cannot be terminated. See sections "Reads interrupted by a Read" and "Write interrupted by a Write" in 3.2.4 for details.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See Section
6. "X" means "H or L(but a defined logic level)".

## Clock Enable (CKE) TRUTH TABLE for Synchronous Transitions

| Current State[2] | CKE | | Command (N)[3] RAS, CAS, WE, CS | Action (N)[3] | Notes |
|---|---|---|---|---|---|
| | Previous Cycle[1] (N-1) | Current Cycle[1] (N) | | | |
| Power Down | L | L | x | Maintain Power-Down | 13, 15 |
| | L | H | DESELECT or NOP | Power Down Exit | 4, 8 |
| Self Refresh | L | L | x | Maintain Self Refresh | 15 |
| | L | H | DESELECT or NOP | Self Refresh Exit | 4, 5, 9 |
| Bank(s) Active | H | L | DESELECT or NOP | Active Power Down Entry | 4, 8, 10, 11 |
| All Banks Idle | H | L | DESELECT or NOP | Precharge Power Down Entry | 4, 8, 10 |
| | H | L | AUTOREFRESH | Self Refresh Entry | 6, 9, 11 |
| Any other state | H | H | Refer to the Command Truth Table | | 7 |

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitely described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the $t_{XSNR}$ period. Read commands may be issued only after $t_{XSRD}$ (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Entry and Exit are NOP and DESELECT only.
10. Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge or Refresh operations are in progress. See section 2.2.9 "Power Down" and 2.2.8 "Self Refresh Command" for a detailed list of restrictions.
11. Minimum CKE high time is tbd.; minimum CKE low time is tbd. (subject to separate ballot)
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section ?(will be defined)
14. CKE must be maintained high while the SDRAM is in OCD calibration mode i.e. if any of the bits A7, A8, A9 in EMRS(1) are set to "1".
15. “X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT fucntion is enabled (Bit A2 or A6 set to “1” in EMRS(1) ).

## WRITE MASK TRUTH TABLE

| Function | CKEn-1 | CKEn | $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | DM | ADDR | A10/AP | BA | Note |
|---|---|---|---|---|---|---|---|---|
| Data Write | H | X | X | L | X | | | 1 |
| Data-In Mask | H | X | X | H | X | | | 1 |

**Note :**

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strobes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

## OPERATION COMMAND TRUTH TABLE-I

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| IDLE | H | X | X | X | X | DSEL | NOP or power down[3] |
| | L | H | H | H | X | NOP | NOP or power down[3] |
| | L | H | H | L | X | NOP | NOP or power down[3] |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[4] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[4] |
| | L | L | H | H | BA, RA | ACT | Row Activation |
| | L | L | H | L | BA, AP | PRE/PALL | NOP |
| | L | L | L | H | X | AREF/SREF | Auto Refresh or Self Refresh[5] |
| | L | L | L | L | OPCODE | MRS | Mode Register Set |
| ROW ACTIVE | H | X | X | X | X | DSEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | NOP | NOP |
| | L | H | L | H | BA, CA, AP | READ/READAP | Begin read : optional AP[6] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | Begin write : optional AP[6] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4] |
| | L | L | H | L | BA, AP | PRE/PALL | Precharge[7] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| READ | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | NOP | Continue burst to end |
| | L | H | L | H | BA, CA, AP | READ/READAP | Term burst, new read:optional AP[8] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4] |
| | L | L | H | L | BA, AP | PRE/PALL | Term burst, precharge |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| WRITE | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | NOP | Continue burst to end |
| | L | H | L | H | BA, CA, AP | READ/READAP | Term burst, new read:optional AP[8] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | Term burst, new write:optional AP |

## OPERATION COMMAND TRUTH TABLE-II

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| WRITE | L | L | H | H | BA, RA | ACT | ILLEGAL[4] |
| | L | L | H | L | BA, AP | PRE/PALL | Term burst, precharge |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| READ WITH AUTOPRE-CHARGE | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | NOP | Continue burst to end |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[10] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[4,10] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| WRITE AUTOPRE-CHARGE | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | NOP | Continue burst to end |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[10] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[4,10] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| PRE-CHARGE | H | X | X | X | X | DSEL | NOP-Enter IDLE after tRP |
| | L | H | H | H | X | NOP | NOP-Enter IDLE after tRP |
| | L | H | H | L | X | NOP | NOP-Enter IDLE after tRP |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[4,10] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[4,10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, AP | PRE/PALL | NOP-Enter IDLE after tRP |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |

## OPERATION COMMAND TRUTH TABLE-III

| Current State | CS | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| ROW ACTIVATING | H | X | X | X | X | DSEL | NOP - Enter ROW ACT after tRCD |
| | L | H | H | H | X | NOP | NOP - Enter ROW ACT after tRCD |
| | L | H | H | L | X | NOP | NOP - Enter ROW ACT after tRCD |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[4,10] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[4,10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,9,10] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[4,10] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| WRITE RECOVERING | H | X | X | X | X | DSEL | NOP - Enter ROW ACT after tWR |
| | L | H | H | H | X | NOP | NOP - Enter ROW ACT after tWR |
| | L | H | H | L | X | NOP | NOP - Enter ROW ACT after tWR |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[4,11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| WRITE RECOVERING WITH AUTOPRE-CHARGE | H | X | X | X | X | DSEL | NOP - Enter precharge after tDPL |
| | L | H | H | H | X | NOP | NOP - Enter precharge after tDPL |
| | L | H | H | L | X | NOP | NOP - Enter precharge after tDPL |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[4,8,10] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[4,10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[4,11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| REFRESHING | H | X | X | X | X | DSEL | NOP - Enter IDLE after tRC |
| | L | H | H | H | X | NOP | NOP - Enter IDLE after tRC |
| | L | H | H | L | X | NOP | NOP - Enter IDLE after tRC |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[11] |

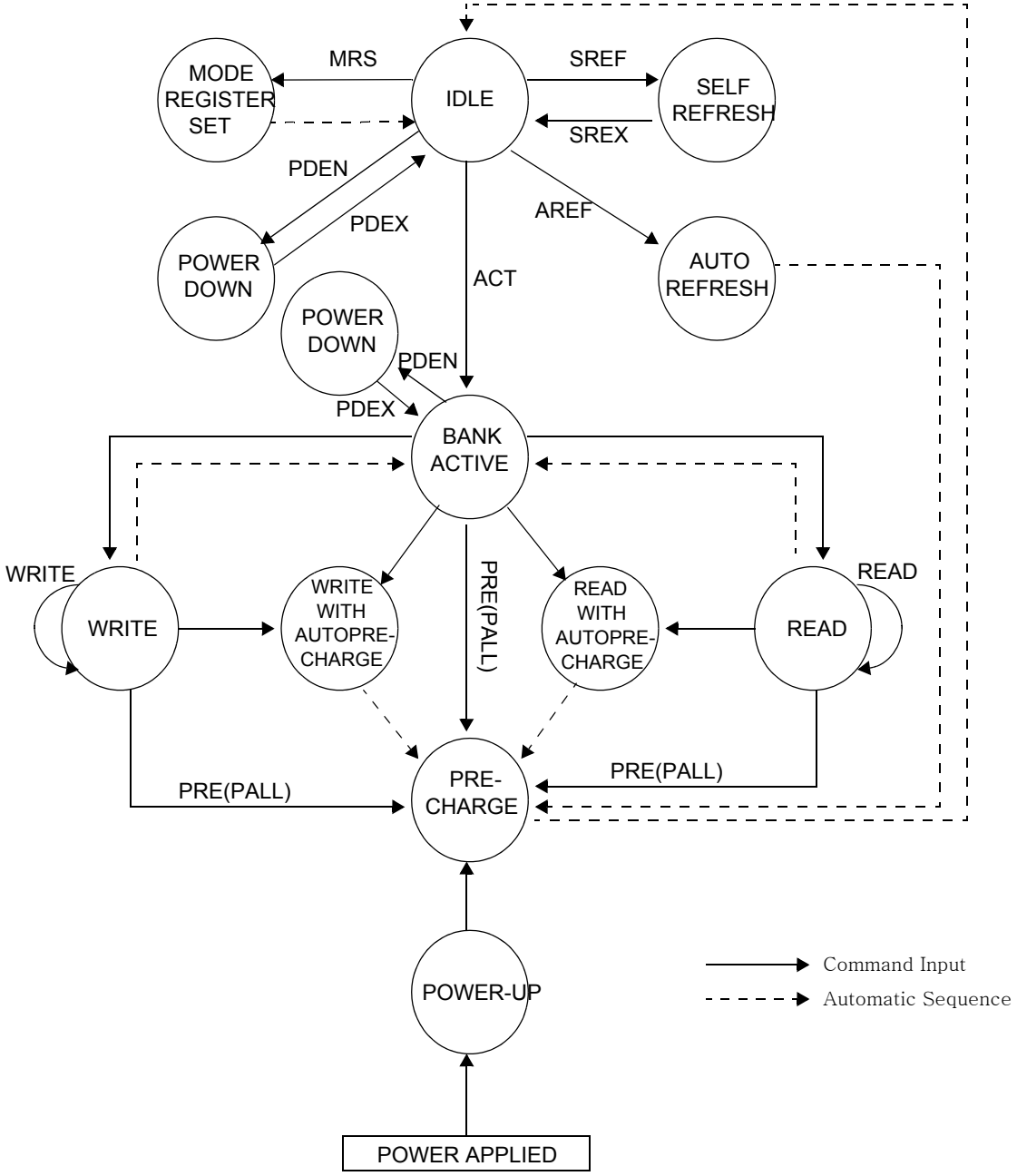
## OPERATION COMMAND TRUTH TABLE-IV

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| REFRESHING | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[11] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[11] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| MODE REGISTER ACCESSING | H | X | X | X | X | DSEL | NOP - Enter IDLE after tMRD |
| | L | H | H | H | X | NOP | NOP - Enter IDLE after tMRD |
| | L | H | H | L | X | NOP | NOP - Enter IDLE after tMRD |
| | L | H | L | H | BA, CA, AP | READ/READAP | ILLEGAL[11] |
| | L | H | L | L | BA, CA, AP | WRITE/WRITEAP | ILLEGAL[11] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[11] |
| | L | L | H | L | BA, AP | PRE/PALL | ILLEGAL[11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |

**Note :**

1. H - Logic High Level, L - Logic Low Level, X - Don't Care, V - Valid Data Input,
   BA - Bank Address, AP - AutoPrecharge Address, CA - Column Address, RA - Row Address, NOP - NO Operation.
2. All entries assume that CKE was active(high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive(low level), then in power down mode.
4. Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA) depending on the state of that bank.
5. If both banks are idle and CKE is inactive(low level), then self refresh mode.
6. Illegal if tRCD is not met.
7. Illegal if tRAS is not met.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Illegal if tRRD is not met.
10. Illegal for single bank, but legal for other banks in multi-bank devices.
11. Illegal for all banks.

## SIMPLIFIED STATE DIAGRAM



## POWER-UP SEQUENCE AND DEVICE INITIALIZATION

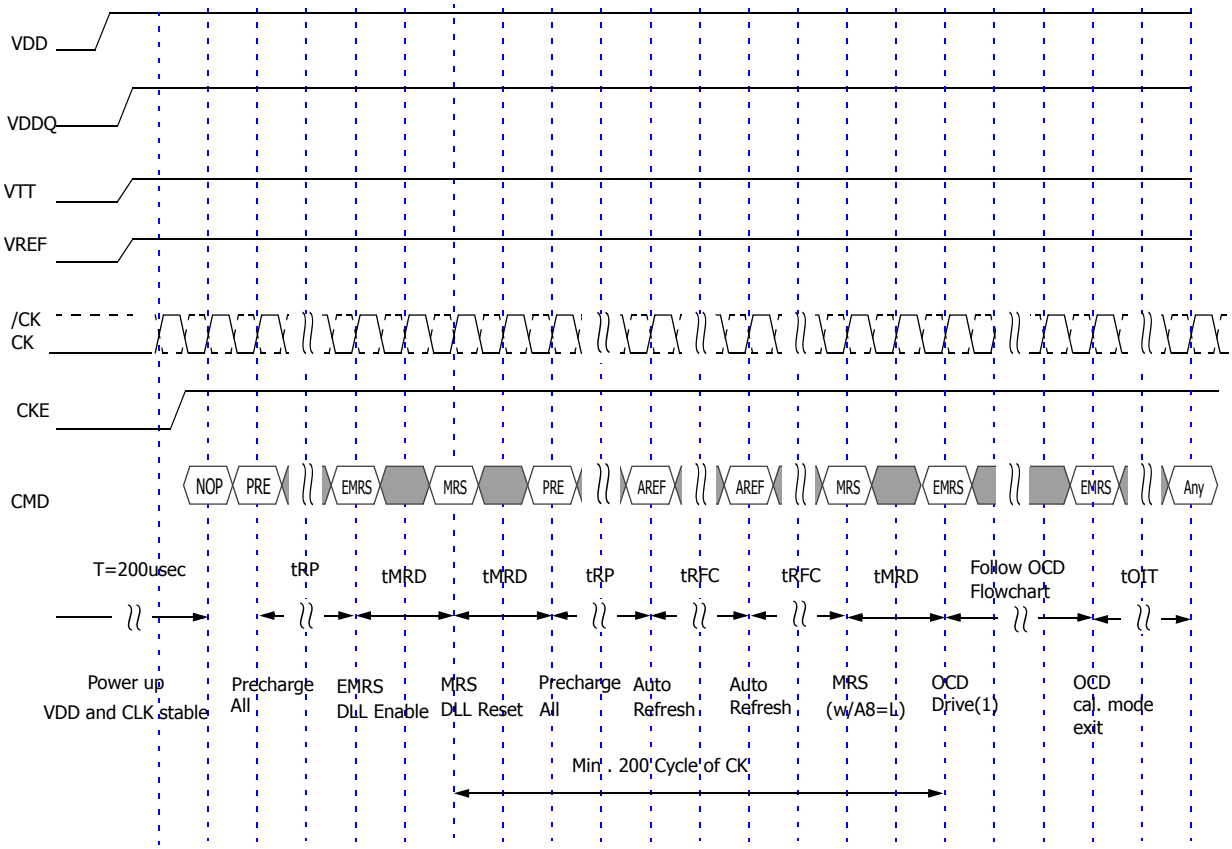
DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied any time after VDDQ, but is expected to be nominally coincident with VTT. The DQ and DQS outputs are in the High-Z state, where they remain until driven active in normal operation (by a read access). After all power supply, reference voltages, and the clocks are stable, the DDR2 SDRAM requires a 200us delay prior to applying an executable command. Once the 200us delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought HIGH. Following the NOP command, a Precharge ALL command must be applied. Next a Mode Register Set command must be issued for the Extended Mode Register, to enable the DLL. Then a Mode Register Set command must be issued for the Mode Register, to reset the DLL and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A Precharge ALL command should be applied, placing the device in the "all banks idle" state.
Once in the idle state, two Auto Refresh cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR2 SDRAM is ready for normal operation. Failure to follow these steps may lead to unpredictable start-up modes.

**Power-Up and Initialization Sequence**

The following sequence is required for POWER UP and Initialization.

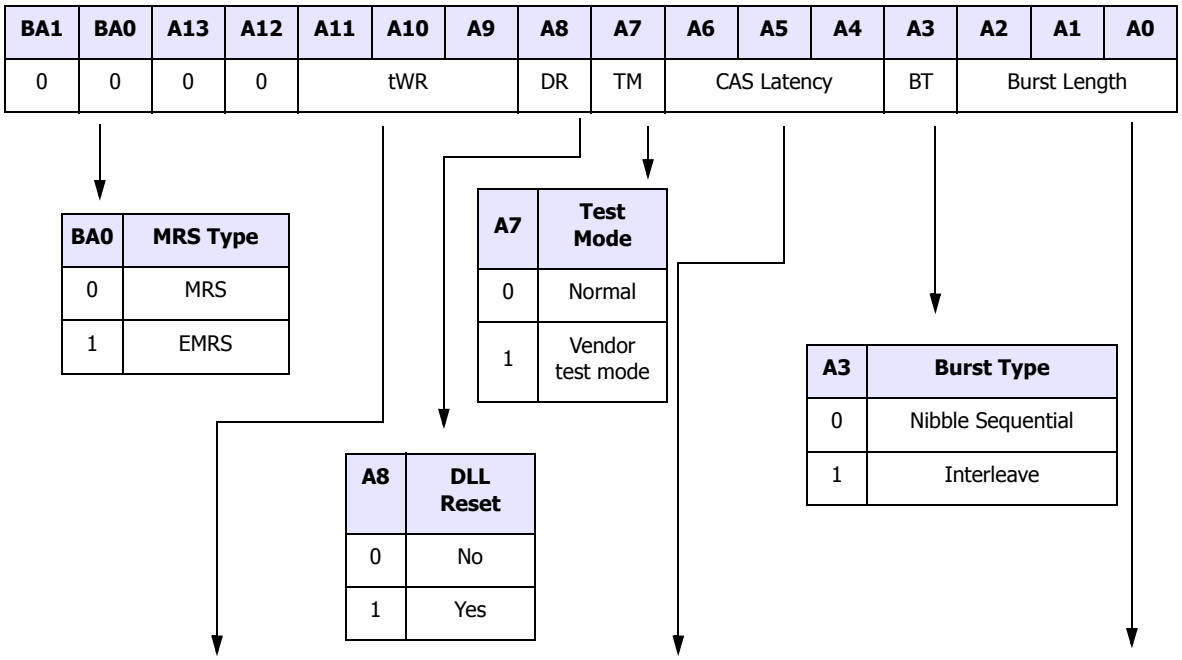
1. Apply power and attempt to maintain CKE and ODT at a low state (all other inputs may be undefined.)
- Apply VDD before or at the same time as VDDQ.
- Apply VDDQ before or at the same time as VTT & Vref.
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock(CK, CK), apply NOP & take CKE high.
4. Wait tRFC then issue precharge commands for all banks of the device.
5. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL.
(To issue DLL reset command, provide "High" to A8 and "Low" to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command with low to A8 to initialize device operation.
10. Carry out OCD (Off Chip Driver impedance adjustment). At Least, EMRS OCD Default command (A9=A8=A7=1) must be issued.

**Power-Up and Initialization Sequence Timing Diagram**



## MODE REGISTER SET (MRS)

The mode register is used to store the various operating modes such as CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is programed via MRS command. This command is issued by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$ and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The mode register set command time(tMRD) must be satisfied to write the data in mode register. During the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until resetted by another MRS command.



| BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | tWR | | | DR | TM | CAS Latency | | | BT | Burst Length | | |

| BA0 | MRS Type |
|---|---|
| 0 | MRS |
| 1 | EMRS |

| A7 | Test Mode |
|---|---|
| 0 | Normal |
| 1 | Vendor test mode |

| A3 | Burst Type |
|---|---|
| 0 | Nibble Sequential |
| 1 | Interleave |

| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| A11 | A10 | A9 | tWR |
|---|---|---|---|
| 0 | 0 | 0 | Disable |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| A2 | A1 | A0 | Burst Length | |
|---|---|---|---|---|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | Reserved | Reserved |
| 0 | 0 | 1 | Reserved | Reserved |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | Reserved |

## BURST LENGTH & TYPE

Read and write accesses to the DDR2 SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. DDR2 SDRAM supports 4bit burst and 8bit burst modes only. For 8bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation.

Accesses within a given burst may be programmed to be either nibble sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definitionon Table

Seamless burst read or write operation are supported. Unlike DDR-I devices, interruption of a burst read or write operation is prohibited. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

### Burst Length and Sequence

| Burst Length | Starting Address (A2,A1,A0) | Nibble Sequential | Interleave |
|---|---|---|---|
| 4 | X00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | X01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | X10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | X11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 000 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 001 | 1, 2, 3, 0, 5, 6, 7, 4 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 010 | 2, 3, 0, 1, 6, 7, 4, 5 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 011 | 3, 0, 1, 2, 7, 4, 5, 6 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 100 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 101 | 5, 6, 7, 4, 1, 2, 3, 0 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 110 | 6, 7, 4, 5, 2, 3, 0, 1 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 111 | 7, 4, 5, 6, 3, 0, 1, 2 | 7, 6, 5, 4, 3, 2, 1, 0 |

## CAS LATENCY

The CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 3, 4 or 5 clocks. If a Read command is registered at clock edge n, and the latency is m clocks, the data is available nominally coincident with clock edge n + m. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## DLL RESET

A DLL reset is inititated by issuing a Mode Register Set command with bit A8 set to one during initialization sequence. A DLL reset command must be issued to ensure proper device operation. It should be followed by a Mode Register Set command. Fot the stablization of DLL and proper device operation, minimum 200 clock cycles are required between DLL reset and any read command.

## EXTENDED MODE REGISTER SET (EMRS)

The extended mode register is used to store the various operating modes such as DLL disabling, output driver strength, Additive Latency, ODT value selection, OCD programming, DQS and RDQS disabling. The extended mode register is program via MRS command. This command is issued by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ , $\overline{WE}$ and high signals of BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The mode register set command time(tMRD) must be satisfied to write the data in mode register. During the the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until resetted by another EMRS command.

| BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | RDQS | /DQS | OCD Program | | | RTT | Additive Latency | | | RTT | DIC | DLL |

| BA0 | MRS Type |
|---|---|
| 0 | MRS |
| 1 | EMRS(1) |

| A10 | $\overline{DQS}$ Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A11 | RDQS Enable |
|---|---|
| 0 | Disable |
| 1 | Enable |

| A6 | A2 | RTT(nominal) |
|---|---|---|
| 0 | 0 | ODT Disable |
| 0 | 1 | 75ohm |
| 1 | 0 | 150ohm |
| 1 | 1 | Reserved |

| A0 | DLL Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A1 | Output Driver Impedance Control |
|---|---|
| 0 | Full Strength Driver |
| 1 | Half Strength Driver |

**Off-Chip-Driver program**

| A9 | A8 | A7 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | OCD calibration mode exit |
| 0 | 0 | 1 | Drive(1) |
| 0 | 1 | 0 | Drive(0) |
| 0 | 1 | 1 | Adjust mode |
| 1 | 1 | 1 | OCD calibration default |

| A5 | A4 | A3 | Additive Latency |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

* All bits in RFU address fields must be programmed to Zero, all other states are reserved for future usage.

## DLL ENABLE

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before an any command can be issued.

## ADDITIVE LATENCY

Posted CAS, is a feature that allows a DRAM to latch CAS command immediately after the bank activate command (or any time during the tRCD period) without tRCD delay. In side of DRAM, read or Write - CAS command is held for the time of the Additive Latency (AL) before it is issued. Additive latency is programmed to EMRS and it determine internal command hold time. Therefore, if read or write command are issued earlier than minimum tRCD delay, proper addtive latency value must be chosen to insure and that value must be programmed to EMRS. In case of AL=0, operation is the same with ormal SDRAM and DDR SDRAM.

## DQS ENABLE

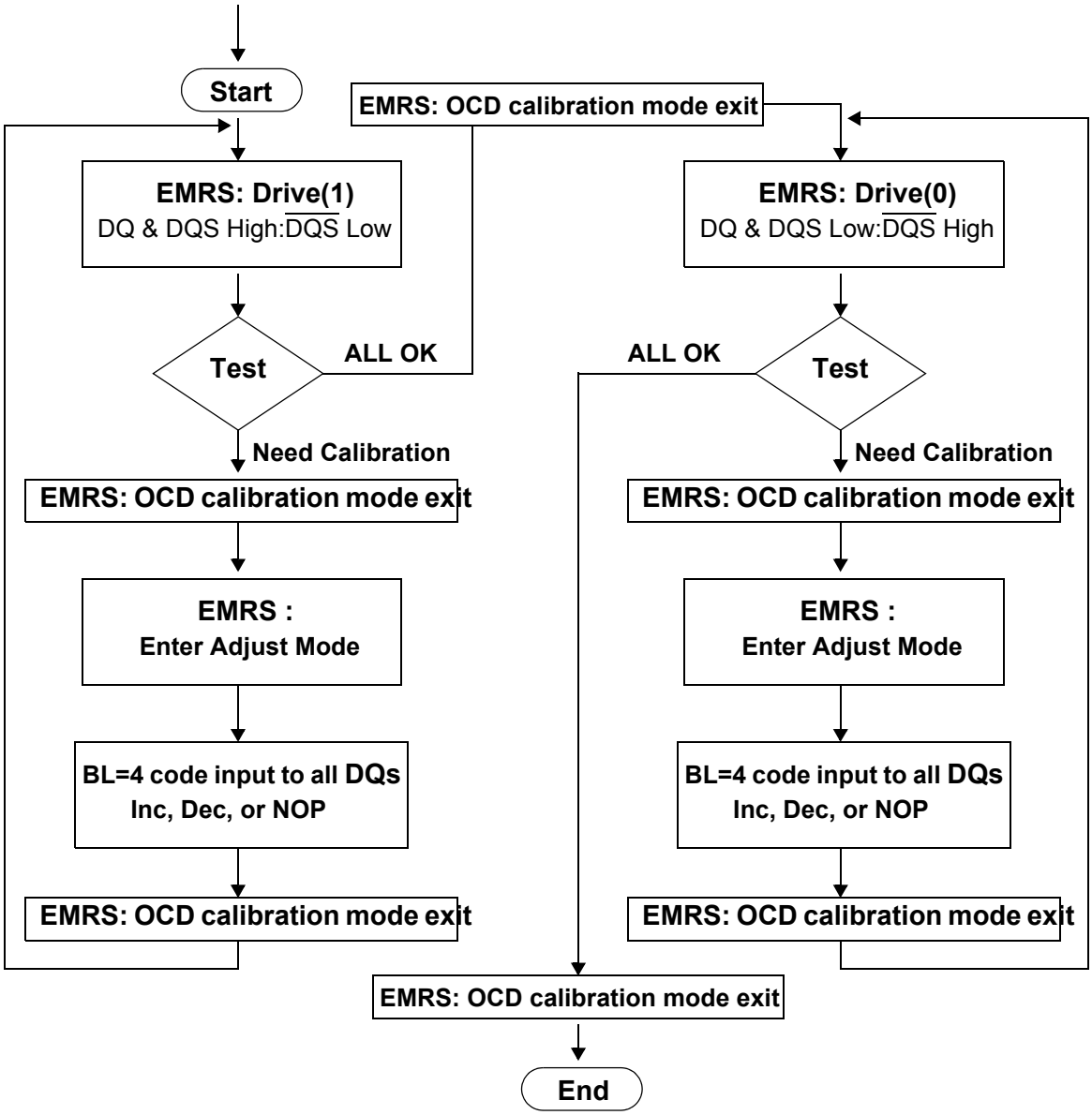
DDR2 SDRAM support both signle ended data strobe and differential data strobe. Differential Strobe is enabled by issuing a Extended Mode Register Set command with bit A10 to set to zero. When differential data strobe is enabled, timing relationships are measured relative to the crosspoint of DQS and its complement, DQS. Differential Strobe is disabled by issuing a Extended Mode Register Set command with bit A10 to set to one. In single ended data strobe mode, timing relationships are measured relative to the rising or falling edges of DQS. It's operation is the same with DDR-I.

## RDQS ENABLE

Read Data Strobe, feature is intended to simplify controller design when x4 configuration DRAM based DIMM and x8 configuration DRAM based DIMM are mixed on the board. Read Data Strobe, is the feature for the only x8 configuration DRAMs. When Read Data Strobe is enabled by issuing a Extended Mode Register Set command with bit A11 to set to zero, data out - DQ0~3 alligned with DQS and DQ4~7 alligned with RDQS. When write case, input on RDQS is ignored by DRAM.

## OFF CHIP DRIVER(OCD) IMPEDANCE ADJUSTMENT

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment.



## Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive(1) mode, all DQ, DQS signals are driven high and all $\overline{DQS}$ signals are driven low. In drive(0) mode, all DQ, DQS signals are driven low and all $\overline{DQS}$ signals are driven high. In adjust mode, BL=4 of operation code data must be used. In case of OCD calibration default, output driver characteristics follow approximate nominal V/I curve for 18 ohm output drivers, but are not guranteed. If tighter control is required, which is controlled within 18ohm +/- 3ohm driver impedance range, OCD must be used.

**Off-Chip Driver program**

| A9 | A8 | A7 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | OCD calibration mode exit |
| 0 | 0 | 1 | Drive(1) DQ, DQS high and $\overline{DQS}$ low |
| 0 | 1 | 0 | Drive(0) DQ, DQS low and $\overline{DQS}$ high |
| 1 | 0 | 0 | Adjust mode |
| 1 | 1 | 1 | OCD calibration default |

## OCD impedance adjust

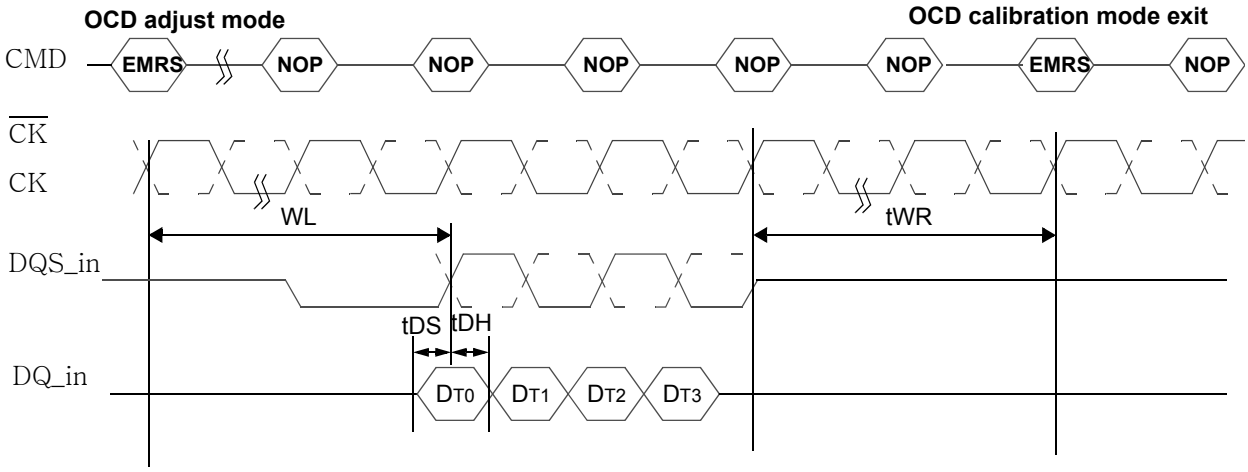
OCD impedance adjustment can be done using “EMRS Adjust mode” and “input operation code patterns” as the following table. To adjust output driver impedance, controllers must issue “Adjust mode” command using an EMRS command first, after that drive 4 bit of burst code information to DDR2 SDRAM. For this operation, controllers must drive all DQs to each device. Driver impedance in each DDR2 SDRAM device is adjusted for all DQs simultaneously. The maximum step count for adjustment is 8 and when the limit is reached, further increment or decrement has no effect. Default setting can be any step within the 8 step range.

**Off Chip Driver Program**

| 4bit burst code inputs to all DQs | | | | Operation | |
|---|---|---|---|---|---|
| DT0 | DT1 | DT2 | DT3 | Pull-up driver strength | Pull-down driver strength |
| 0 | 0 | 0 | 0 | NOP(No operation) | NOP (No operation) |
| 0 | 0 | 0 | 1 | Increase by 1 step | NOP |
| 0 | 0 | 1 | 0 | Decrease by 1 step | NOP |
| 0 | 1 | 0 | 0 | NOP | Increase by1 step |
| 1 | 0 | 0 | 0 | NOP | Decrease by 1 step |
| 0 | 1 | 0 | 1 | Increase by 1 step | Increase by1 step |
| 0 | 1 | 1 | 0 | Decrease by 1 step | Increase by1 step |
| 1 | 0 | 0 | 1 | Increase by1 step | Decrease by 1 step |
| 1 | 0 | 1 | 0 | Decrease by 1 step | Decrease by 1 step |
| Other Combinations | | | | Reserved | |

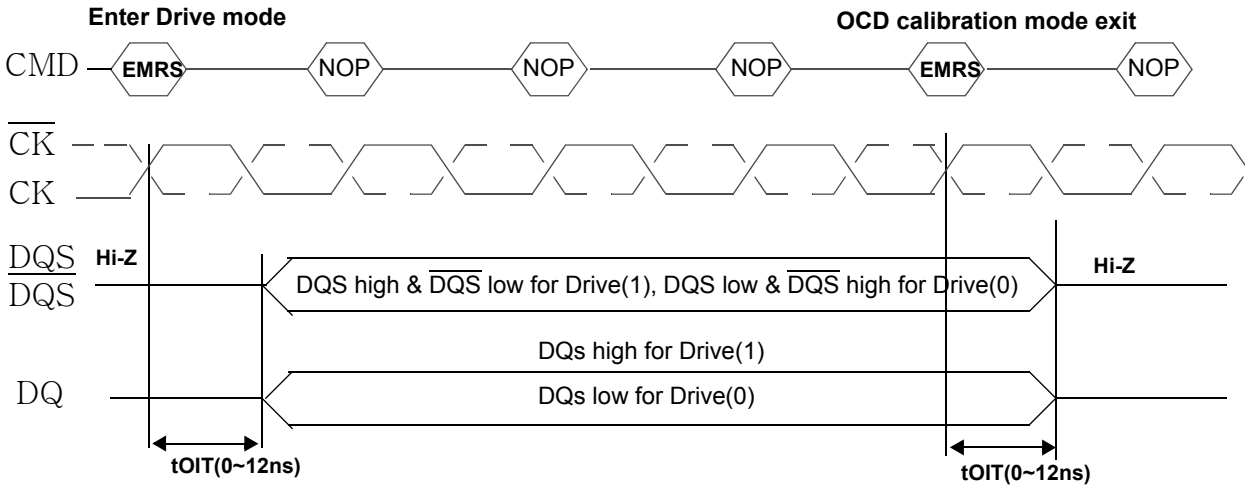
## OCD impedance adjust(continued)

For proper operation of adjust mode, WL = RL - 1 = AL + CL -1 clocks and tDS/tDH should be met as the following timing diagram. For input data pattern for adjustment, DT0-DT3 is a fixed order and “not affected by MRS addressing mode (ie. sequential or interleave)




## Drive Mode

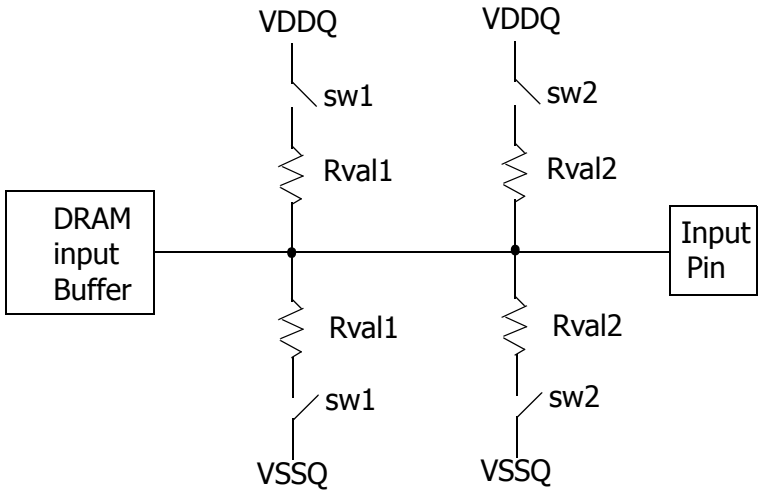
Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned off tOIT after “OCD calibration mode exit” command as the following timing diagram.



## ON DIE TERMINATION

On DRAM Termination (ODT), is a feature that allows a DRAM to turn on/off an active termination resistance for DQ, DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, and DM signals via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. This proposal outlines DDR2 SDRAM ODT definition and functionality for ACTIVE and STANDBY modes. The Active Termination function is turned off and not supported in SELF REFRESH mode.

## FUNCTIONAL REPRESENTATION OF ODT




Switch sw1 or sw2 is enabled by ODT pin.

Selection between sw1 or sw2 is determined by “Rtt(nominal)” in EMRS.

Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

Target Rtt (Ohm) = (Rval1) / 2 or (Rval2) / 2

## DC Electrical Characteristics and Operating Conditions

| Parameter / Condition | SYMBOL | MIN | NOM | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Rtt effective impedance value for EMRS(A6, A2)=0, 1; 75 ohm | Rtt1(eff) | 60 | 75 | 90 | ohm | 1 |
| Rtt effective impedance value for EMRS(A6, A2)=1, 0; 150 ohm | Rtt2(eff) | 120 | 150 | 80 | ohm | 1 |
| Rtt mismatch tolerance between any pull-up/pull-down pair | Rtt(mis) | -3.75 | | +3.75 | % | 1 |

## TEST CONDITION FOR Rtt MEASUREMENTS (Note1)

### Measurement Definition for Rtt (eff)

Apply VIHac and VILac to test pin seperately, then measure current I(VIHac) and I(VILac) respectively.

$$\mathrm{Rtt(eff)} = \frac{\mathrm{VIHac} - \mathrm{VILac}}{\mathrm{I(VIHac)} - \mathrm{I(VILac)}}$$

### Measurement Definition for Rtt (mis)

Measure voltage (VM) at test pin (midpoint) with no load.

$$\mathrm{Rtt(mis)} = \left(\frac{2 \times \mathrm{Vm}}{VDDQ} - 1\right) \times 100\%$$

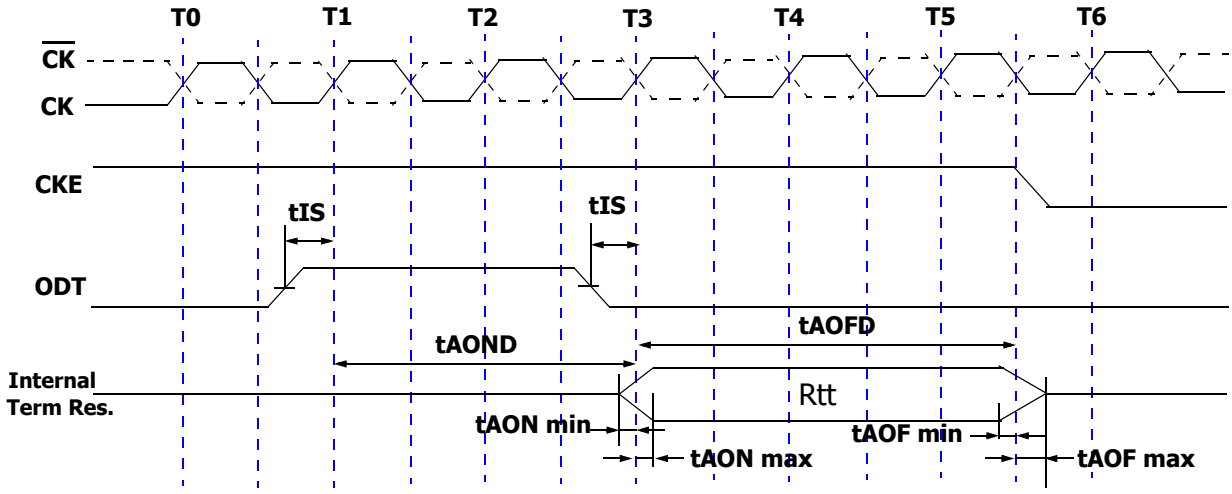
Note1 : VIHac, VILac, and VDDQ values defined in SSTL_18 (JC-16 item #103).

## AC Electrical Characteristics and Operating Conditions

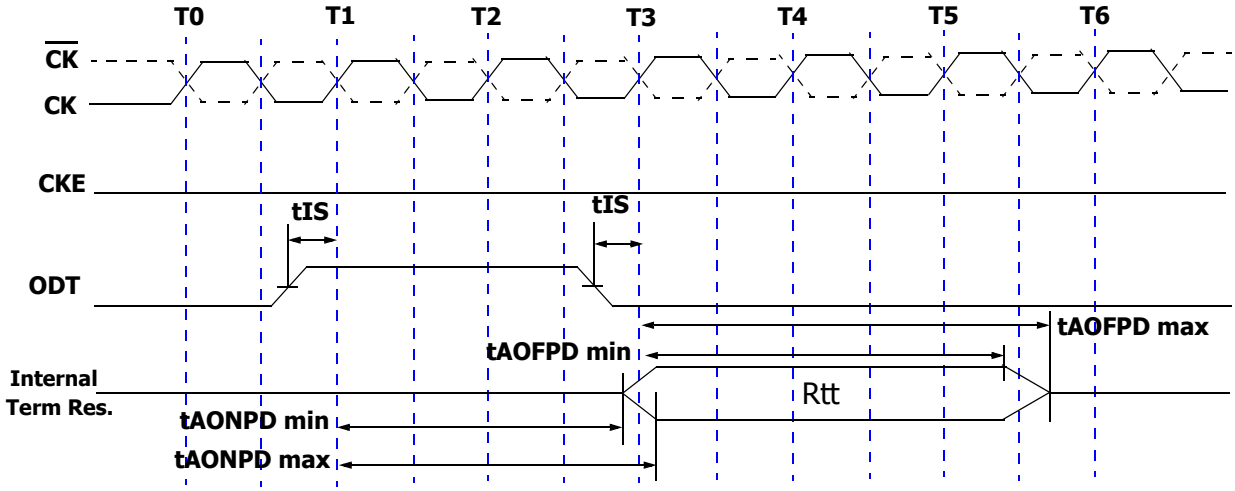
| Parameter / Condition | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| ODT turn-on delay | tAOND | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(min) | tAC(max)+1ns | ns | 1 |
| ODT turn-on(Power Down mode) | tAONPD | tAC(min)+2ns | 2tCK+tAC(max)+1ns | ns | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(min) | tAC(max)+1ns | ns | 2 |
| ODT turn-off (Power Down mode) | tAOFPD | tAC(min)+2ns | 2.5tCK+tAC(max)+1ns | ns | |

Note1 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.
Note2 ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

**ODT Timing for Active/Standby Mode**




**ODT Timing for Power Down Mode**



## ON DIE TERMINATION - 2 Slot System Termination Matrix

### Termination Matrix for Writes to DRAM

| Configuration | Write to | Target DQ On Die Termination Resistance RTT | | | | |
|---|---|---|---|---|---|---|
| | | Controller | Module in Slot 1 | | Module in Slot 2 | |
| | | | Rank1 | Rank2 | Rank1 | Rank2 |
| 2R/2R | Slot 1 | Infinite | Infinite | Infinite | 75ohm | Infinite (note1) |
| | Slot 2 | Infinite | 75ohm | Infinite (note1) | Infinite | Infinite |
| 2R/1R | Slot 1 | Infinite | Infinite | Infinite | 75ohm | Unpopulated |
| | Slot 2 | Infinite | 75ohm | Infinite (note1) | Infinite | Unpopulated |
| 1R/2R | Slot 1 | Infinite | Infinite | Unpopulated | 75ohm | Infinite (note1) |
| | Slot 2 | Infinite | 75ohm | Unpopulated | Infinite | Infinite |
| 1R/1R | Slot 1 | Infinite | Infinite | Unpopulated | 75ohm | Unpopulated |
| | Slot 2 | Infinite | 75ohm | Unpopulated | Infinite | Unpopulated |
| 2R/Empty | Slot 1 | Infinite | 150ohm | Infinite | Unpopulated | Unpopulated |
| Empty/2R | Slot 2 | Infinite | Unpopulated | Unpopulated | 150ohm | Infinite |
| 1R/Empty | Slot 1 | Infinite | 150ohm | Unpopulated | Unpopulated | Unpopulated |
| Empty/1R | Slot 2 | Infinite | Unpopulated | Unpopulated | 150ohm | Unpopulated |

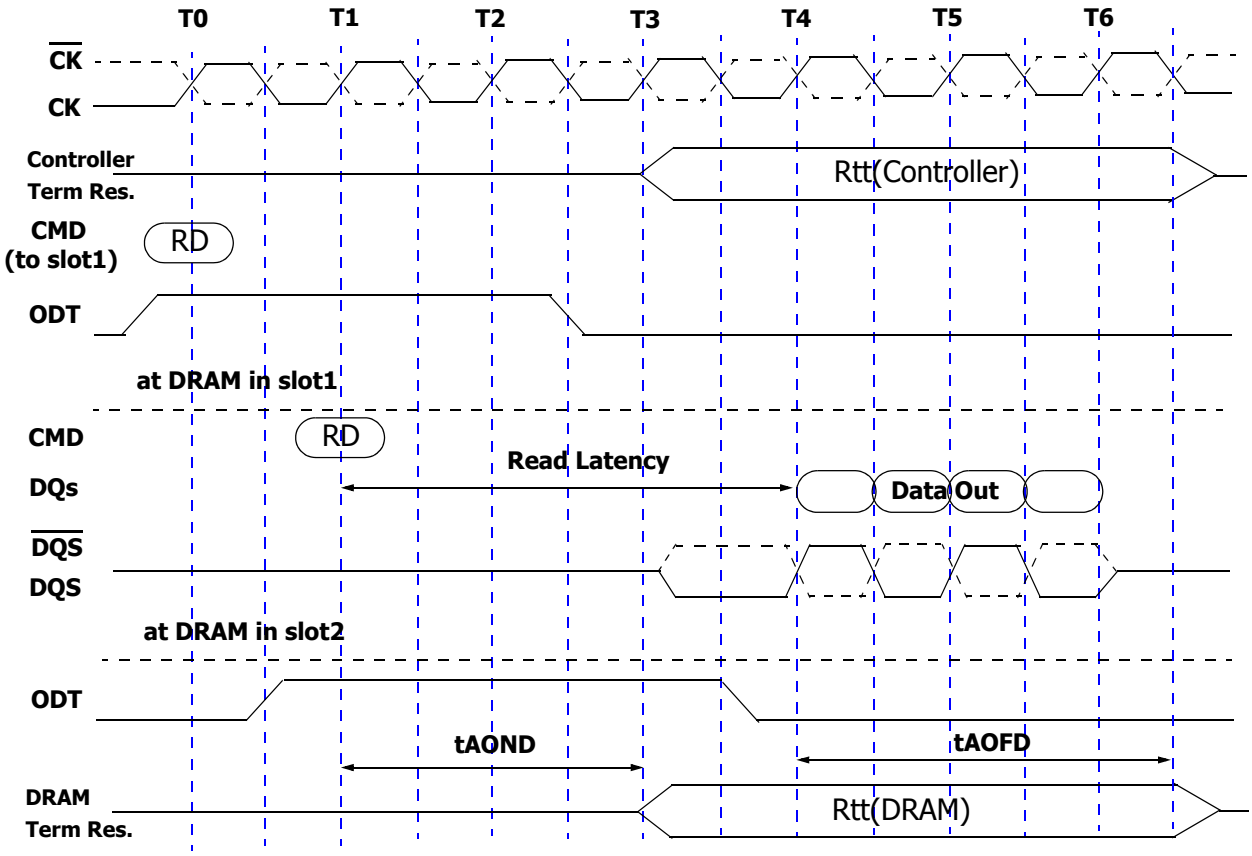
### Termination Matrix for Read from DRAM

| Configuration | Read from | Target DQ On Die Termination Resistance RTT | | | | |
|---|---|---|---|---|---|---|
| | | Controller | Module in Slot 1 | | Module in Slot 2 | |
| | | | Rank1 | Rank2 | Rank1 | Rank2 |
| 2R/2R | Slot 1 | 150ohm | Infinite | Infinite | 75ohm | Infinite (note1) |
| | Slot 2 | 150ohm | 75ohm | Infinite (note1) | Infinite | Infinite |
| 2R/1R | Slot 1 | 150ohm | Infinite | Infinite | 75ohm | Unpopulated |
| | Slot 2 | 150ohm | 75ohm | Infinite (note1) | Infinite | Unpopulated |
| 1R/2R | Slot 1 | 150ohm | Infinite | Unpopulated | 75ohm | Infinite (note1) |
| | Slot 2 | 150ohm | 75ohm | Unpopulated | Infinite | Infinite |
| 1R/1R | Slot 1 | 150ohm | Infinite | Unpopulated | 75ohm | Unpopulated |
| | Slot 2 | 150ohm | 75ohm | Unpopulated | Infinite | Unpopulated |
| 2R/Empty | Slot 1 | 75ohm | Infinite | Infinite | Unpopulated | Unpopulated |
| Empty/2R | Slot 2 | 75ohm | Unpopulated | Unpopulated | Infinite | Infinite |
| 1R/Empty | Slot 1 | 75ohm | Infinite | Unpopulated | Unpopulated | Unpopulated |
| Empty/1R | Slot 2 | 75ohm | Unpopulated | Unpopulated | Infinite | Unpopulated |

Note1 : Alternatively, the controller may use rank2 for termination instead of rank1

## ODT Control of READs

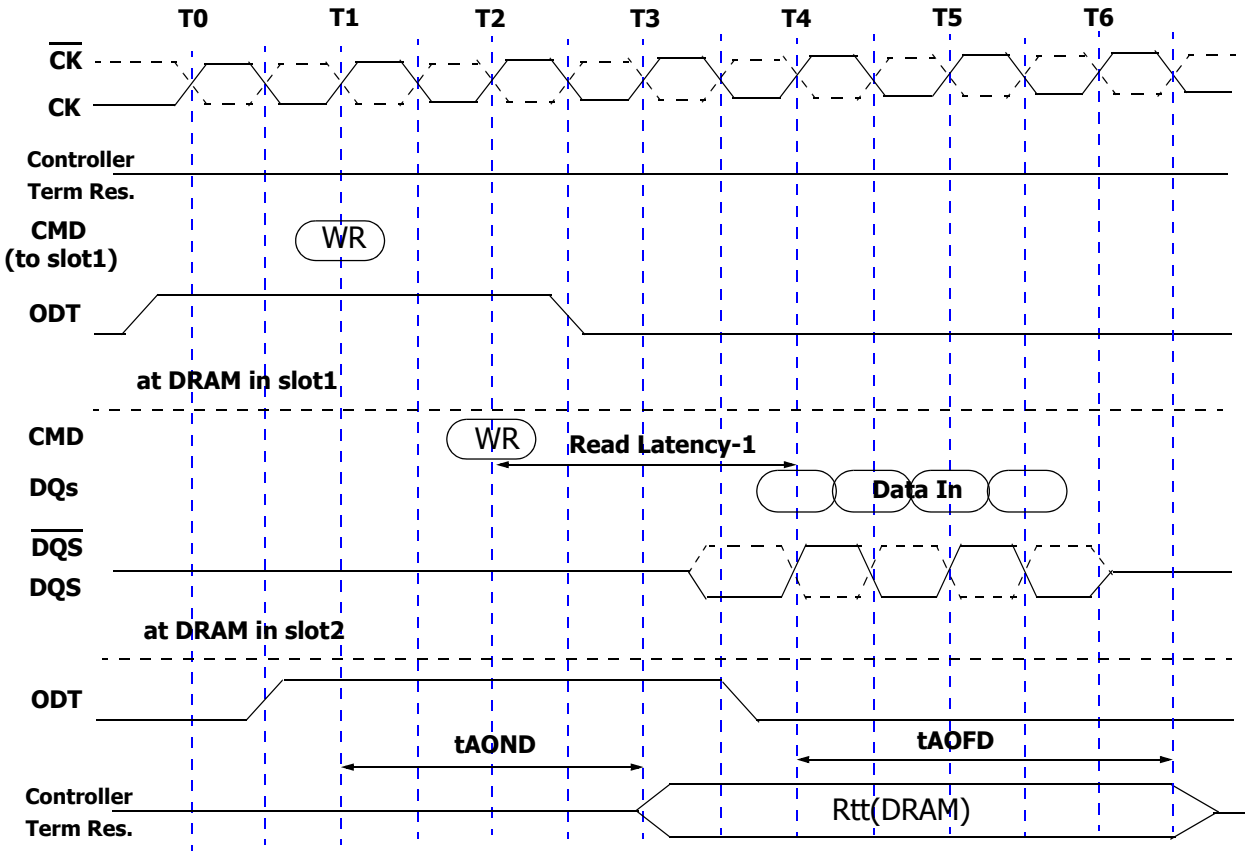
At a minimum, ODT must be latched High by CK at (Read Latency - 3tCK) after the Read Command and remain High until (Read Latency + BL/2 - 2tCK) after the RD command (where Read Latency = AL + CL). The controller is also required to activate it's own termination with a turn on time the same as the DRAM and keeping it on until valid data is no longer on the system bus.




**Read Example for a 2 slot registered system with 2nd slot in Active Mode**
**(Read Latency = 3tCK; tAOND = 2tCK; tAOFD = 2.5tCK)**

## ODT Control of Writes

At a minimum, ODT must be latched High by CK at (Read Latency - 3tCK) after the WR Command and remain High until (Write Latency + BL/2 - 2tCK) after the WR command (where Write Latency = Read Latency - 1tCK). During writes, no ODT is required at the controller.




**Write Example for a 2 slot registered system with 2nd slot in Active Mode**
**(Read Latency = 3tCK; tAOND = 2tCK; tAOFD = 2.5tCK)**

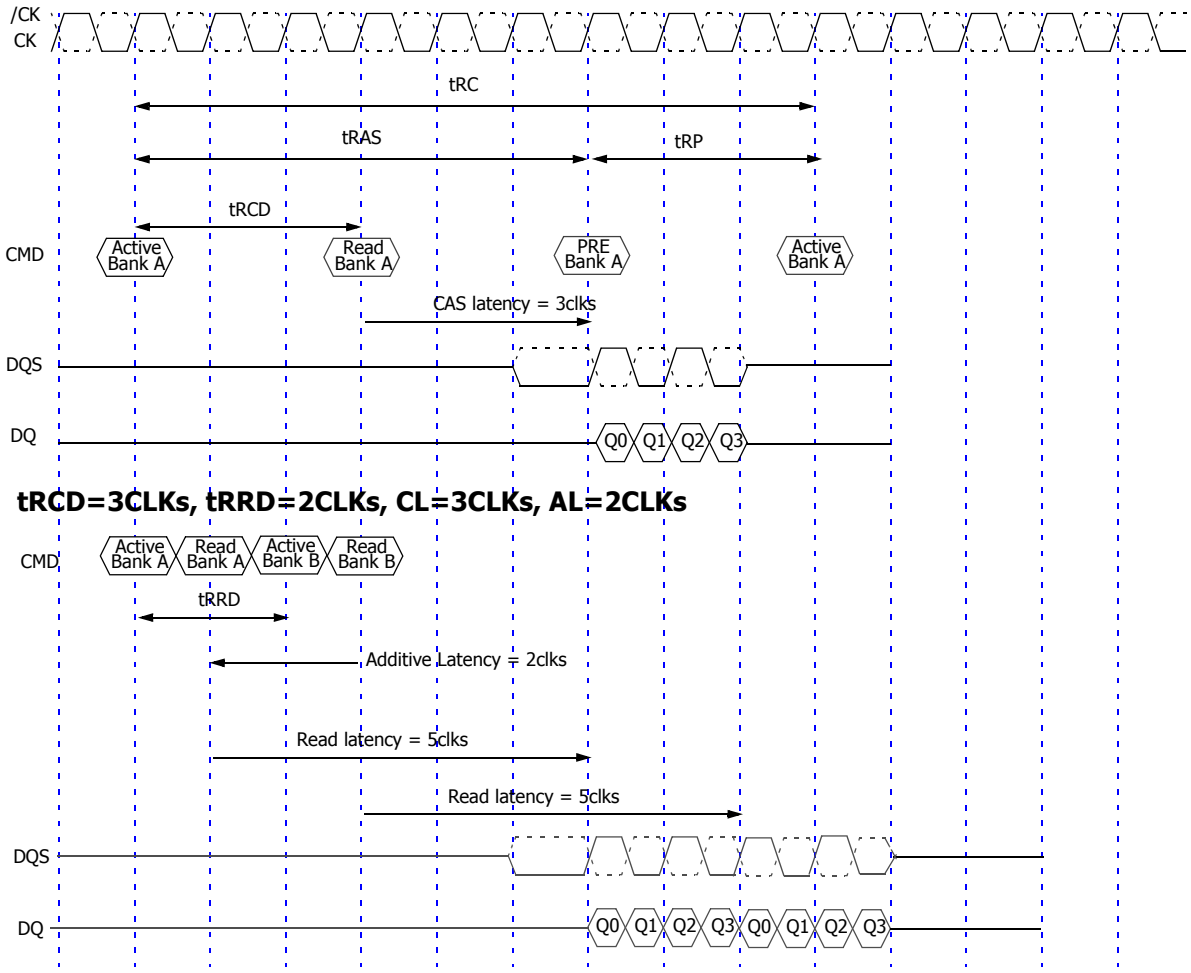
## FUNCTION DESCRIPTION

### Bank Active Operation

Bank active should be issued to activate (or open) a row in particular bank for a subsequent read or write access. Bank active command is issued by holding $\overline{CS}$ and $\overline{RAS}$ low, $\overline{CAS}$ and $\overline{WE}$ high at the rising edge of clock. Bank address and row address provided on inputs BA0~BA1 and A0~A13 selects the bank and row. Minumun delay between bank active to read or write command is determined by additive latency, which programmed to EMRS. When additive latency value zero is programmed to EMRS, minumun delay between bank active to read or write command is tRCD (RAS to CAS delay). In that case, operation is the same with normal SDRAM and DDR SDRAM. But,. when the other additive latency values are programmed to EMRS, read or write command could be issued without time delay of tRCD (RAS to CAS delay). But, if read or write command are issued earlier than minimum tRCD delay, proper addtive latency value must be chosen to insure and that value must be programmed to EMRS.

To select different row in the same bank, activated bank must be prechareged prior to bank active. Minimum interval between successive bank activate commands to the same bank is determined by the tRC (RAS cycle time), which is equal to tRAS + tRP. To ensure proper operation, minimun delay of tRAS and tRP must be maintained.

**tRCD=3CLKs, tRP=3CLKs, CL=3CLKs, AL=0CLK**




**tRCD=3CLKs, tRRD=2CLKs, CL=3CLKs, AL=2CLKs**

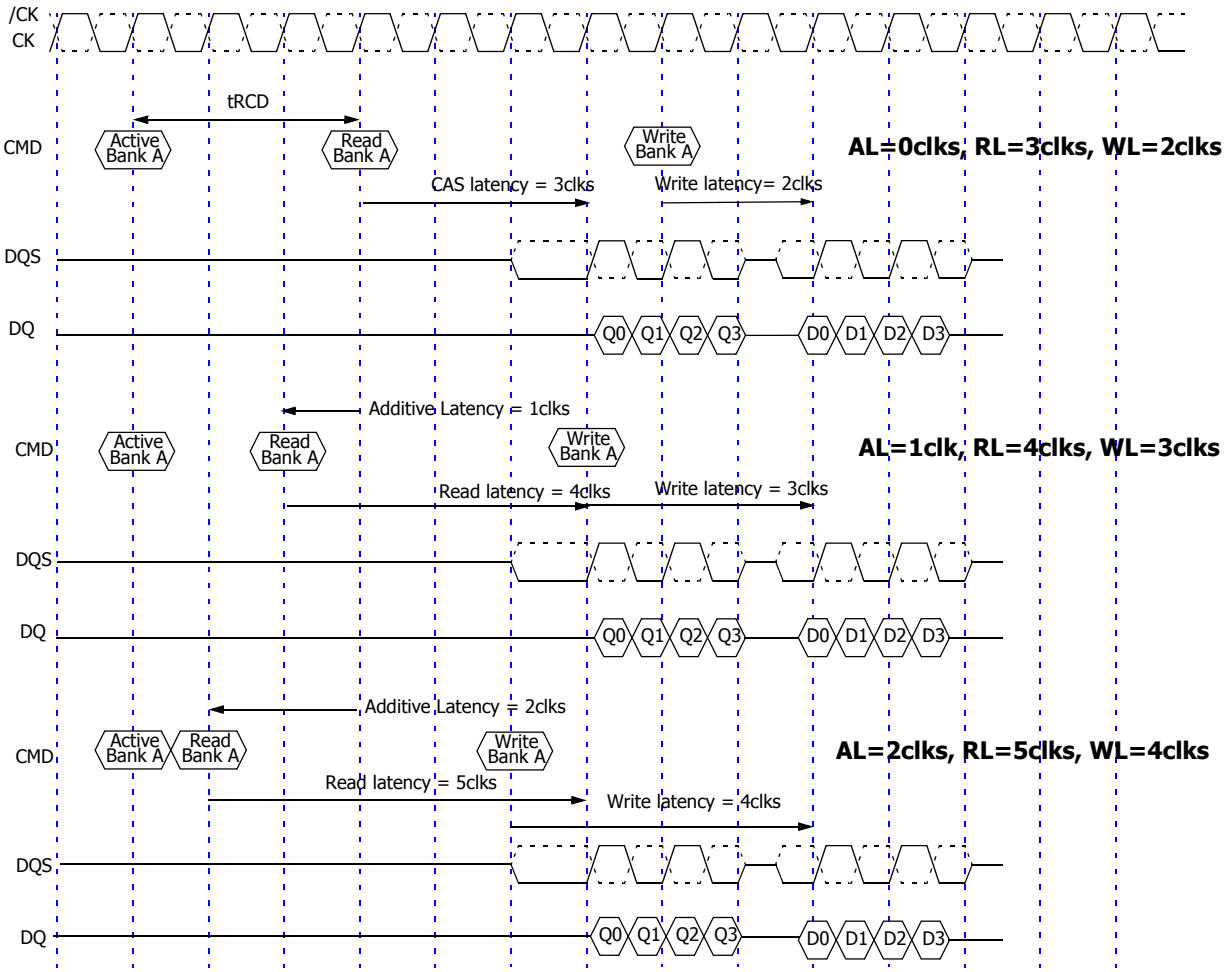
## Posted CAS Opeation

DDR2 SDRAM has new feature, Posted CAS. It is intended for improvement of command bus efficiency. Posted CAS operation make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In Posted CAS operation, read or write command could be issued immediately after the bank activate command (or any time during the tRCD period) without tRCD delay.

In side of DRAM, read or Write - CAS command is held for the time of the Additive Latency (AL) before it is issued. Additive latency is programmed to EMRS and it determine internal command hold time. Therefore, if read or write command are issued earlier than minimum tRCD delay, proper addtive latency value must be chosen to insure and that value must be programmed to EMRS. In case of AL=0, operation is the same with normal SDRAM and DDR SDRAM.

Due to the nature of posted CAS operation, DDR2 define RL (read latency) and WL (write latency). RL is determined by sum of additive latency and CAS latency. WL is defined as RL-1. To utilize this feature, proper additive latency value (greater than 0) must be programmed to EMRS.

**tRCD=3CLKs, CL=3CLKs**



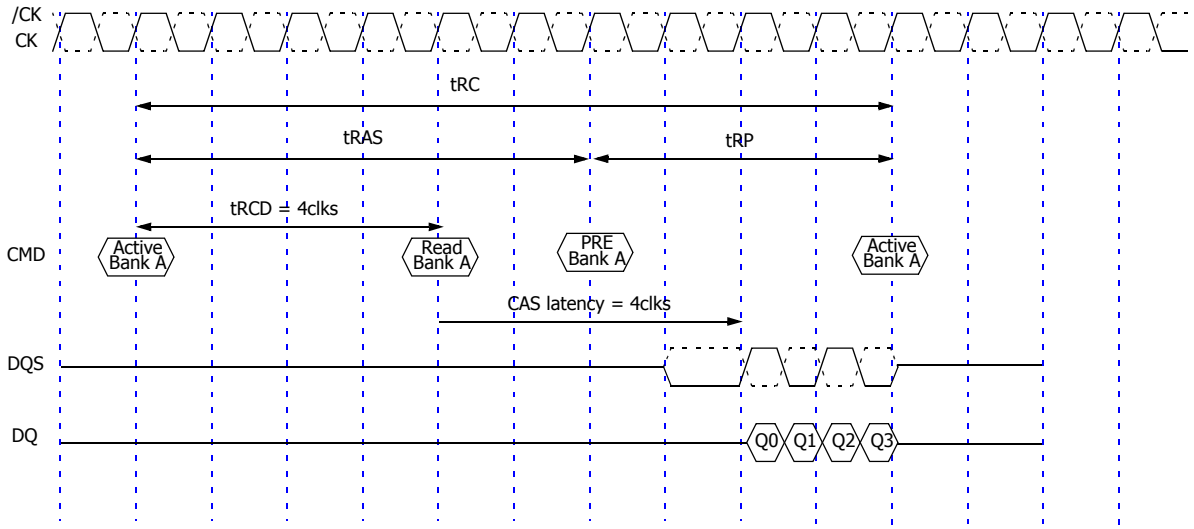
## Burst Read Opeation

Burst read command is issued by activating CS and CAS, deactivating $\overline{RAS}$ and $\overline{WE}$ at the rising edge of clock. Bank address and column address provided on inputs BA0~BA1 and A0~A13 selects the bank and starting column address for burst operation. Before the burst read command, the bank must be activated earlier. First burst data come out RL delay later when burst read command is issued. Burst read command to data output delay is determined by RL (Read Latency), where AL + CL.

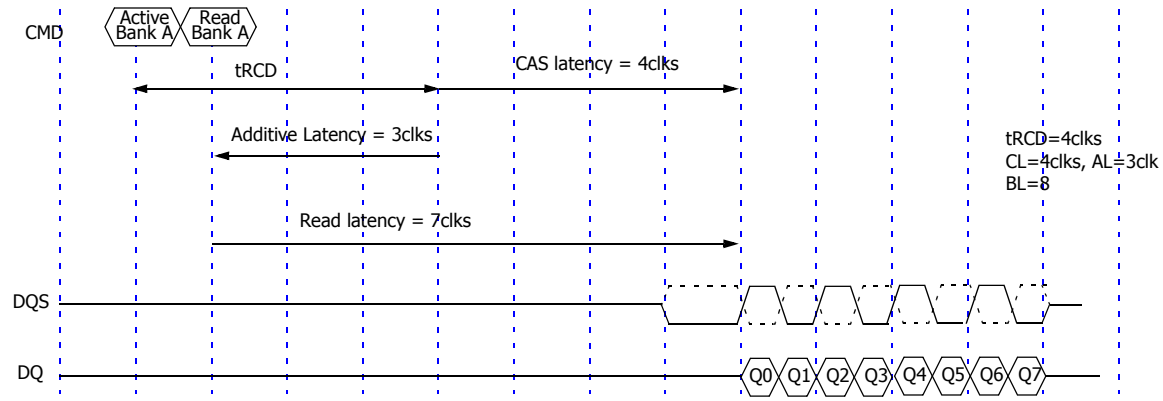
DDR2 SDRAM has been implemented with differential data strobe signal pair (/DQS and DQS) which toggles high and low during burst with the same frequency as clock. DQS pair (/DQS) is driven by the DDR2 SDRAM along with output data. Differenital pair of data strobe is driven to low/high state from Hi-Z state one clock prioir to valid data. The initial state on DQS (/DQS) is called as the read preamble. Optional single ended strobe operation is supported by EMRS.

DDR2 SDRAM do not allow any interruption of read burst due to the nature of 4bit prepatch architecture. Unlike DDR-I SDRAM, read burst interupt by precharge, another read command or burst stop is prohibited during read burst. Burst read command to the another bank can be given with having activated that bank where RAS to RAS delay (tRRD) is satisfied.

**tRCD=4CLKs, tRP=4CLKs, CL=4CLKs, AL=0CLK, BL=4**




**tRCD=4CLKs, tRP=4CLKs, CL=4CLKs, AL=3CLK, BL=8**



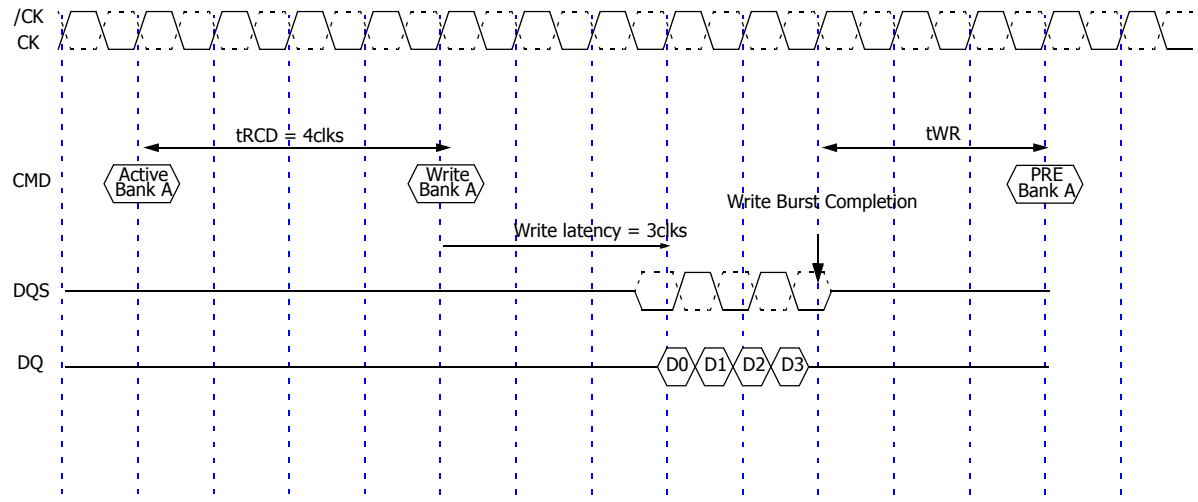
## Burst Write Opeation

Burst write command is issued by activating $\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ and deactivating RAS at the rising edge of clock. Bank address and column address provided on inputs BA0~BA1 and A0~A13 selects the bank and starting column address for burst operation. Before the burst write command, the bank must be activated earlier. Write command to data-in delay is determined by WL (Write latency). WL is RL-1, it's equal to AL+CL-1.

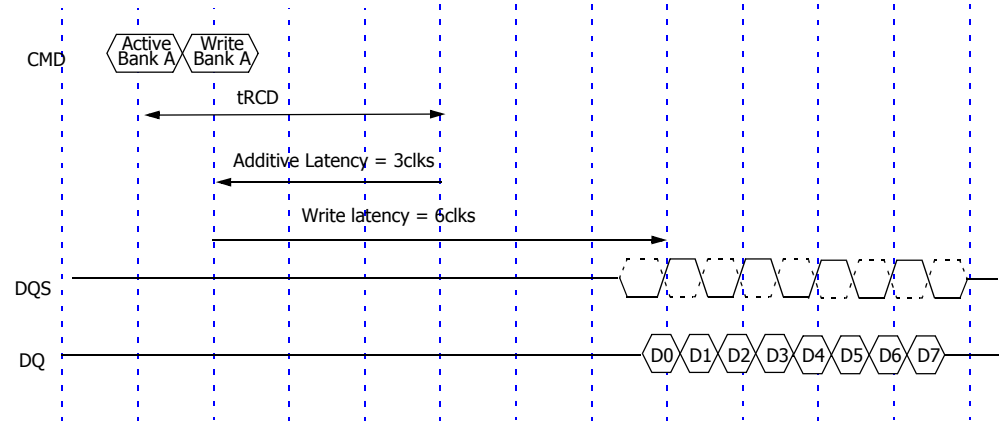
A data strobe signal pair (DQS and /DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The subsequent burst bit data are issued on successive edges of the DQS until the write burst is completed. The tDQSS specification must be satisfied for write cycles. To complete burst write operation, write recovery time (tWR) must be maintained before precharge commaned issued.

DDR2 SDRAM do not allow any interruption of write burst due to the nature of 4bit prepatch architecture. Unlike DDR-I SDRAM, write burst interupt by precharge, or another write command is prohibited during write burst. Burst write command to the another bank can be given with having activated that bank where RAS to RAS delay (tRRD) is satisfied.

**CL=4CLKs, AL=0CLK, tWR=3CLKs, BL=4**



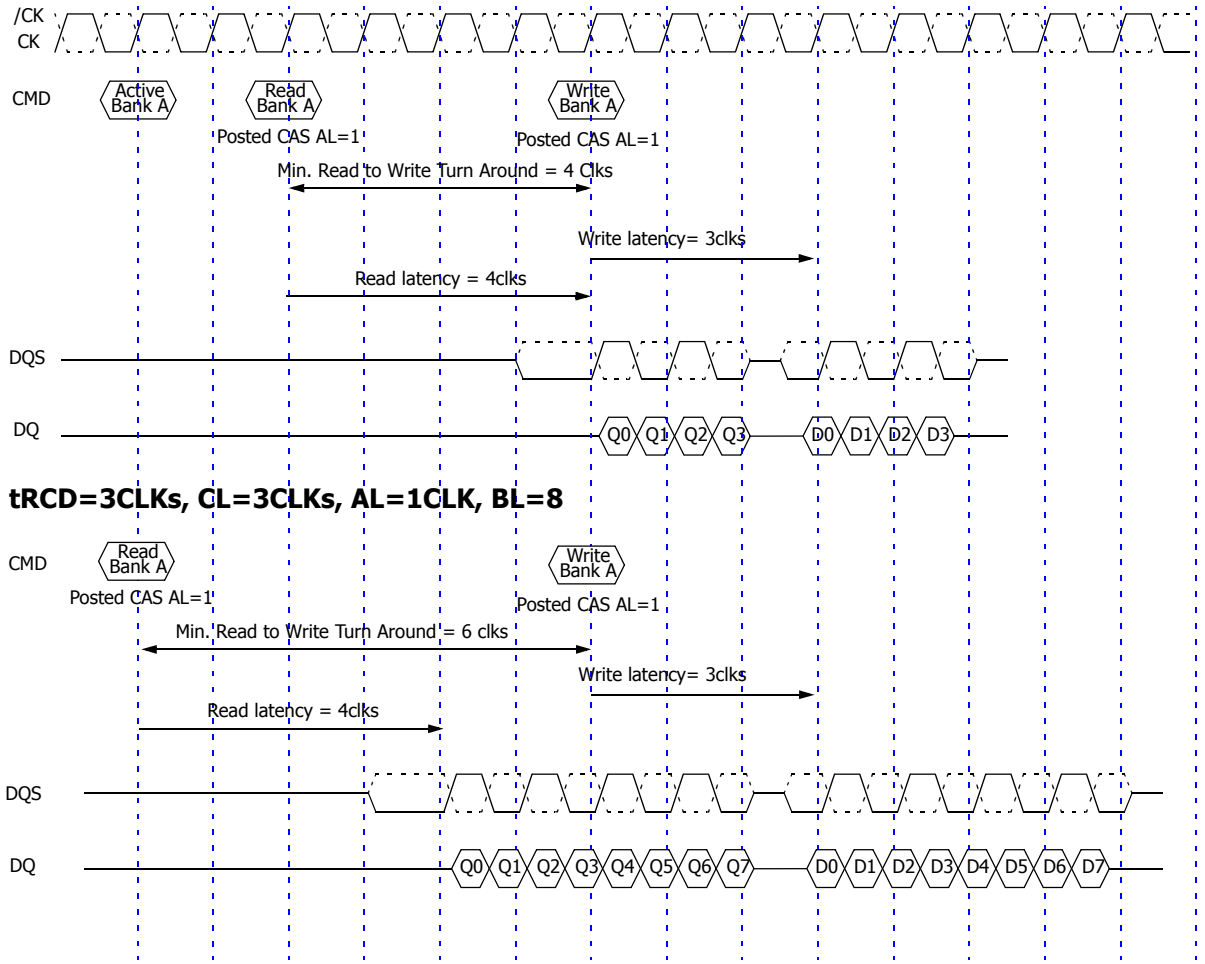

**CL=4CLKs, AL=3CLK, BL=8**



## Read to Write Opeation

Minimum read-to-write-turn around-time is 4 clocks for BL4, 6 clock for BL8

### tRCD=3CLKs, CL=3CLKs, AL=1CLK, BL=4

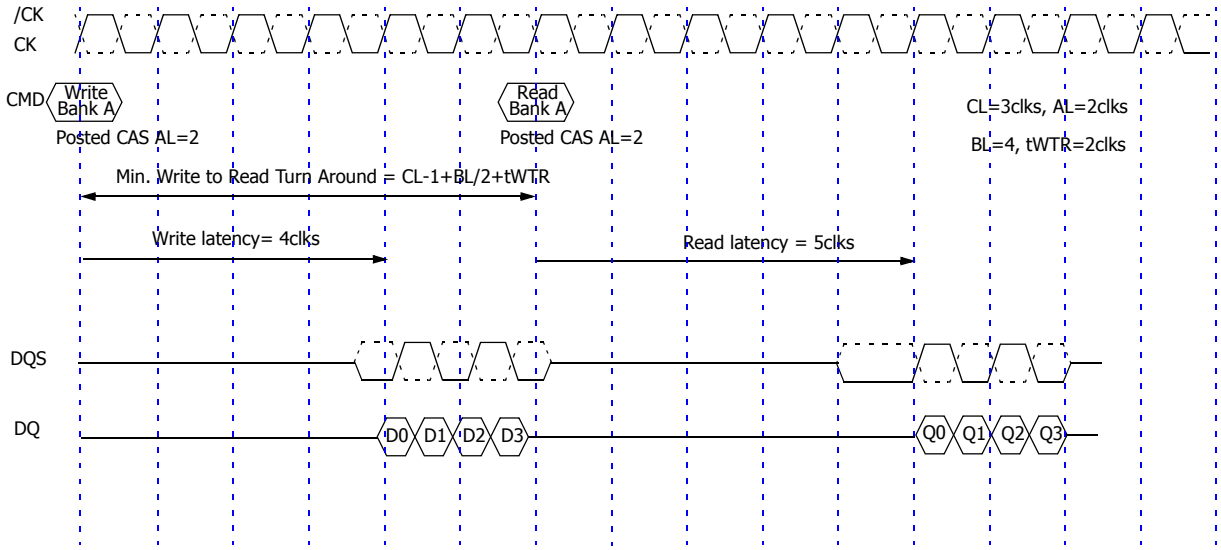



### tRCD=3CLKs, CL=3CLKs, AL=1CLK, BL=8

## Write to Read Opeation

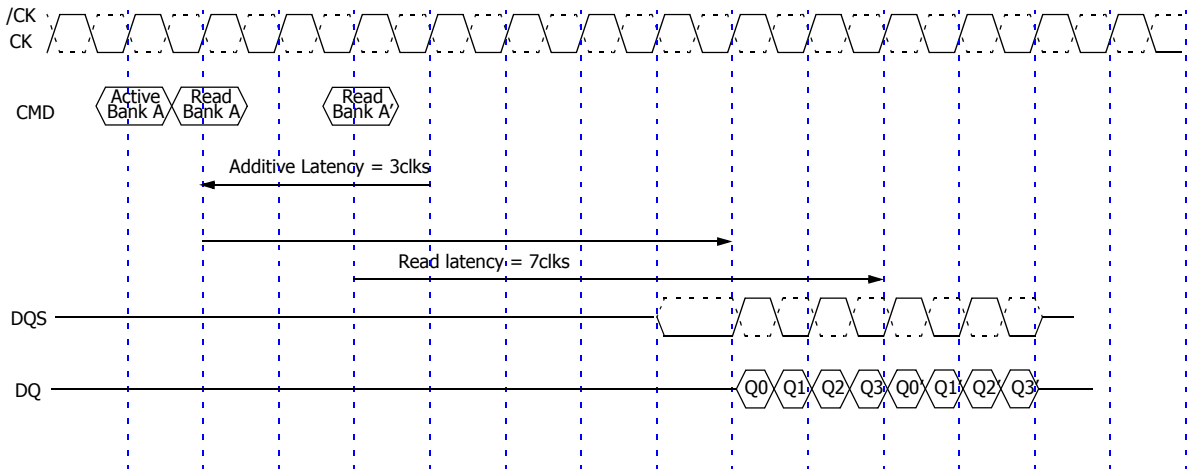
Minimum time interval from burst write to burst read is "CL-1+BL/2+tWTR" (Internal Write to Read command delay)

**CL=3CLKs, AL=2CLK, BL=4, tWTR=2CLKs**



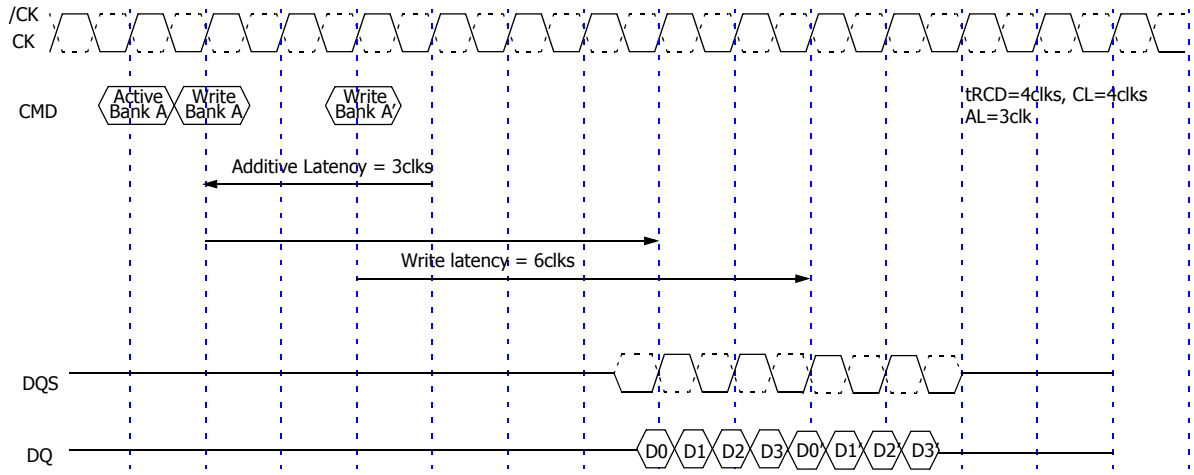
## Seamless Burst Read Opeation

### tRCD=4CLKs, CAS Latency=4CLKs, Additive Latency=3CLKs




## Seamless Burst Write Opeation

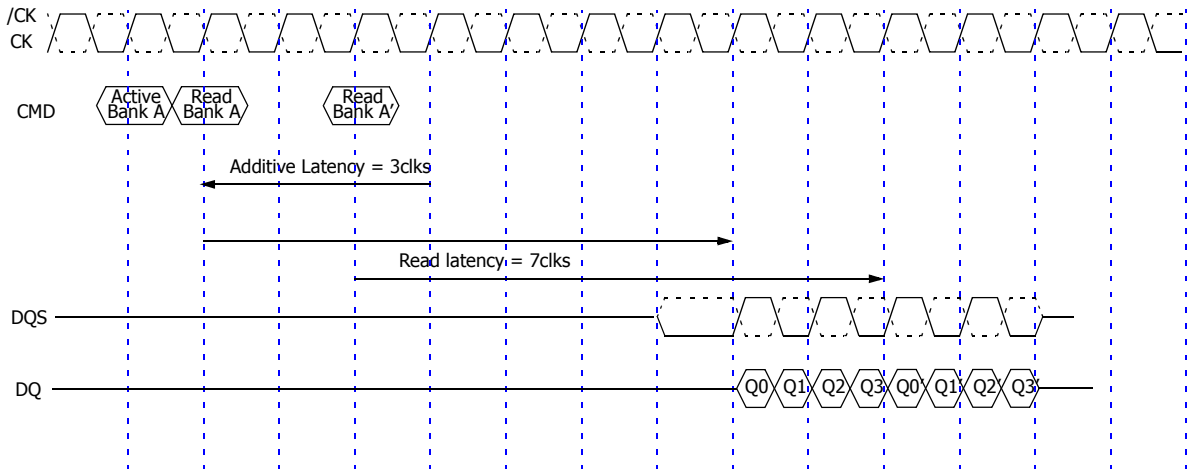
### tRCD=4CLKs, CAS latency=4CLKs, Additive Latency=3CLKs



## Read Burst Interrupt Opeation

Read burst interrupt functions is only allowed on a burst of 8. Interrupting a burst of 4 is prohibited. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited. Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited. Read burst interruption is allowed to any bank inside DRAM. Read burst with Auto Precharge enabled is not allowed to be interrupted. Read burst interruption is allowed by a Read with Auto Precharge command. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL+BL/2 where BL is the burst length set in the mode register and not the actual burst(which is shorter beacuse of interrupt).

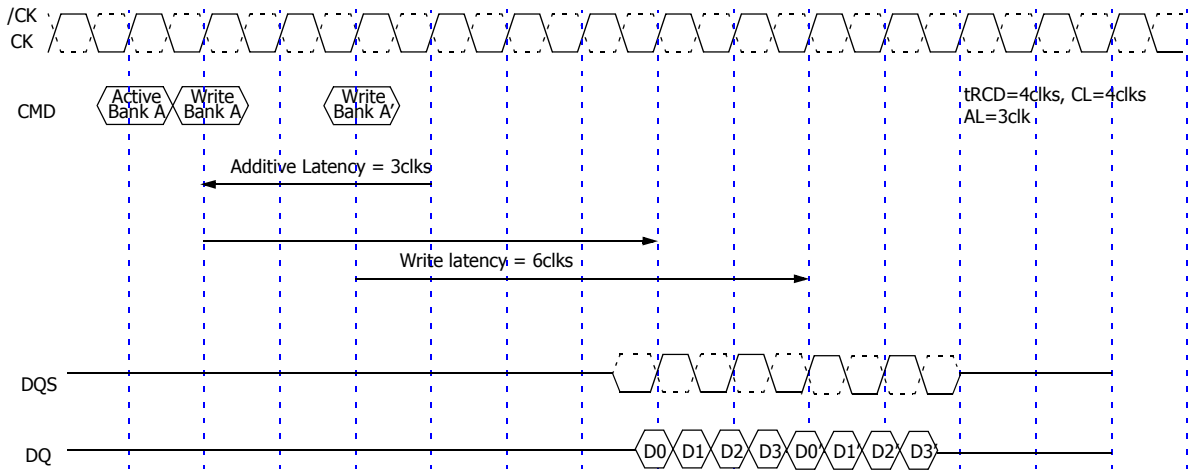
**tRCD=4CLKs, CAS Latency=4CLKs, Additive Latency=3CLKs BL=8**



## Write Burst Interrupt Opeation

Write burst interrupt functions is only allowed on a burst of 8. Interrupting a burst of 4 is prohibited. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited. Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited. Write burst interruption is allowed to any bank inside DRAM. Write burst with Auto Precharge enabled is not allowed to be interrupted. Write burst interruption is allowed by a Write with Auto Precharge command. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

**tRCD=4CLKs, CAS latency=4CLKs, Additive Latency=3CLKs BL=8**



## Precharge Opeation

The precharge command is used to close or deactivate the open row in particular bank or the open row in all banks. Precharge command is issued by activating $\overline{CS}$, $\overline{RAS}$, WE and deactivating CAS at the rising edge of clock. Bank address and A10 provided on inputs BA0~BA1, A10 selects the bank to be precharged. Input A10 determines whether one or all banks precharge. All bank precharged command is issued with A10=high, at that case, the other bank address inputs are don't care. But Bank address inputs select bank to be precharged, when precharge command is issued with A10 = low. Once a bank has been precharged, it is in the idle state and must be activated prior to any read or write commands being issued to that bank. The bank will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Burst termination by precharge command is prohibited.

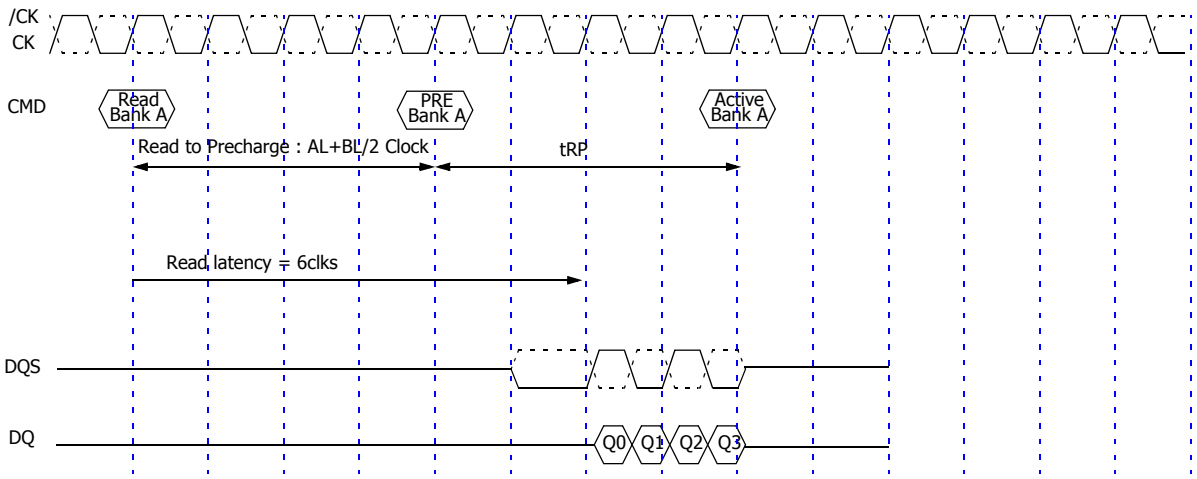
### Bank Selection for Precharge

| A10 | BA0 | BA1 | Precharged Bank |
|---|---|---|---|
| Low | Low | Low | Bank 0 only |
| Low | Low | High | Bank 1 only |
| Low | High | Low | Bank 2 only |
| Low | High | High | Bank 3 only |
| High | Don't care | Don't care | All Banks 0~3 |

## Read to Precharge

**Minimum read to precharge command delay is AL + BL/2clks.**

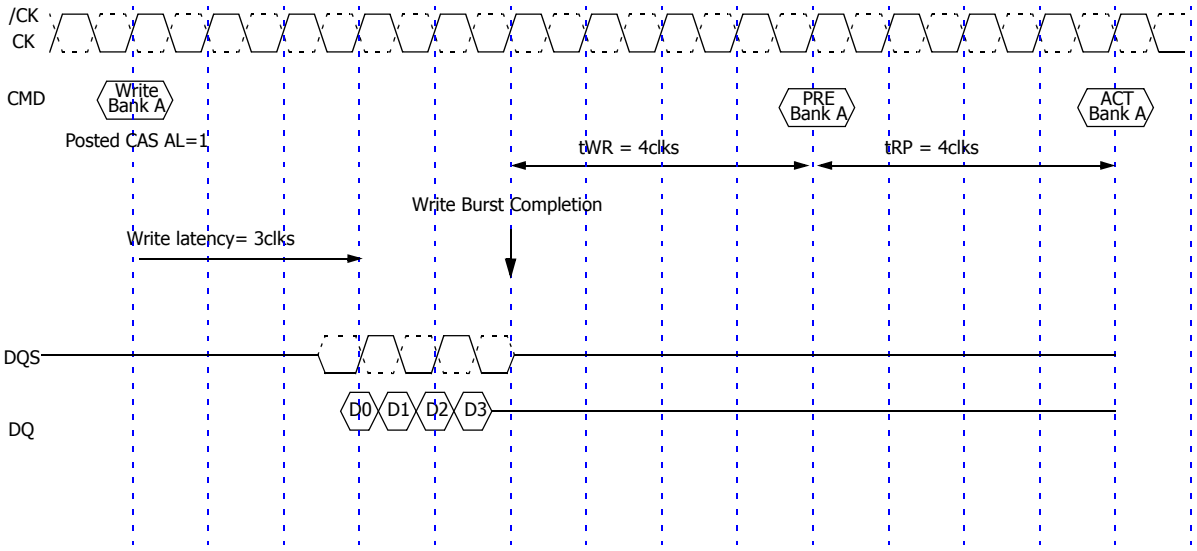
### tRCD=4CLKs, tRP=4CLK, BL=4, CL=4CLKs, AL=2CLKs




## Write to Precharge

**Minimum write to precharge command delay is WL+BL/2clks + tWR.**

### CL=3CLKs, AL=1CLKs, BL=4, tWR=4CLKs



## Auto Precharge

The auto precharge command is issued in conjunction with a specific read or write command. If read or write with auto precharge is issued, precharge command is performed automatically upon completion of the read or write burst. Therefore, activatied bank is closed/ precharged without precharge command. Either normal read (or write) or read (or write) with auto precharge is determined by A10. If A10 is low when read (or write) command is issued, DRAM remain row active state after read or write burst operation. If A10 is high when read (or write) command is issued, DRAM perform read (or write) with auto precharge.

If read with auto precharge is issued to DRAM, DRAM execute normal read burst and then, begin to precharge on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst. If write with auto precharge is issued to DRAM, DRAM execute normal write burst and then, begin to precharge after data-in burst is properly stored The RAS lock-out circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

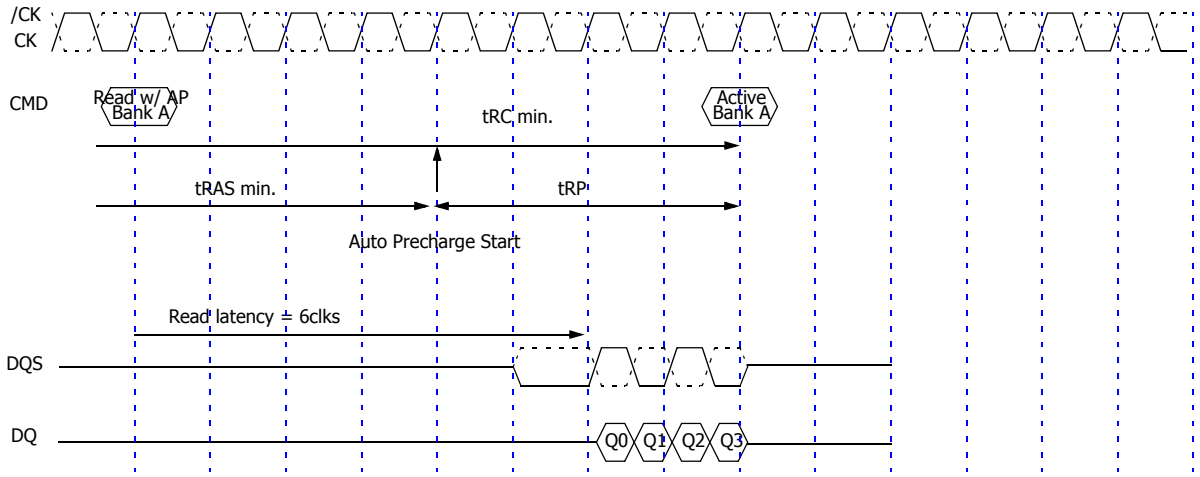
This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lock-out circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

## Read with Auto Precharge

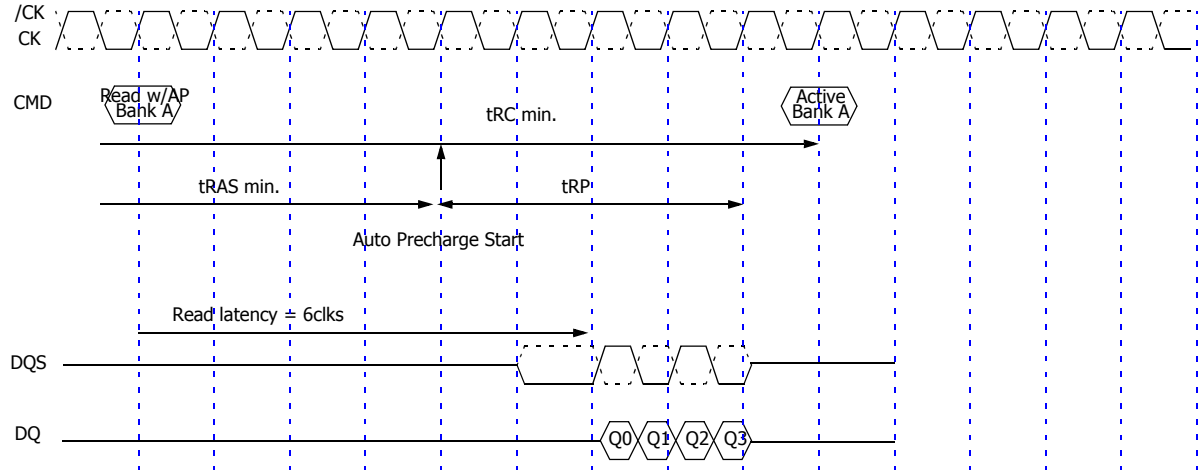
If A10 is high when read command is issued, DRAM perform read with auto precharge. When read with auto precharge command is issued, internal Precharge start automatically. If tRAS minimum is satisfied, internal precharge start at AL+BL/2 cycles later. If tRAS minimum is not satisfied, internal precharge starting point is delayed until tRAS minimum is satisfied. A new active command can be issued to the same bank if the following two conditions are satisfied simultaneously.

1. The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
2. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

### tRCD=4CLKs, tRP=4CLK, BL=4, CL=4CLKs, AL=2CLKs (tRP limit)



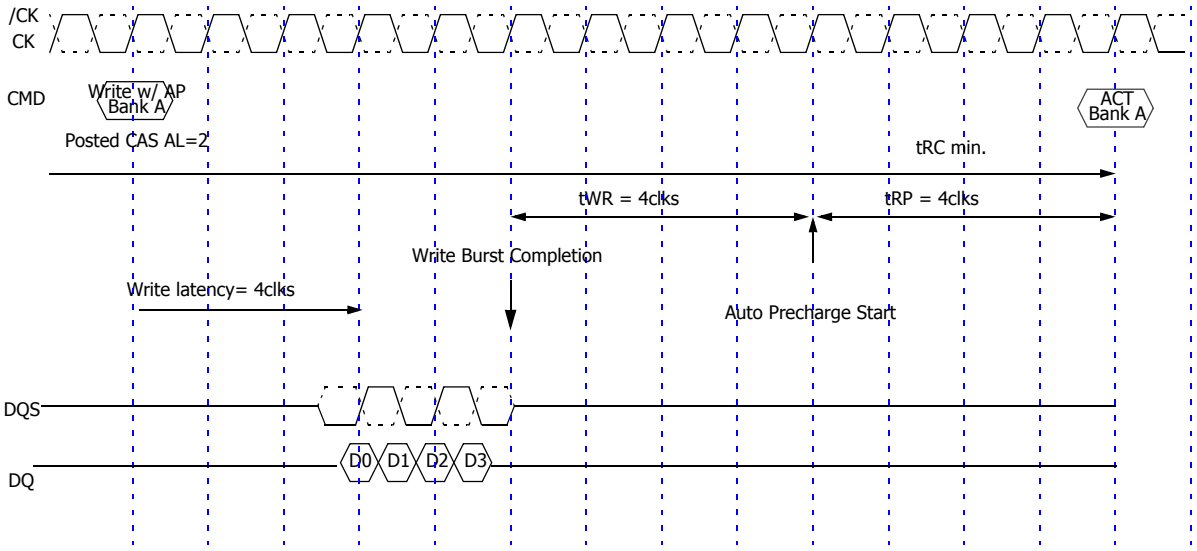

### tRCD=4CLKs, tRP=4CLK, BL=4, CL=4CLKs, AL=2CLKs (tRC limit)



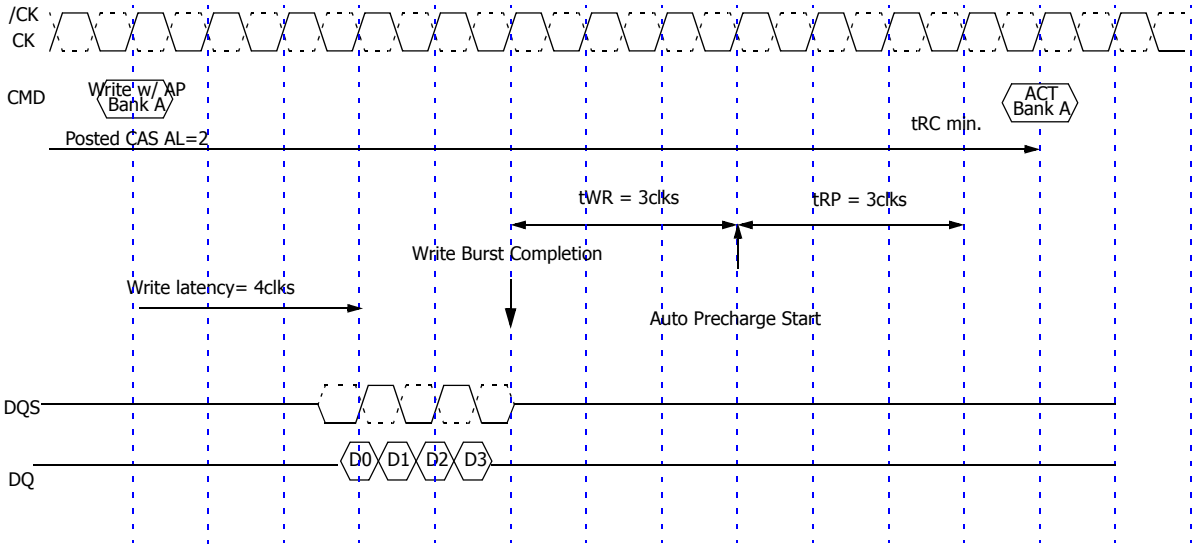
## Write with Auto Precharge

If A10 is high when wrtie command is issued, DRAM perform write with auto precharge. When write with auto precharge command is issued, internal Precharge start automatically. If tRAS minimum is satisfied, internal precharge start at write recovery delay later after the completion of the burst write. If tRAS minimum is not satisfied, internal precharge starting point is delayed until tRAS minimum is satisfied. The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.
1. The data-in to bank activate delay time (tWR+tRP) has been satisfied.
2. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

### CL=3CLKs, AL=2CLKs, BL=4, tWR=4CLKs, tRP=4CLKs (tWR+tRP Limit)

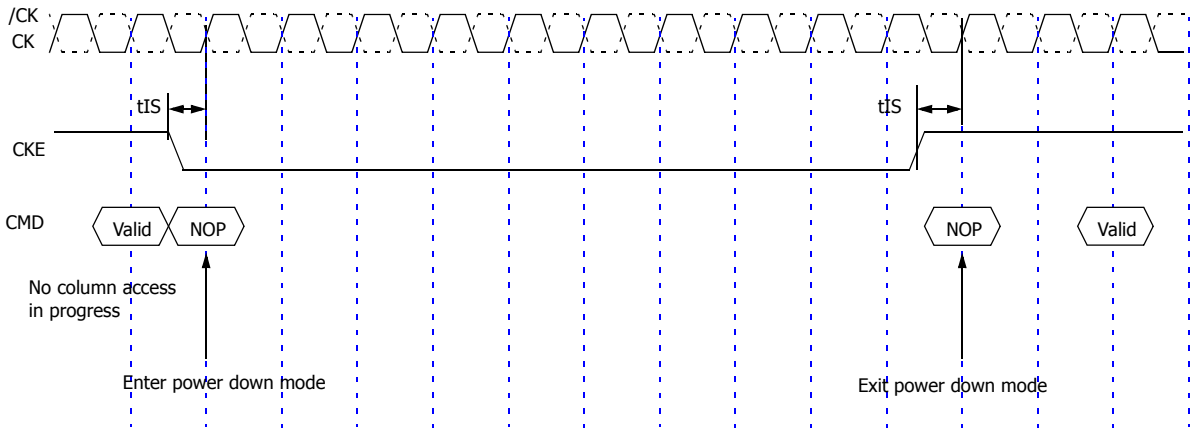



### CL=3CLKs, AL=2CLKs, BL=4, tWR=3CLKs, tRP=4CLKs (tRC limit)



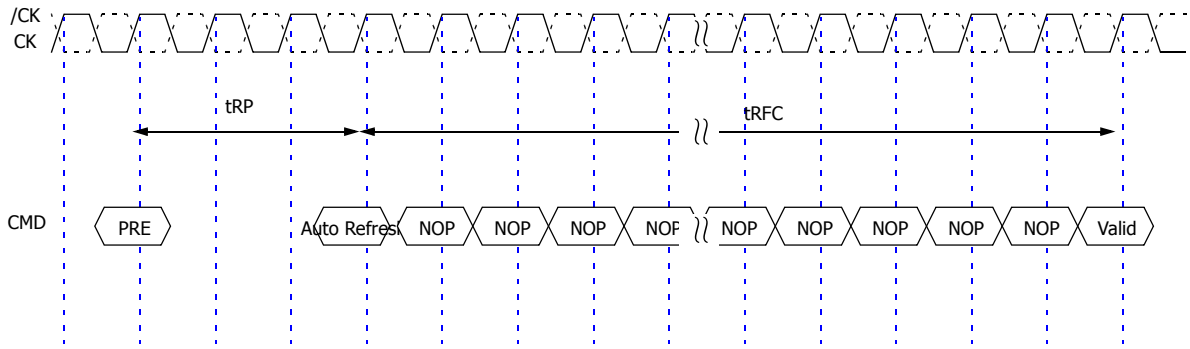
## Power Down

When CKE goes low DDR2 DRAM entered power down mode. If power down command is issued during all bank idle state, DRAM enter precharge power down mode. If power down command is issued when any particular row is active states, DRAM enter active power down mode. Power down command is prohibited during any read or write burst accesses. During power down mode, all input and output buffer is turned off except CK, $\overline{CK}$ and CKE, which means all input signals are Don't care. Power down mode is maintained by keep CKE low. Power-down duration is limited by the refresh requirements of the device. Power down state is synchronously exited when CKE assert high. A valid, executable command may be applied two clock cycles later.



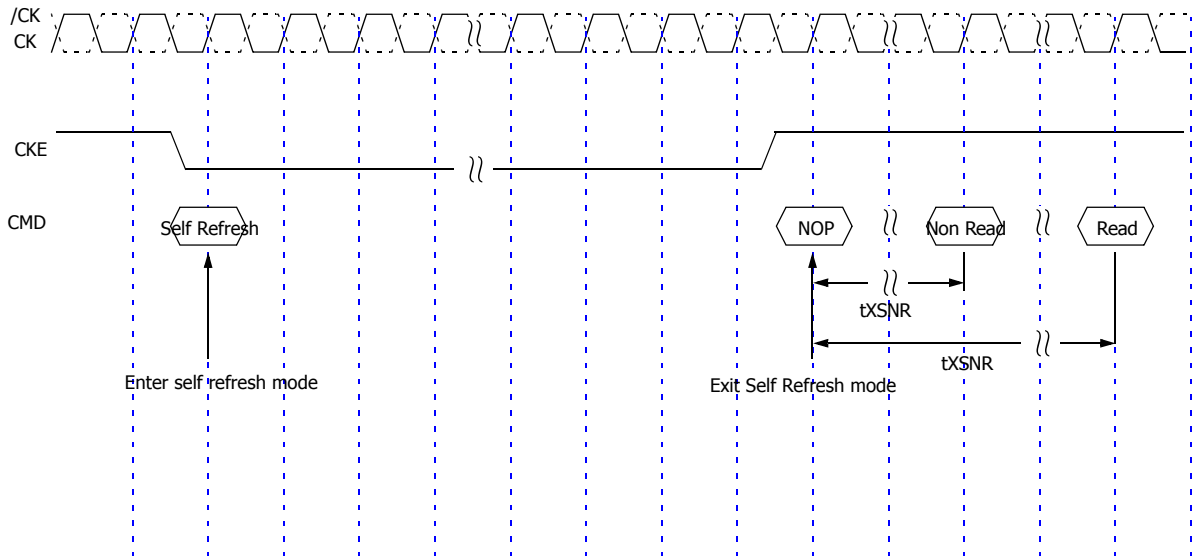
## Auto Refresh

Auto refresh command executes refresh operation with internal address increment. Auto refresh command is issued by activating $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and deactivating $\overline{WE}$ at the rising edge of clock. NOP cycle must be inserted during the entire auto refresh cycle time defined by tRFC. On chip refresh counter is incremented during each refresh cycle. Auto refresh command must be issued each time a refresh is required. The 512Mb DDR2 SDRAM requires auto refresh cycles at an average periodic interval of 7.8 us (maximum) and support internal multi-row refresh operation, which means one auto refresh command executes two internal refresh cycle during tRFC cycle. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. But, a maximum of eight auto refresh commands can be posted. Before entering Auto Refresh mode, all banks must be in a precharge state and Auto refresh command can be issued after tRP period from precharge all command.



## Self Refresh

When auto refresh command with CKE=low is issued, DDR2 DRAM entered self refresh mode. During the self refresh mode, DRAM retain data without external clocking and any external system control. Before issuing Self Refresh command, all banks must be in a precharge state and CKE must be low. All input buffer is turned off except CKE pin, which means all input signals (except CKE) are Don't care during self refresh. On-chip DLL is automatically disabled upon entering self refresh mode. DRAM retains data by internal self refresh operation. Self refresh mode is exit by assering CKE high. Once CKE is high, the DDR2 SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. After self refresh exit, stable input clock should be supplied to DRAM. A minimum of 200 cycles of stable input clock, where CKE is held high, is required to lock the internal DLL circuit of DDR2 SDRAM.



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Case Temperature | TC | TBD | °C |
| Storage Temperature | TSTG | -55 ~ +100 | °C |
| Voltage on Any Pin relative to VSS | VIN, VOUT | -0.5 ~ +2.3 | V |
| Voltage on VDD relative to VSS | VDD | -1.0 ~ +2.3 | V |
| Voltage on VDDQ relative to VSS | VDDQ | -0.5 ~ +2.3 | V |
| Voltage on VDDL relative to VSS | VDDL | -0.5 ~ +2.3 | V |

**Note :** Operation at above absolute maximum rating can adversely affect device reliability

## DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VDD | 1.7 | 1.8 | 1.9 | V | |
| Power Supply Voltage | VDDL | 1.7 | 1.8 | 1.9 | V | |
| Power Supply Voltage | VDDQ | 1.7 | 1.8 | 1.9 | V | 1 |
| Reference Voltage | VREF | 0.49*VDDQ | 0.5*VDDQ | 0.51*VDDQ | V | 3 |
| Input High Voltage | VIH | VREF + 0.125 | - | VDDQ + 0.3 | V | |
| Input Low Voltage | VIL | -0.3 | - | VREF - 0.125 | V | 2 |
| Termination Voltage | VTT | VREF - 0.04 | VREF | VREF + 0.04 | V | |

**Note :**
1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak noise on VREF may not exceed +/- 2% of the dc value.

## DC CHARACTERISTICS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Min. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Leakage Current | ILI | -5 | 5 | uA | 1 |
| Output Leakage Current | ILO | -5 | 5 | uA | 2 |
| Output High Voltage | VOH | TBD | - | V | - |
| Output Low Voltage | VOL | - | TBD | V | - |

**Note** : 1. VIN = 0 to 1.9V, All other pins are not tested under VIN =0V. 2. DOUT is disabled, VOUT=0 to 1.8V

## DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Test Condition | | 400 3/3/3 | 400 4/4/4 | 533 4/4/4 | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Operating Current | IDD0 | One ban; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | | TBD | TBD | TBD | mA | |
| Operating Current | IDD1 | One bank; Active - Read - Precharge; Burst Length=4; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle | | TBD | TBD | TBD | mA | |
| Precharge Power Down Standby Current | IDD2P | All banks idle; Power down mode; CKE=Low, tCK=tCK(min) | | TBD | TBD | TBD | mA | |
| Idle Standby Current | IDD2F | $\overline{CS}$=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM | | TBD | TBD | TBD | mA | |
| Active Power Down Standby Current | IDD3P | One bank active; Power down mode; CKE=Low, tCK=tCK(min) | | TBD | TBD | TBD | mA | |
| Active Standby Current | IDD3N | $\overline{CS}$=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | TBD | TBD | TBD | mA | |
| Operating Current | IDD4R | Burst=4; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA | | TBD | TBD | TBD | mA | |
| Operating Current | IDD4W | Burst=4; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle | | TBD | TBD | TBD | | |
| Auto Refresh Current | IDD5 | tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR 2 at 133Mhz; distributed refresh | | TBD | TBD | TBD | | |
| Self Refresh Current | IDD6 | CKE =< 0.2V; External clock on; tCK=tCK(min) | Normal | TBD | TBD | TBD | mA | |
| | | | Low Power | TBD | TBD | TBD | mA | |
| Operating Current - Four Bank Operation | IDD7 | Four bank interleaving with BL=4, Refer to the following page for detailed test condition | | TBD | TBD | TBD | mA | |

**This Page will be changed by the standardization result of Jedec Committee.**

## DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Test Condition | | 533 5/5/5 | 667 5/5/5 | 667 6/6/6 | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Operating Current | IDD0 | One ban; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | | TBD | TBD | TBD | mA | |
| Operating Current | IDD1 | One bank; Active - Read - Precharge; Burst Length=4; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle | | TBD | TBD | TBD | mA | |
| Precharge Power Down Standby Current | IDD2P | All banks idle; Power down mode; CKE=Low, tCK=tCK(min) | | TBD | TBD | TBD | mA | |
| Idle Standby Current | IDD2F | $\overline{CS}$=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM | | TBD | TBD | TBD | mA | |
| Active Power Down Standby Current | IDD3P | One bank active; Power down mode; CKE=Low, tCK=tCK(min) | | TBD | TBD | TBD | mA | |
| Active Standby Current | IDD3N | $\overline{CS}$=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | TBD | TBD | TBD | mA | |
| Operating Current | IDD4R | Burst=4; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA | | TBD | TBD | TBD | mA | |
| Operating Current | IDD4W | Burst=4; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle | | TBD | TBD | TBD | | |
| Auto Refresh Current | IDD5 | tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR 2 at 133Mhz; distributed refresh | | TBD | TBD | TBD | | |
| Self Refresh Current | IDD6 | CKE =< 0.2V; External clock on; tCK=tCK(min) | Normal | TBD | TBD | TBD | mA | |
| | | | Low Power | TBD | TBD | TBD | mA | |
| Operating Current - Four Bank Operation | IDD7 | Four bank interleaving with BL=4, Refer to the following page for detailed test condition | | TBD | TBD | TBD | mA | |

**This Page will be changed by the standardization result of Jedec Committee.**

## DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7

### IDD1 : Operating current: One bank operation

1. Typical Case : VDD = 1.8V, T=25 °C

2. Worst Case : VDD = 1.9V, T= 10 °C

3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA

4. Timing patterns

   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changingt

     50% of data changing at every burst

   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst

   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

### IDD7 : Operating current: Four bank operation

1. Typical Case : VDD = 1.8V, T=25 °C

2. Worst Case : VDD = 1.9V, T= 10 °C

3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA

4. Timing patterns

   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

**This Page will be changed by the standardization result of Jedec Committee.**

## AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | VIH(AC) | VREF + 0.25 | | V | |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals | VIL(AC) | | VREF - 0.25 | V | |
| Input Differential Voltage, CK and /CK inputs | VID(AC) | TBD | TBD | V | 1 |
| Input Crossing Point Voltage, CK and /CK inputs | VIX(AC) | TBD | TBD | V | 2 |

**Note :**
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

## AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

| Parameter | Value | Unit |
|---|---|---|
| Reference Voltage | VDDQ x 0.5 | V |
| Termination Voltage | VDDQ x 0.5 | V |
| AC Input High Level Voltage (VIH, min) | VREF + 0.25 | V |
| AC Input Low Level Voltage (VIL, max) | VREF - 0.25 | V |
| Input Timing Measurement Reference Level Voltage | VREF | V |
| Output Timing Measurement Reference Level Voltage | VTT | V |
| Input Signal maximum peak swing | 1.5 | V |
| Input minimum Signal Slew Rate | 1 | V/ns |
| Termination Resistor (RT) | TBD | Ω |
| Series Resistor (RS) | TBD | Ω |
| Output Load Capacitance for Access Time Measurement (CL) | TBD | pF |

**This Page will be changed by the standardization result of Jedec Committee.**

## AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | Symbol | 400 3/3/3 | | 400 4/4/4 | | 533 4/4/4 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Row Cycle Time | tRC | 60 | - | 65 | - | 60 | - | ns | |
| Auto Refresh Row Cycle Time | tRFC | 105 | - | 105 | - | 105 | - | ns | * |
| Row Active Time | tRAS | 45 | - | 45 | - | 45 | - | ns | |
| Active to Read with Auto Precharge Delay | tRAP | tRCD min | - | tRCD min | - | tRCD min | - | ns | 16 |
| Row Address to Column Address Delay | tRCD | 15 | - | 20 | - | 15 | - | ns | |
| Row Active to Row Active Delay (2K page size) | tRRD | 10 | | 10 | | 10 | | ns | |
| Row Active to Row Active Delay (1K page size) | | 7.5 | - | 7.5 | - | 7.5 | - | ns | |
| Column Address to Column Address Delay | tCCD | - | - | - | - | - | - | CK | |
| Row Precharge Time | tRP | 15 | - | 20 | - | 15 | - | ns | |
| Write Recovery Time | tWR | 15 | - | 15 | - | 15 | - | ns | * |
| Internal write to Read Command delay | tWTR | 10 | - | 10 | - | 7.5 | - | ns | |
| Auto Precharge Write Recovery + Precharge Time | tDAL | tWR+ tRP | - | tWR+ tRP | - | tWR+ tRP | | CK | 15 |
| System Clock Cycle Time | tCK | 5 | 8 | 5 | 8 | 3.75 | 8 | ns | |
| Clock High Level Width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| Clock Low Level Width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| Data-Out edge to Clock edge Skew | tAC | -600 | 600 | -600 | 600 | -500 | 500 | ps | |
| DQS-Out edge to Clock edge Skew | tDQSCK | -500 | 500 | -500 | 500 | -450 | 450 | ps | |
| DQS-Out edge to Data-Out edge Skew | tDQSQ | - | 350 | - | 350 | - | 300 | ps | |
| Data-Out hold time from DQS | tQH | tHPmin -tQHS | - | tHPmin -tQHS | - | tHPmin -tQHS | - | ps | 1, 10 |
| Clock Half Period | tHP | tCH/L min | - | tCH/L min | - | tCH/L min | - | ps | 1,9 |
| Data Hold Skew Factor | tQHS | - | 450 | - | 450 | - | 400 | ps | 10 |
| Data-out high-Z window from CK, /CK | tHZ | - | 600 | - | 600 | - | 500 | ps | |
| Data-out low-Z window from CK, /CK | tLZ | -600 | 600 | -600 | 600 | -500 | 500 | ps | |
| Input Setup Time (fast slew rate) | tIS | 600 | - | 600 | - | 500 | - | ps | 2,3,5,6 |
| Input Hold Time (fast slew rate) | tIH | 600 | - | 600 | - | 500 | - | ps | 2,3,5,6 |
| Input Pulse Width | tIPW | 0.6 | - | 0.6 | - | 0.6 | - | CK | 6 |
| Write DQS High Level Width | tDQSH | 0.35 | - | 0.35 | - | 0.35 | - | CK | |

| Parameter | Symbol | 400 3/3/3 | | 400 4/4/4 | | 533 4/4/4 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Write DQS Low Level Width | tDQSL | 0.35 | - | 0.35 | - | 0.35 | - | CK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | 0.2 | - | 0.2 | - | CK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | - | 0.2 | - | 0.2 | - | CK | |
| Write Command to First Rising edge of DQS-In | tDQSS | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | CK | |
| Data-In Setup Time to DQS-In (DQ & DM) | tDS | 400 | - | 400 | - | 350 | - | ps | 6,7, 11~13 |
| Data-in Hold Time to DQS-In (DQ & DM) | tDH | 400 | - | 400 | - | 350 | - | ps | 6,7, 11~13 |
| DQ & DM Input Pulse Width | tDIPW | 0.35 | - | 0.35 | - | 0.35 | - | CK | |
| Read DQS Preamble Time | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | CK | |
| Read DQS Postamble Time | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CK | |
| Write DQS Preamble Setup Time | tWPRES | 0 | - | 0 | - | 0 | - | CK | |
| Write DQS Preamble | tWPRE | 0.25 | - | 0.25 | - | 0.25 | - | CK | |
| Write DQS Postamble Time | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CK | |
| Mode Register Set Delay | tMRD | 2 | - | 2 | - | 2 | - | CK | |
| Exit Self Refresh to Any Command | tXSC | 200 | - | 200 | - | | | CK | 8 |
| Exit power down to any non-read command | tXPNR | 2 | - | 2 | - | 2 | - | CK | |
| Exit active power down to read command | tXARD | 2 | - | 2 | - | 2 | - | CK | |
| Exit precharge power down to read command | tXPRD | 6-AL | | 6-AL | | 6-AL | | CK | |
| Average Periodic Refresh Interval | tREFI | - | 7.8 | - | 7.8 | - | 7.8 | us | |

## AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | Symbol | 533 5/5/5 | | 667 5/5/5 | | 667 6/6/6 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Row Cycle Time | tRC | 60 | - | | | | | ns | |
| Auto Refresh Row Cycle Time | tRFC | 105 | - | | | | | ns | |
| Row Active Time | tRAS | 45 | - | | | | | ns | |
| Active to Read with Auto Precharge Delay | tRAP | tRCD min | - | | | | | ns | |
| Row Address to Column Address Delay | tRCD | 18.75 | - | 15 | - | 18 | - | ns | |
| Row Active to Row Active Delay (2K page size) | tRRD | 10 | | 10 | - | 10 | - | ns | |
| Row Active to Row Active Delay (1K page size) | | 7.5 | - | 7.5 | - | 7.5 | - | ns | |
| Column Address to Column Address Delay | tCCD | - | - | | | | | CK | |
| Row Precharge Time | tRP | 18.75 | - | 15 | - | 18 | - | ns | |
| Write Recovery Time | tWR | 15 | - | | - | | - | ns | |
| Internal write to Read Command delay | tWTR | 7.5 | - | 2 | - | 2 | - | ns | |
| Auto Precharge Write Recovery+ Precharge Time | tDAL | tWR+ tRP | | tWR+ tRP | - | tWR+ tRP | - | CK | |
| System Clock Cycle Time | tCK | 3.75 | 8 | 3 | 8 | 3 | 8 | ns | |
| Clock High Level Width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| Clock Low Level Width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| Data-Out edge to Clock edge Skew | tAC | -500 | 500 | | | | | ps | |
| DQS-Out edge to Clock edge Skew | tDQSCK | -450 | 450 | | | | | ps | |
| DQS-Out edge to Data-Out edge Skew | tDQSQ | - | 300 | - | | - | | ps | |
| Data-Out hold time from DQS | tQH | tHPmin -tQHS | - | tHPmin -tQHS | - | tHPmin -tQHS | - | ps | |
| Clock Half Period | tHP | tCH/L min | - | tCH/L min | - | tCH/L min | - | ps | |
| Data Hold Skew Factor | tQHS | - | 400 | | | | | ps | |
| Data-out high-Z window from CK, /CK | tHZ | - | 500 | - | tAC max | - | tAC max | ps | |
| Data-out low-Z window from CK, /CK | tLZ | -500 | 500 | tAC min | tAC max | tAC min | tAC max | ps | |
| Input Setup Time(fast slew rate) | tIS | 500 | - | | - | | - | ps | |
| Input Hold Time (fast slew rate) | tIH | 500 | - | | - | | - | ps | |
| Input Pulse Width | tIPW | 0.6 | - | 0.6 | - | 0.6 | - | CK | |

| Parameter | Symbol | 533 5/5/5 | | 667 5/5/5 | | 667 6/6/6 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Write DQS High Level Width | tDQSH | 0.35 | - | 0.35 | - | 0.35 | - | CK | |
| Write DQS Low Level Width | tDQSL | 0.35 | - | 0.35 | - | 0.35 | - | CK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | 0.2 | - | 0.2 | - | CK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | - | 0.2 | - | 0.2 | - | CK | |
| Write Command to First Rising edge of DQS-In | tDQSS | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | CK | |
| Data-In Setup Time to DQS-In(DQ & DM) | tDS | 350 | - | | - | | - | ps | |
| Data-In Hold Time to DQS-In(DQ & DM) | tDH | 350 | - | | - | | - | ps | |
| DQ & DM Input Pulse Width | tDIPW | 0.35 | - | 0.35 | - | 0.35 | - | CK | |
| Read DQS Preamble Time | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | CK | |
| Read DQS Postamble Time | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CK | |
| Write DQS Preamble Setup Time | tWPRES | 0 | - | 0 | - | 0 | - | CK | |
| Write DQS Preamble | tWPRE | 0.25 | - | 0.25 | - | 0.25 | - | CK | |
| Write DQS Postamble Time | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CK | |
| Mode Register Set Delay | tMRD | 2 | - | 2 | - | 2 | - | CK | |
| Exit Self Refresh to Any Command | tXSC | | | | | | | CK | |
| Exit Power Down to Any non-read Command | tXPNR | 2 | - | | | | | CK | |
| Exit Active Power down to read Command | tXARD | 2 | - | 2 | - | 2 | - | CK | |
| Exit Precharge Power down to read Command | tXPRD | 6-AL | | | | | | CK | |
| Average Periodic Refresh Interval | tREFI | - | 7.8 | | | | | us | |

**Note :**

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A13, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
   This derating table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
   Input Setup / Hold Slew-rate Derating Table.

| Input Setup / Hold Slew-rate | Delta tIS | Delta tIH |
|---|---|---|
| V/ns | ps | ps |
| 0.5 | 0 | 0 |
| 0.4 | +50 | 0 |
| 0.3 | +100 | 0 |

5. CK, /CK slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(LDQS, UDQS) : DQ, LDM/UDM.
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects and p-channel to n-channel variation of the output drivers.
11. This derating table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.
    Input Setup / Hold Slew-rate Derating Table.

| Input Setup / Hold Slew-rate | Delta tDS | Delta tDH |
|---|---|---|
| V/ns | ps | ps |
| 0.5 | 0 | 0 |
| 0.4 | +75 | +75 |
| 0.3 | +150 | +150 |

12. I/O Setup/Hold Plateau Derating. This derating table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

| I/O Input Level | Delta tDS | Delta tDH |
|---|---|---|
| mV | ps | ps |
| +280 | +50 | +50 |

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This derating table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as (1/SlewRate1)-(1/SlewRate2). For example, if slew rate 1 = 0.5V/ns and Slew Rate2 = 0.4V/n then the Delta Inverse Slew Rate = -0.5ns/V.

| (1/SlewRate1)-(1/SlewRate2) | Delta tDS | Delta tDH |
|---|---|---|
| ns/V | ps | ps |
| 0 | 0 | 0 |
| +/-0.25 | +50 | +50 |
| +/- 0.5 | +100 | +100 |

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. tDAL = (tDPL / tCK ) + (tRP / tCK ). For each of the terms above, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
    Example: For DDR266B at CL=2.5 and tCK = 7.5 ns,
    tDAL = (15 ns / 7.5 ns) + (20 ns / 7.5 ns) = (2.00) + (2.67)
    Round up each non-integer to the next highest integer: = (2) + (3), tDAL = 5 clocks
16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be tRAS - BL/2 x tCK.

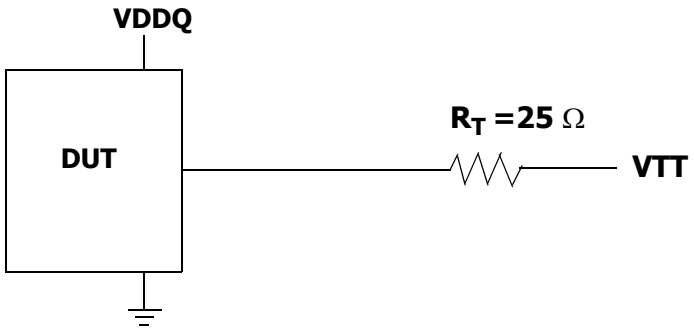
**The previous and This Page will be changed by the standardization result of Jedec Committee.**

## CAPACITANCE (TA=25°C, f=100MHz )

| Parameter | Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Clock Capacitance | CK, $\overline{CK}$ | CCK | 1.5 | 2.5 | pF |
| Delta Input Clock Capacitance | CK, $\overline{CK}$ | CDCK | - | 0.25 | pF |
| Input Capacitance | All other input-only pins | CI | 1.5 | 2.5 | pF |
| Delta Input Capacitance | All other input-only pins | CDI | - | 0.25 | pF |
| Input / Output Capacitance | DQ, DQS, DM | CIO | 3.0 | 4.0 | pF |
| Delta Input / Output Capacitance | DQ, DQS, DM | CDIO | - | 0.5 | pF |

**Note :**
1. VDD = min. to max., VDDQ = 1.7V to 1.9V, VODC = VDDQ/2, VOpeak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

## OUTPUT LOAD CIRCUIT



## OUTPUT DRIVE CHARACTERISTICS (FULL STRENGTH DRIVER)

| Voltage | Pull Down Current (mA) | | | | Pull Up Current (mA) | | | |
|---|---|---|---|---|---|---|---|---|
| | Nominal Low | Nominal High | Min. | Max. | Nominal Low | Nominal High | Min. | Max. |
| 0.1 | | | | | | | | |
| 0.2 | | | | | | | | |
| 0.3 | | | | | | | | |
| 0.4 | | | | | | | | |
| 0.5 | | | | | | | | |
| 0.6 | | | | | | | | |
| 0.7 | | | | | | | | |
| 0.8 | | | | | | | | |
| 0.9 | | | | | | | | |
| 1.0 | | | | | | | | |
| 1.1 | | | | | | | | |
| 1.2 | | | | | | | | |
| 1.3 | | | | | | | | |
| 1.4 | | | | | | | | |
| 1.5 | | | | | | | | |
| 1.6 | | | | | | | | |
| 1.7 | | | | | | | | |
| 1.8 | | | | | | | | |
| 1.9 | | | | | | | | |
| 2.0 | | | | | | | | |
| 2.1 | | | | | | | | |
| 2.2 | | | | | | | | |
| 2.3 | | | | | | | | |
| 2.4 | | | | | | | | |
| 2.5 | | | | | | | | |
| 2.6 | | | | | | | | |
| 2.7 | | | | | | | | |

Evaluation conditions:

Typical 25 °C (TAmbient), VDDQ=1.8V, typical process

Minimum 70 °C (TAmbient), VDDQ=1.7V, slow slow process

Maximum 0 °C (TAmbient), VDDQ=1.9V, fast fast process

## OUTPUT DRIVE CHARACTERISTICS (FULL STRENGTH DRIVER )