

## RICMOS™ LOW POWER SOI GATE ARRAYS

## HLX2000 FAMILY

### FEATURES

- Optimized for Ultra Low Power Applications
- Fabricated on Honeywell's Radiation Hardened 0.55  $\mu\text{m}_{\text{Leff}}$  RICMOS™ IV SOI Process
- Array Sizes from 15K to 600K Available Gates
- Supports 3.3V and/or 2.5V Operation
- Mixed Voltage CMOS Compatible I/O Buffers
- Single or dual Port Custom SRAM Drop-In Capability
- Supports System Speeds Beyond 50 MHz
- Supports Chip Level Power Down for Cold Sparring
- Total Dose Hardness  $\geq 1 \times 10^6$  rad(SiO<sub>2</sub>)
- Soft Error Rate  $\leq 1 \times 10^{-9}$  Errors/Bit-Day\*
- No Latchup

\*Projected

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### GENERAL DESCRIPTION

The HLX2000 gate arrays are low power sea-of-transistor arrays, fabricated on Honeywell's 0.55  $\mu\text{m}$  RICMOS™ IV Silicon On Insulator (SOI) low voltage process. High density is achieved with the standard 3-layer metal or optional 4-layer metal process, providing up to 310,000 usable gates. The high density and performance characteristics of the RICMOS (Radiation Insensitive CMOS) SOI process make possible device operation beyond 50 MHz over the full military temperature range, even after exposure to ionizing radiation exceeding  $1 \times 10^6$  rad(SiO<sub>2</sub>). Flip-Flops have been designed for a Soft Error Rate (SER) of less than  $1 \times 10^{-9}$  errors/bit/day in the Adams 90% worst case environment.

Each HLX2000 design is founded on our proven RICMOS ASIC library of SSI and MSI logic elements, custom RAM cells and selectable I/O pads. These low power gate arrays feature a global clock network capable of handling multiple clock signals with low clock skew between registers. This family is fully compatible with Honeywell's high reliability screening procedures and consistent with QML Class Q and V requirements.

Designers can choose from a wide variety of I/O types. Output buffer options include 8 drive strengths, IEEE 1149.1 boundary scan, pull-up/pull-down resistors, and three-state capability. Input buffers can be selected with IEEE 1149.1 boundary scan, and pull-up/pull-down resistors. Bi-directional buffers are also available.

Another important feature is the dual voltage I/O capability in which the designer has complete flexibility in terms of placement of I/O buffers. This feature allows adjacent I/O buffers with different supply voltages.

The HLX2000 family provides options for custom drop-in SRAM macrocells. Word widths can be selected in two bit increments. Single port and two port options are available.

The HLX2000 family has a special feature to allow a chip level power down mode, in which the associated buses connected to the chip can remain active. This high impedance off-state buffer feature allows users to power down portions of their system for power savings or for cold sparing.

Logic designers need not have prior experience in radiation hardening. Honeywell's VDS™ Toolkit and RICMOS IV SOI libraries provide the necessary guidance to achieve first pass design success. The VDS Toolkit supports industry standard platforms including those offered by Mentor Graphics and Synopsys.

Honeywell can perform design translations to the HLX2000 arrays from other CAD platforms. Our synthesis capabilities allow customers to use familiar CAD tools and libraries to map the existing designs to Honeywell library components.

# HLX2000

HLX2000 Characteristics	HLX2015	HLX2060*	HLX2120*	HLX2240	HLX2450	HLX2600*	
Total Core Gate Count	15K	60K	120K	250K	468K	600K	
Usable Gate Count	3-Layer Metal 4-Layer Metal (1)	10K 13K	32K 42K	57K 77K	108K 143K	180K 244K	225K 310K
Maximum Die I/O	56	132	176	240	336	372	
Maximum Package I/O (2)	56	120	176	240	320	320	
Typical Delay—2 Input NAND	410 ps at 3.3V, 500 ps at 2.5V						
Selectable I/O	Driver, Receiver, Bi-Directional, Three-State						
I/O Interface Levels	CMOS						
Typical Power Dissipation, $\mu$ W/Gate/MHz	0.15 @ 3.3V, 0.08 @ 2.5V						
Operating Voltage	3.3V $\pm$ 10% (Core and I/O) 2.5V $\pm$ 5% (Core and I/O)						
Operating Temperature	-55° C to 125° C						
Process Technology	RICMOS™ IV SOI						
Minimum Geometry	0.55 $\mu$ m $L_{eff}$ / 0.7 $\mu$ m drawn						

(1) Projected  
(2) Design and package dependent

\*Planned Arrays

The HLX2000 family of gate arrays is the right choice for your high reliability applications demanding low power and high radiation hardness.

To learn more about Honeywell's variety of space components, call us at 612-954-2888.

**To learn more about Honeywell Solid State Electronics Center, visit our web site at <http://www.ssec.honeywell.com>**

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