# HT23C128

## CMOS 16K×8-Bit Mask ROM

### Features

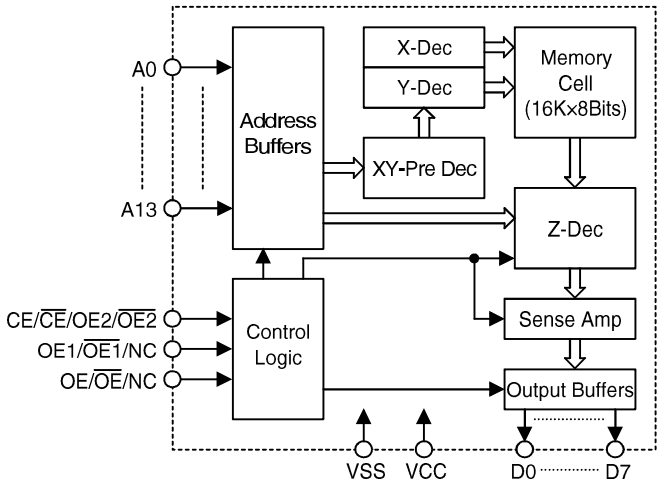
- Operating voltage: 2.7V~5.5V
- Low power consumption
  - Operation: 25mA Max. ($V_{CC}$=5V)
    10mA Max. ($V_{CC}$=3V)
  - Standby: 30μA Max. ($V_{CC}$=5V)
    10μA Max. ($V_{CC}$=3V)
- Access time:150ns Max. ($V_{CC}$=5V)
  250ns Max. ($V_{CC}$=3V)
- 16384×8 bits of mask ROM
- Mask options: chip enable CE/$\overline{CE}$/OE2/$\overline{OE2}$ and output enable OE/$\overline{OE}$/NC & OE1/$\overline{OE1}$/NC
- TTL compatible inputs and outputs
- Tristate outputs
- Fully static operation
- Package type: 28-pin DIP/SOP

### General Description

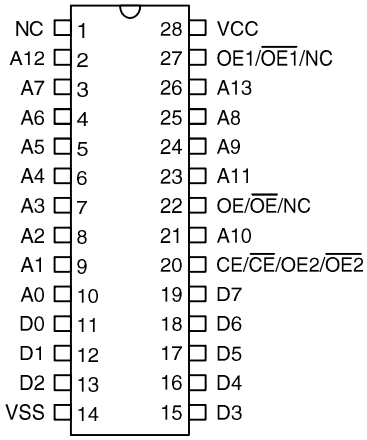
The HT23C128 is a read-only memory with high performance CMOS storage device whose 128K of memory is arranged into 16384 words by 8 bits.

For application flexibility, the chip enable and output enable control pins can be selected as active high or active low. This flexibility not only allows easy interface with most microprocessors, but also eliminates bus contention in multiple bus microprocessor systems. An additional feature of the HT23C128 is its ability to enter the standby mode whenever the chip enable (CE/$\overline{CE}$) is inactive, thus reducing current consumption to below 30μA. The combination of these functions makes the chip suitable for high density low power memory applications.

### Block Diagram



## Pin Assignment




**HT23C128**
**– 28 DIP/SOP**

## Pin Description

| Pin Name | I/O | Description |
|---|---|---|
| NC | — | No connection |
| A0~A13 | I | Address inputs |
| D0~D7 | O | Data outputs |
| VSS | I | Negative power supply |
| CE/$\overline{\text{CE}}$/OE2/$\overline{\text{OE2}}$ | I | Chip enable/Output enable input |
| OE/$\overline{\text{OE}}$/NC | I | Output enable input |
| OE1/$\overline{\text{OE1}}$/NC | I | Output enable input |
| VCC | I | Positive power supply |

## Operation Truth Table

| Mode | CE/$\overline{\text{CE}}$ | OE/$\overline{\text{OE}}$ | OE1/$\overline{\text{OE1}}$ | A0~A13 | D0~D7 |
|---|---|---|---|---|---|
| Read | H/L | H/L | H/L | Valid | Data Out |
| Deselect | H/L | L/H | X | X | High Z |
| Deselect | H/L | X | L/H | X | High Z |
| Standby | L/H | X | X | X | High Z |

Note: H=$V_{IH}$, L=$V_{IL}$, X=$V_{IH}$ or $V_{IL}$

## Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6V
Input Voltage..... –0.3V to $V_{CC}$+0.3V
Storage Temperature..... –50°C to 125°C
Operating Temperature..... –40°C to 85°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## D.C. Characteristics

**Supply voltage: 2.7V~3.6V** Ta=–40°C to 85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ | Conditions | | | | |
| $V_{CC}$ | Operating Voltage | — | — | 2.7 | — | 3.6 | V |
| $I_{CC}$ | Operating Current | 3V | O/P Unload, f=5MHz | — | — | 10 | mA |
| $V_{IL}$ | Input Low Voltage | 3V | — | $V_{SS}$ | — | 0.4 | V |
| $V_{IH}$ | Input High Voltage | 3V | — | 2.0 | — | $V_{CC}$ | V |
| $V_{OL}$ | Output Low Voltage | 3V | $I_{OL}$=2.1mA | — | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | 3V | $I_{OH}$=–0.4mA | 2.4 | — | $V_{CC}$ | V |
| $I_{LI}$ | Input Leakage Current | 3V | $V_{IN}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{LO}$ | Output Leakage Current | 3V | $V_{OUT}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{STB1}$ | Standby Current | 3V | $\overline{CE}$=$V_{IL}$<br>$\overline{CE}$=$V_{IH}$ | — | — | 500 | μA |
| $I_{STB2}$ | Standby Current | 3V | $\overline{CE}$≤0.2V<br>$\overline{CE}$≥$V_{CC}$-0.2V | — | — | 10 | μA |
| $C_{IN}$ | Input Capacitance (See note) | — | f=1MHz | — | — | 10 | pF |
| $C_{OUT}$ | Output Capacitance (See note) | — | f=1MHz | — | — | 10 | pF |

Note: These parameters are periodically sampled but not 100% tested.

**Supply voltage: 4.5V~5.5V** Ta=–40°C to 85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ | Conditions | | | | |
| $V_{CC}$ | Operating Voltage | — | — | 4.5 | — | 5.5 | V |
| $I_{CC}$ | Operating Current | 5V | O/P Unload, f=5MHz | — | — | 25 | mA |
| $V_{IL}$ | Input Low Voltage | 5V | — | $V_{SS}$ | — | 0.8 | V |
| $V_{IH}$ | Input High Voltage | 5V | — | 2.2 | — | $V_{CC}$ | V |

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ | Conditions | | | | |
| $V_{OL}$ | Output Low Voltage | 5V | $I_{OL}$=3.2mA | — | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | 5V | $I_{OH}$=−1mA | 2.4 | — | $V_{CC}$ | V |
| $I_{LI}$ | Input Leakage Current | 5V | $V_{IN}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{LO}$ | Output Leakage Current | 5V | $V_{OUT}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{STB1}$ | Standby Current | 5V | $\overline{CE}$=$V_{IL}$<br>$\overline{CE}$=$V_{IH}$ | — | — | 1.5 | mA |
| $I_{STB2}$ | Standby Current | 5V | $\overline{CE}$≤0.2V<br>$\overline{CE}$≥$V_{CC}$-0.2V | — | — | 30 | μA |
| $C_{IN}$ | Input Capacitance (See note) | — | f=1MHz | — | — | 10 | pF |
| $C_{OUT}$ | Output Capacitance (See note) | — | f=1MHz | — | — | 10 | pF |

Note: These parameters are periodically sampled but not 100% tested.

## A.C. Characteristics

Ta=−40°C to 85°C

| Symbol | Parameter | $V_{CC}$=2.7V~3.6V | | $V_{CC}$=4.5V~5.5V | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CYC}$ | Cycle Time | 250 | — | 150 | — | ns |
| $t_{AA}$ | Address Access Time | — | 250 | — | 150 | ns |
| $t_{ACE}$ | Chip Enable Access Time | — | 250 | — | 150 | ns |
| $t_{AOE}$ | Output Enable Access Time | — | 150 | — | 80 | ns |
| $t_{OH}$ | Output Hold Time | — | — | 10 | — | ns |
| $t_{OD}$ | Output Disable Time (See Note) | — | — | — | 70 | ns |
| $t_{OE}$ | Output Enable Time (See Note) | — | — | 10 | — | ns |

Note: These parameters are periodically sampled but not 100% tested.

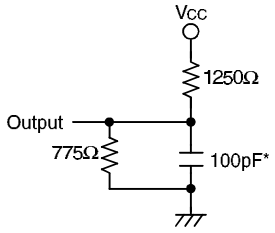
### A.C. test conditions

Output load: see figure right

Input rise and fall time: 10ns

Input pulse levels: 0.4V to 2.4V

Input and output timing reference levels:
0.8V and 2.0V ($V_{CC}$=5V)
1.5V ($V_{CC}$=3V)




* Including scope and jig

Output load circuit

## Functional Description

The HT23C128 has two modes, namely data read mode and standby mode, controlled by CE/$\overline{CE}$/OE2/$\overline{OE2}$, OE/$\overline{OE}$/NC and OE1/$\overline{OE1}$/NC inputs.

- Standby mode

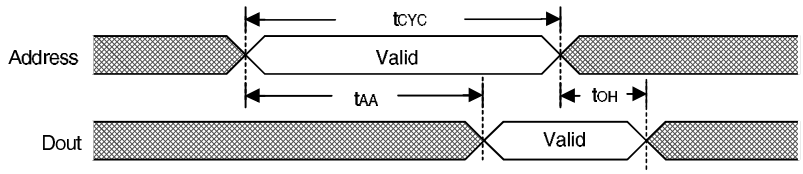
  The HT23C128 has lower current consumption, controlled by the chip enable input (CE/$\overline{CE}$). When a low/high level is applied to the CE/CEB input regardless of the output enable (OE/$\overline{OE}$/NC and OE1/$\overline{OE1}$/NC) states, the chip will enter the standby mode.

- Data read mode

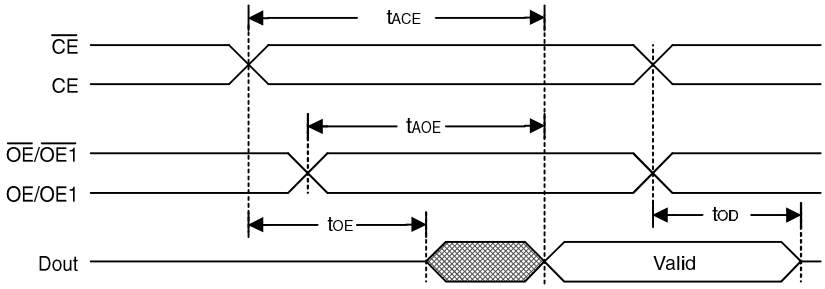
  When both the chip enable (CE/$\overline{CE}$/OE2/$\overline{OE2}$) and the output enable (OE/$\overline{OE}$/NC and OE1/$\overline{OE1}$/NC) are active, the chip is in data read mode. Otherwise, active CE/$\overline{CE}$ and inactive OE/$\overline{OE}$/NC or OE1/$\overline{OE1}$/NC result in deselect mode. The output will remain in Hi-Z state.

## Timing Diagrams

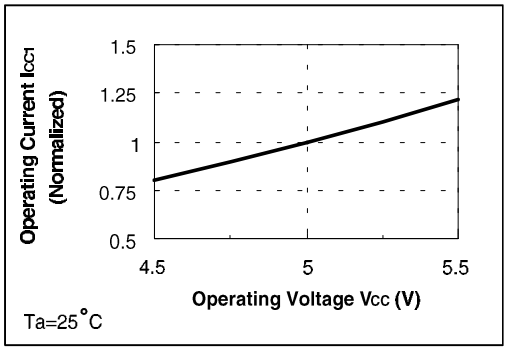
- Propagation delay due to address (CE/$\overline{CE}$/OE2/$\overline{OE2}$, OE/$\overline{OE}$ and OE1/$\overline{OE1}$ are active)

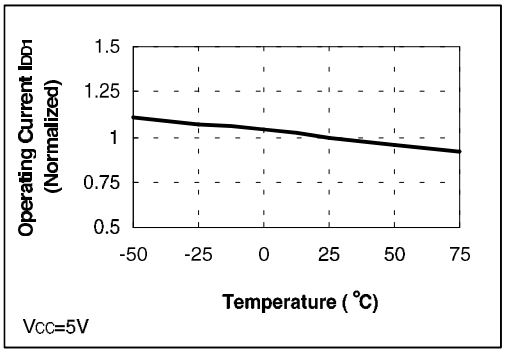


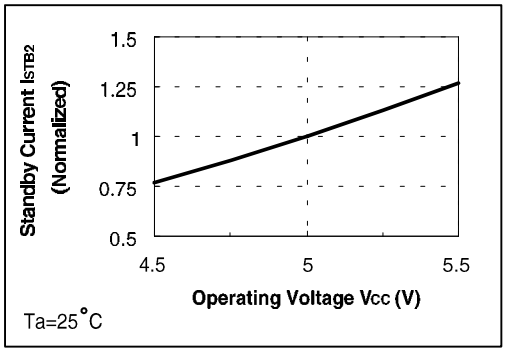

- Propagation delay due to chip enable and output enable (address valid)

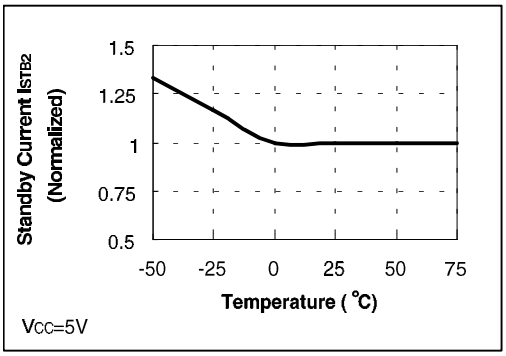


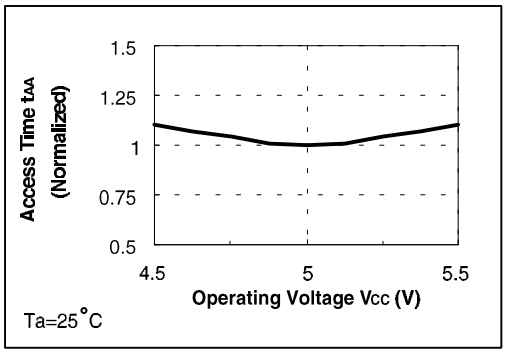
## Characteristic Curves

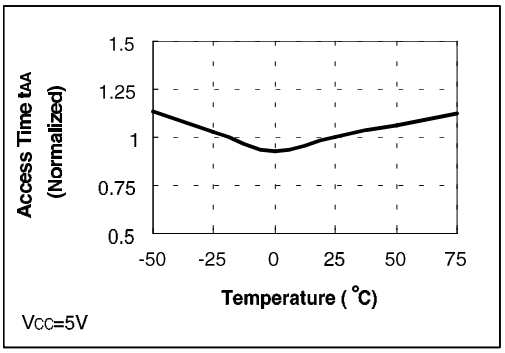


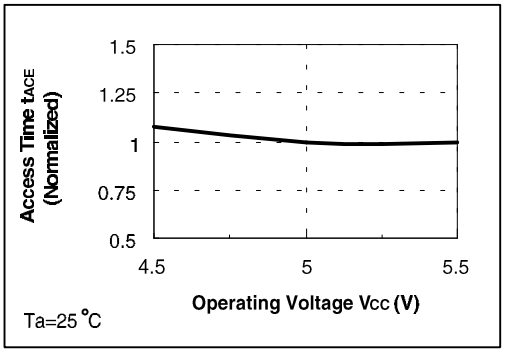



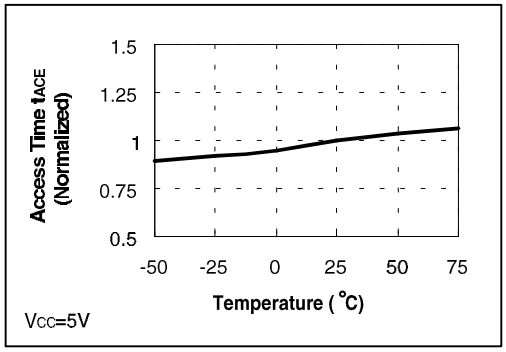



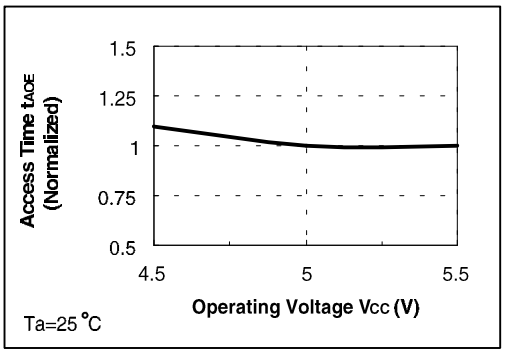



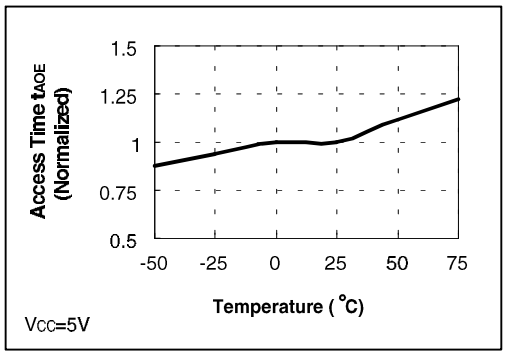




Access Time tACE (Normalized)
1.5
1.25
1
0.75
0.5
4.5
5
5.5
Operating Voltage Vcc (V)
Ta=25°C


Access Time tACE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
Temperature (°C)
VCC=5V


Access Time tACE (Normalized)
1.5
1.25
1
0.75
0.5
4.5
5
5.5
Operating Voltage Vcc (V)
Ta=25°C


Access Time tAOE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
Temperature (°C)
VCC=5V

# HT23C128 MASK ROM ORDERING SHEET

**Custom:**_____

**Input Medium:**

☐ **EPROM** ☐ **DISK** ☐ **File (Mail Address: romfile@holtek.com.tw)** ☐ **OTHER**_____

| User No. | Type/Ref. Name | Q'ty | Check Sum | Memory Address | |
|---|---|---|---|---|---|
| | | | | Start | End |
| | | | | | |

**Control Pin and Package Form Option:**

**(a) 28 Pin Type Pin 20:**_____ **(1) CE (2)** $\overline{\text{CE}}$ **(3) OE2 (4)** $\overline{\text{OE2}}$

**Pin 22:**_____ **(1) OE (2)** $\overline{\text{OE}}$ **(3) NC**

**Pin 27:**_____ **(1) OE1 (2)** $\overline{\text{OE1}}$ **(3) NC**

**(b) Package Form:**_____ **(1) Chip Form (2) 28 DIP (3) 28 SOP**

**Companion User No.**_____

**Package Marking :**_____

**Delivery Date :**_____ **Q'ty:** _____

**CUSTOM CONFIRMED BY:**

_____

**(NAME, DATE, POSITION & CO. CHOP)**

**HOLTEK CONFIRMED BY:**

_____ _____

**(SALES)** **(SALES MANAGER)**