

GaAs InGaP HBT MMIC POWER AMPLIFIER, 5.0 - 7.0 GHz

Typical Applications

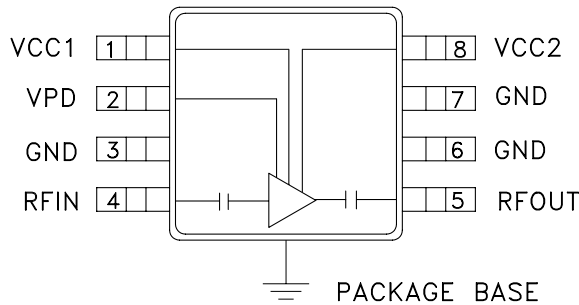
This amplifier is ideal for use as a power amplifier for 5.0 - 7.0 GHz applications:

- UNII
- HiperLAN

Features

- Gain: 15 dB
- Saturated Power: +29 dBm
- 28% PAE
- Supply Voltage: +5.0 V
- Power Down Capability
- No External Matching Required

Functional Diagram



General Description

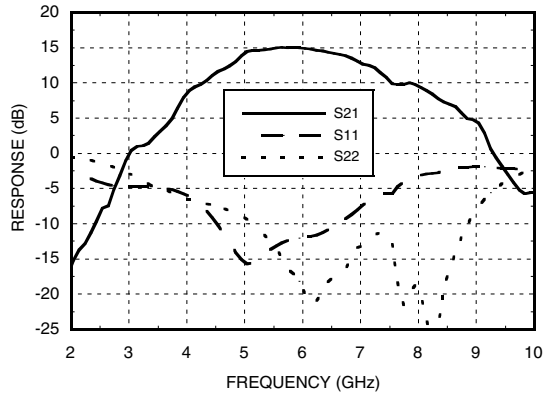
The HMC407MS8G is a high efficiency GaAs InGaP Heterojunction Bipolar Transistor (HBT) MMIC Power amplifier which operates between 5 and 7 GHz. The amplifier requires no external matching to achieve operation and is thus truly 50 Ohm matched at input and output. The amplifier is packaged in a low cost, surface mount 8 leaded package with an exposed base for improved RF and thermal performance. The amplifier provides 15 dB of gain, +29 dBm of saturated power at 28% PAE from a +5.0V supply voltage. Power down capability is available to conserve current consumption when the amplifier is not in use.

Electrical Specifications, $T_A = +25^\circ C$, $V_s = 5V$, $V_{pd} = 5V$

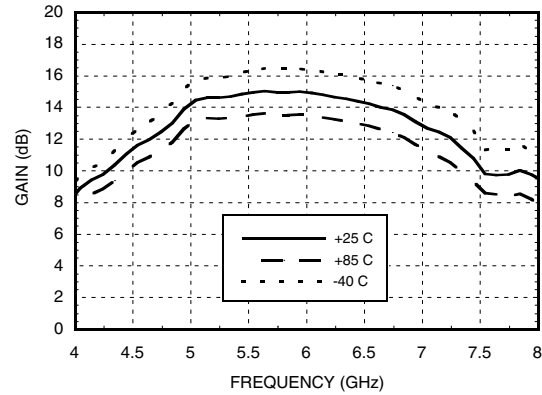
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range	5.0 - 7.0			5.6 - 6.0			GHz
Gain	10	15	18	12	15	18	dB
Gain Variation Over Temperature		0.025	0.035		0.025	0.035	dB/ °C
Input Return Loss		12			12		dB
Output Return Loss		15			15		dB
Output Power for 1 dB Compression (P1dB)	21	25		22	25		dBm
Saturated Output Power (Psat)		29			29		dBm
Output Third Order Intercept (IP3)	32	37		36	40		dBm
Noise Figure		5.5			5.5		dB
Supply Current (Icq)	Vpd = 0V/5V		0.002 / 230	0.002 / 230			mA
Control Current (Ipd)	Vpd = 5V		7	7			mA
Switching Speed	tON, tOFF		30	30			ns

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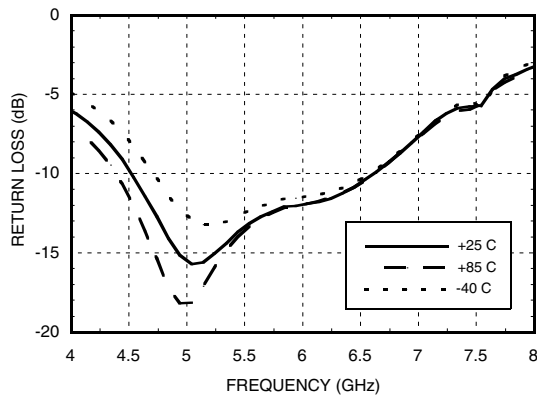
Broadband Gain & Return Loss



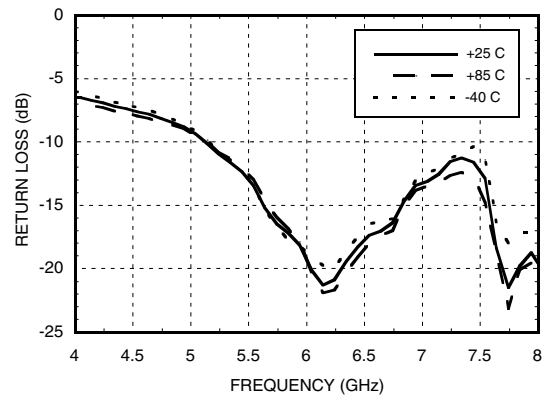
Gain vs. Temperature



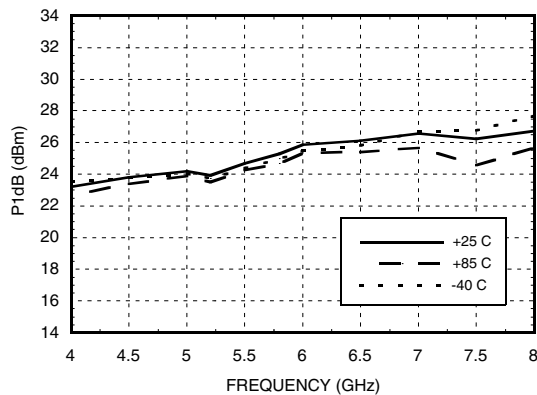
Input Return Loss vs. Temperature



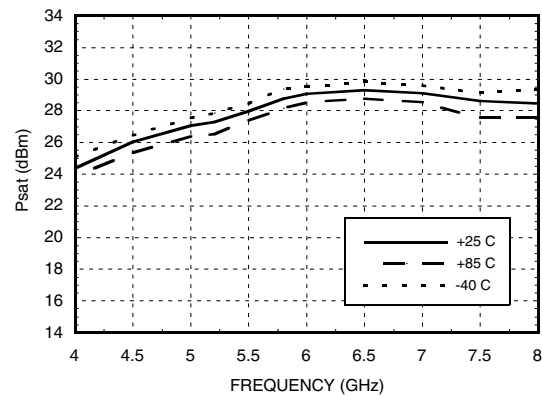
Output Return Loss vs. Temperature



P1dB vs. Temperature

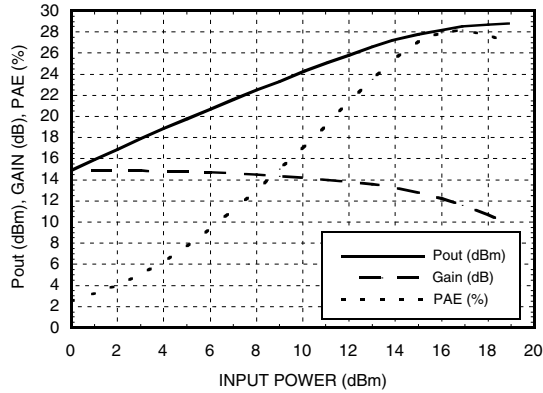


Psat vs. Temperature

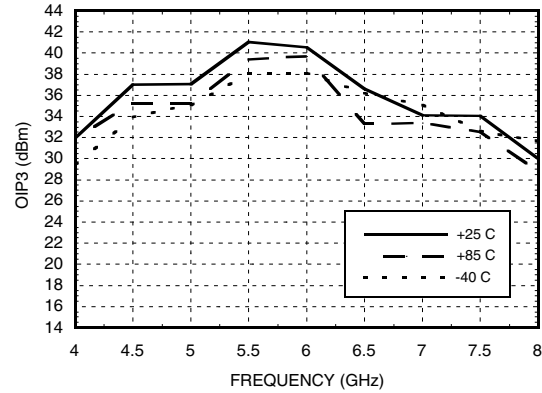


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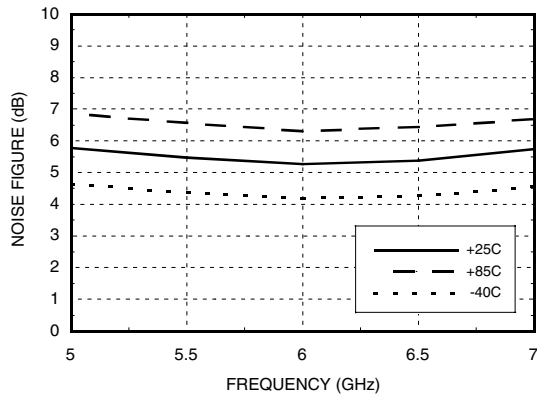
Power Compression @ 5.8 GHz



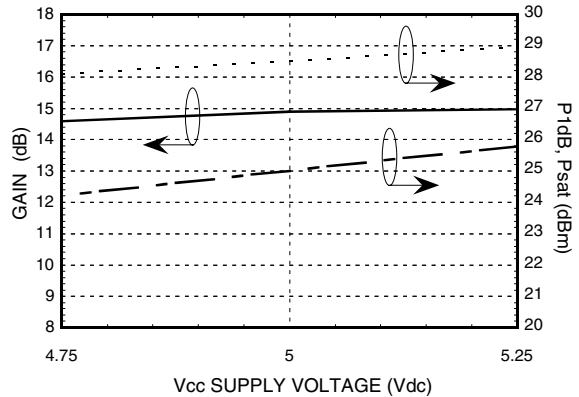
Output IP3 vs. Temperature



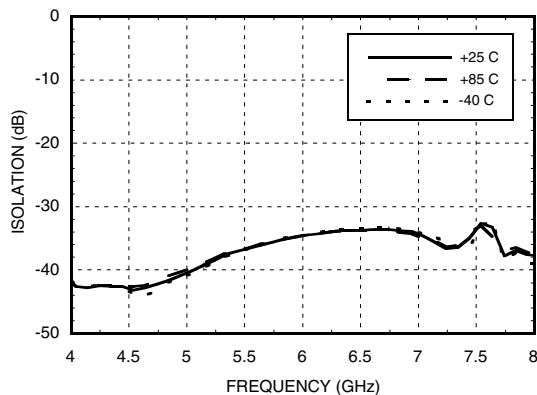
Noise Figure vs. Temperature



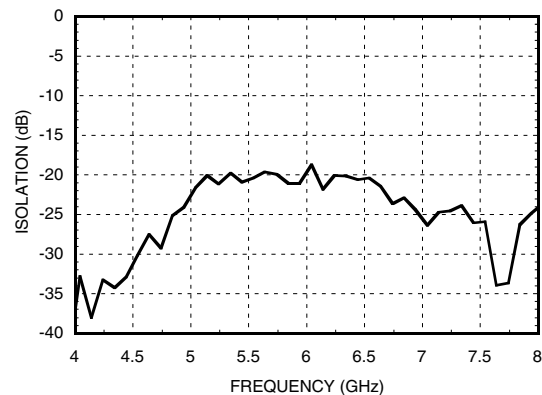
Gain & Power vs. Supply Voltage



Reverse Isolation vs. Temperature

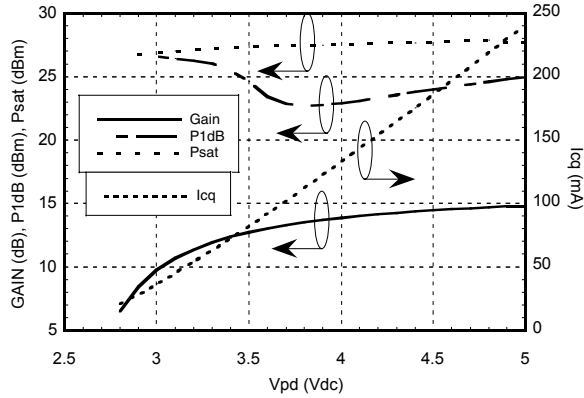


Power Down Isolation



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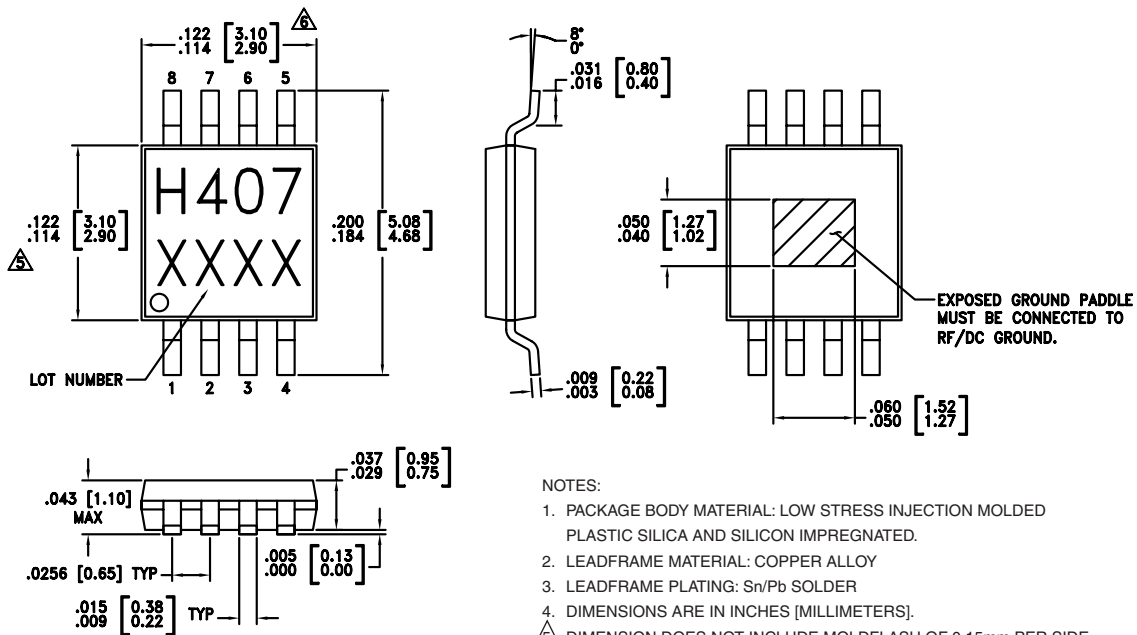
Gain, Power & Quiescent Supply Current vs. Vpd @ 5.8 GHz



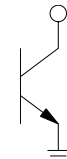
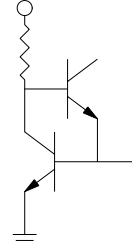



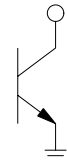
Absolute Maximum Ratings

Collector Bias Voltage (Vcc1, Vcc2)	+5.5 Vdc
Control Voltage (Vpd)	+5.5 Vdc
RF Input Power (RFin)(Vs = Vpd = +5.0 Vdc)	+20 dBm
Junction Temperature	150 °C
Continuous Pdis (T = 85 °C) (derate 31 mW/°C above 85 °C)	2 W
Thermal Resistance (junction to ground paddle)	32 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

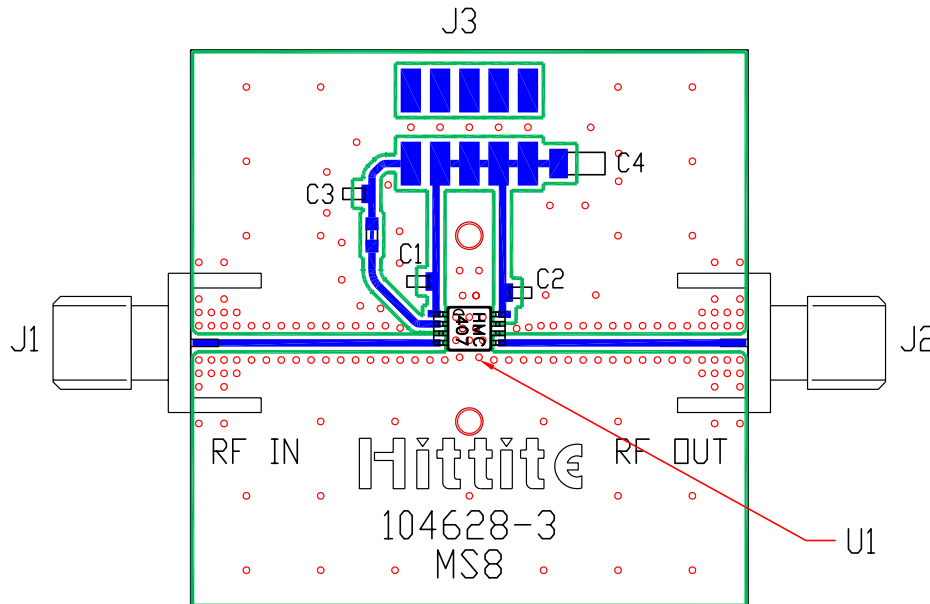
Outline Drawing



Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vcc1	Power supply voltage for the first amplifier stage. An external bypass capacitor of 330 pF is required as shown in the application schematic.	
2	Vpd	Power control pin. For maximum power, this pin should be connected to 5.0V. A higher voltage is not recommended. For lower die current, this voltage can be reduced.	
3, 6, 7	GND	Ground: Backside of package has exposed metal ground slug that must be connected to ground thru a short path. Vias under the device are required.	
4	RF IN	This pin is AC coupled and matched to 50 Ohms from 5.0 to 7.0 GHz.	
5	RF OUT	This pin is AC coupled and matched to 50 Ohms from 5.0 to 7.0 GHz.	
8	Vcc2	Power supply voltage for the output amplifier stage. An external bypass capacitor of 330 pF is required. This capacitor should be placed no more than 20 mils from package lead.	

Evaluation PCB

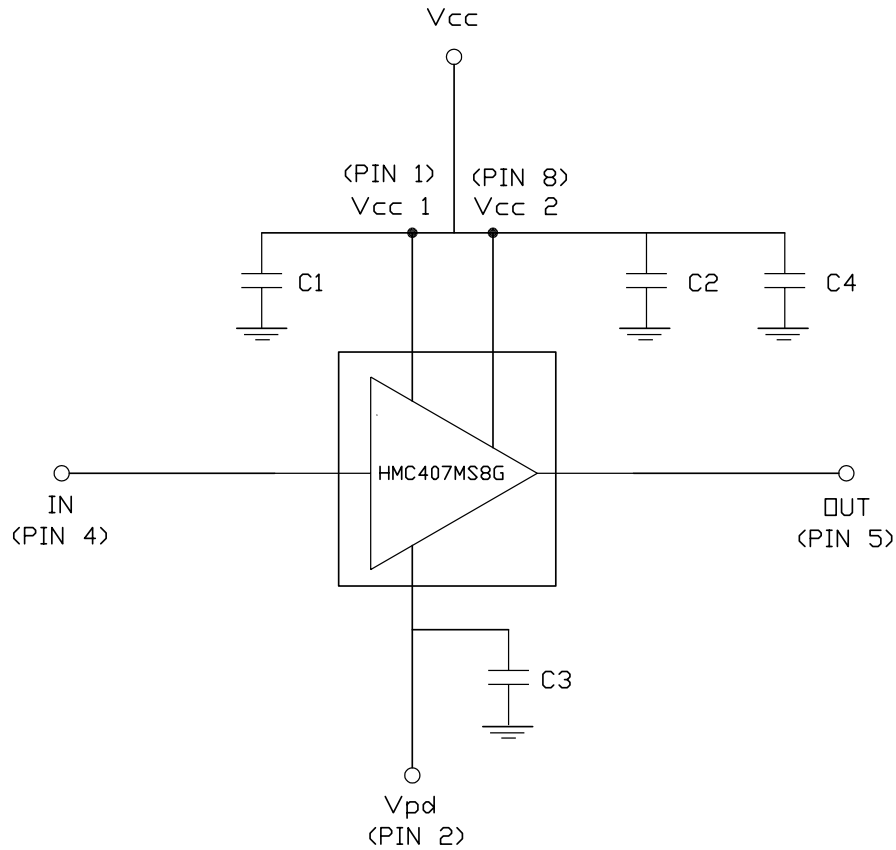


List of Material

Item	Description
J1 - J2	PC Mount SMA RF Connector
J3	2 mm DC Header
C1 - C3	330 pF Capacitor, 0603 Pkg.
C4	2.2 μ F Capacitor, Tantalum
U1	HMC407MS8G Amplifier
PCB*	104628 Eval Board
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Note 1: Vcc1 and Vcc2 may be connected to a common Vcc.

Note 2: C2 should be located < 0.020" from Pin 8 (Vcc2).

HMC407MS8G

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Notes: