

400° ANALOG PHASE SHIFTER 5 - 18 GHz

Typical Applications

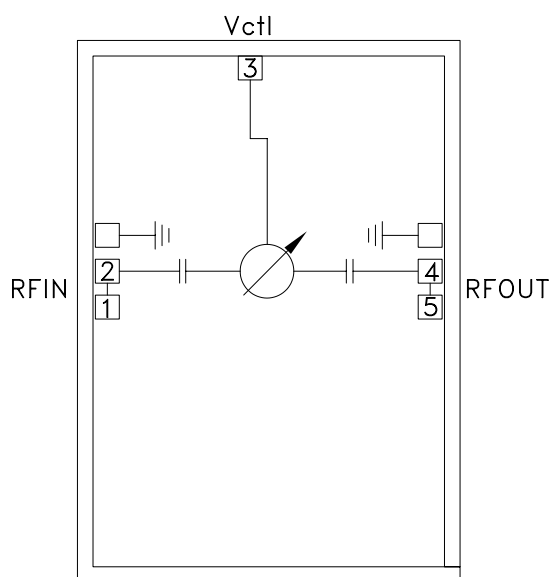
The HMC247 is ideal for:

- Fiber Optics
- Military
- Test Equipment

Features

- Wide Bandwidth: 5 - 18 GHz
- >400° Phase Shift
- Single Positive Voltage Control
- Small Size: 2.5mm x 1.6mm

Functional Diagram



General Description

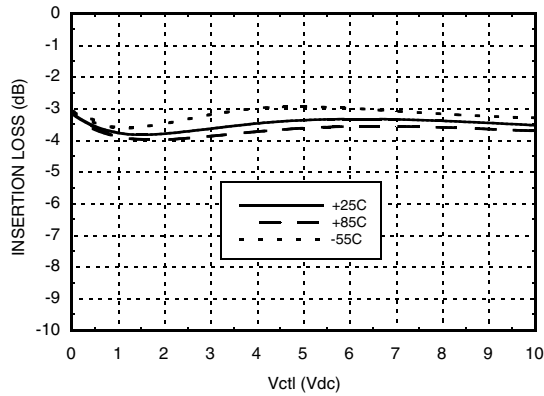
The HMC247 is an Analog Phase Shifter die which is controlled via an analog control voltage from 0 to +10V. The HMC247 provides a continuously variable phase shift of 0 to 300 degrees at 9 GHz, and 0 to 100 degrees at 18 GHz, with consistent insertion loss versus phase shift. The phase shift is monotonic with respect to the control voltage. The control port has a modulation bandwidth of 50 MHz. The low insertion loss and compact size enable this part to be used in a wide range of applications, including the phase adjustment of clocks in fiber optic systems and test equipment. All data is measured with the chip in a 50 ohm test fixture, connected via 0.076 mm (3 mil) ribbon bonds of minimal length <0.31 mm (<12 mils).

Electrical Specifications, $T_A = +25^\circ\text{C}$, 50 Ohm System

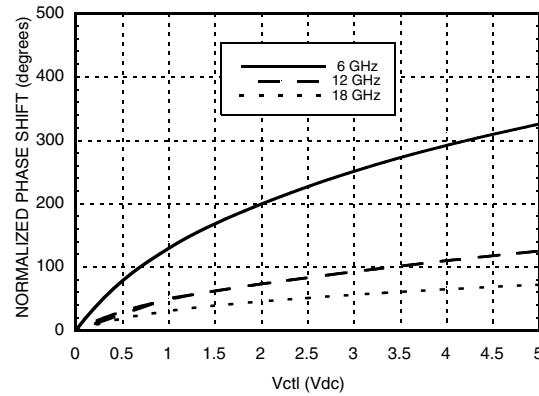
Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Phase Shift Range:	5 - 10 GHz	180	400		degrees
	10 - 13 GHz	135	200		degrees
	13 - 18 GHz	45	120		degrees
Insertion Loss	5 - 10 GHz		8	12	dB
	10 - 18 GHz		4	7	dB
Return Loss (Input and Output)	5 - 18 GHz		8		dB
Control Voltage Range	5 - 18 GHz		0 - 10		Volt
Modulation Bandwidth	5 - 18 GHz		50		MHz
Phase Voltage Sensitivity	5 - 18 GHz		40		deg / Volt
Insertion Phase Temperature Sensitivity	5 - 18 GHz		0.5		deg / °C

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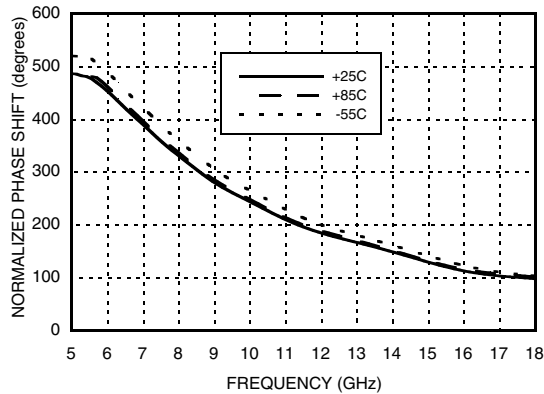
Insertion Loss vs. Control Voltage @ 12 GHz



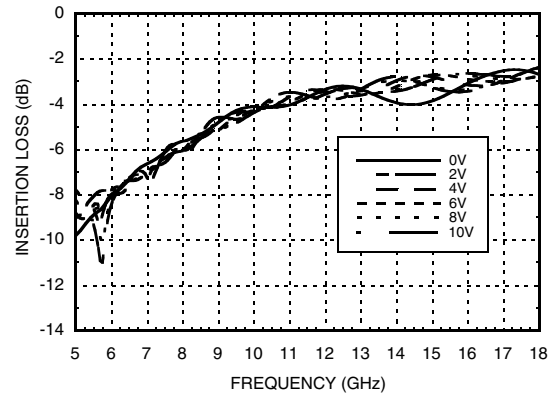
Phase Shift vs. Control Voltage



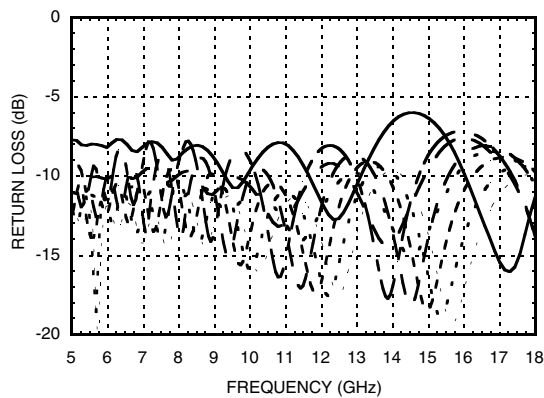
Phase Shift vs. Frequency @ V_{ctl} = 10V
(Relative to V_{ctl} = 0V)



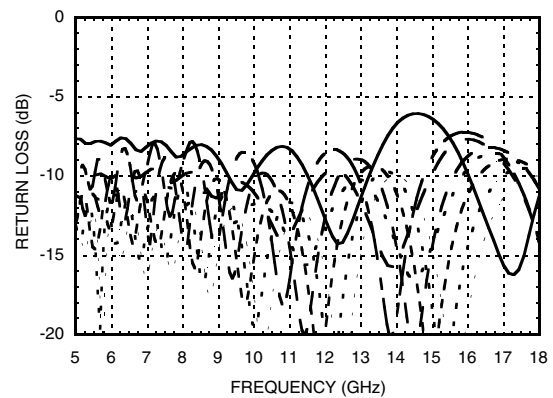
Insertion Loss vs. Frequency



Input Return Loss vs. Frequency,
V_{ctl} = 0 to +10V

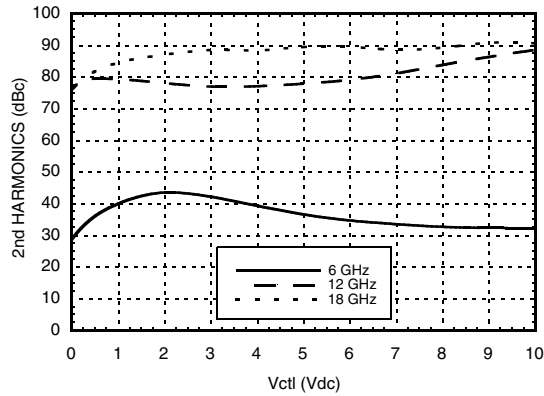


Output Return Loss vs. Frequency,
V_{ctl} = 0 to +10V

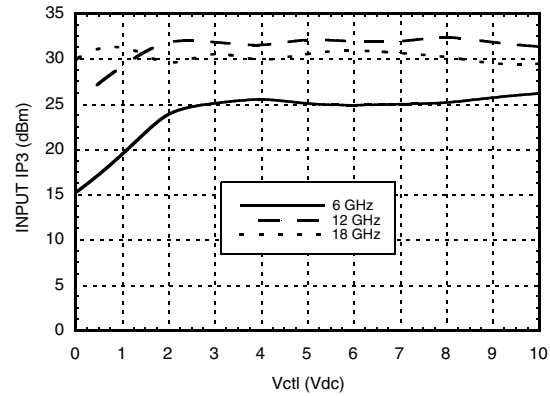


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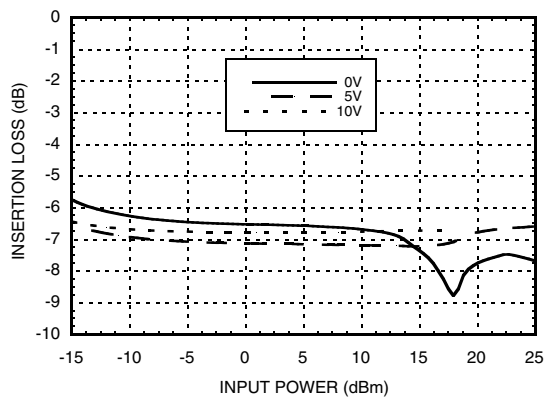
Second Harmonics vs. Control Voltage, Pin = -10 dBm



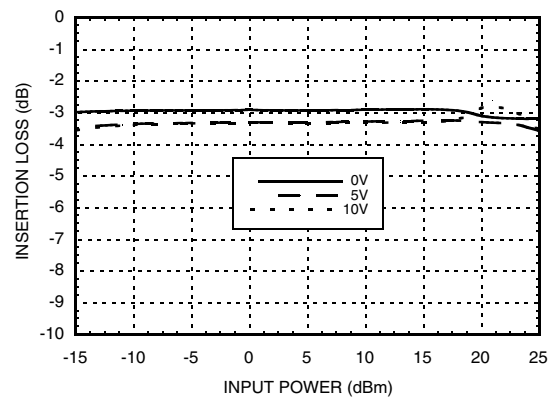
Input IP3 vs. Control Voltage



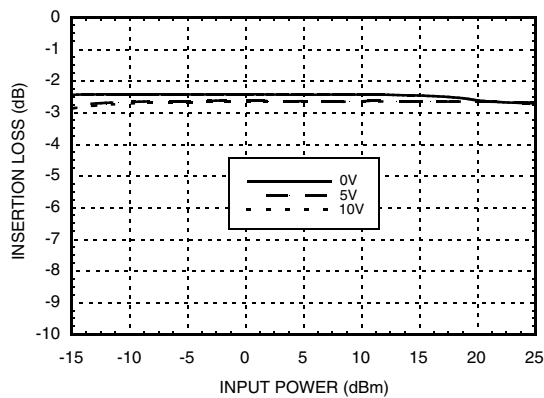
Insertion Loss vs. Pin @ 7 GHz



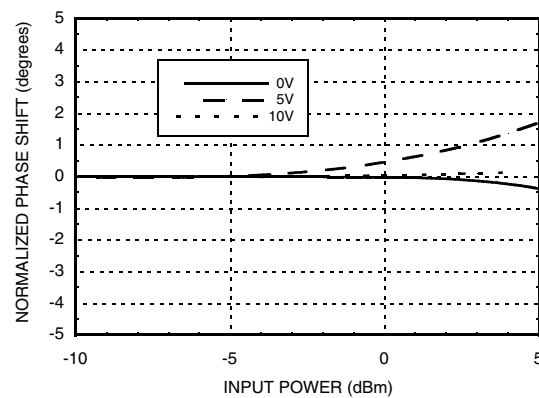
Insertion Loss vs. Pin @ 12 GHz



Insertion Loss vs. Pin @ 18 GHz

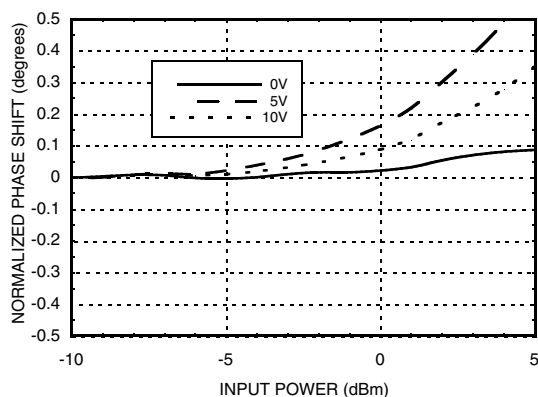


Phase Shift vs. Pin @ 7 GHz

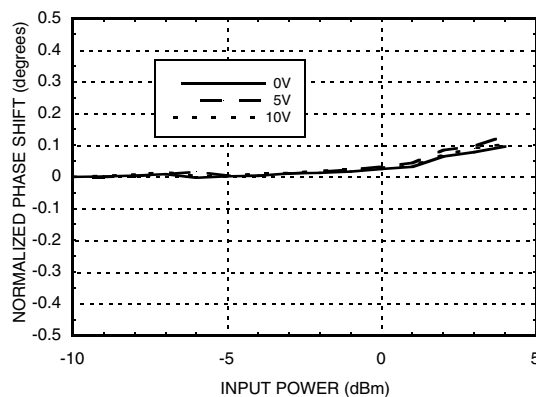


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Phase Shift vs. Pin @ 12 GHz



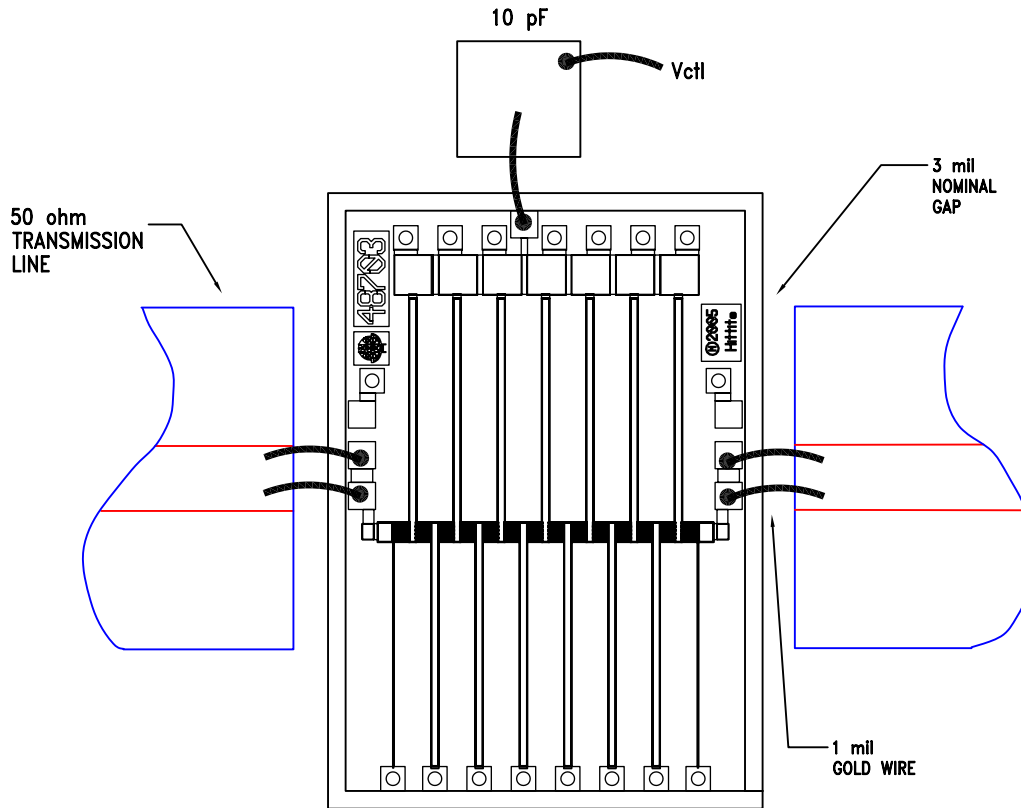
Phase Shift vs. Pin @ 18 GHz



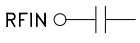
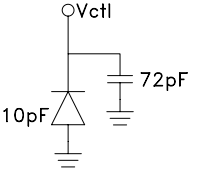


Absolute Maximum Ratings

Control Voltage (Vctl)	+11 Vdc
Reverse Current	5 mA
Input Power (RFin)	+30 dBm
Channel Temperature (Tc)	150 °C
Continuous P _{diss} (T = 85 °C) (derate 28 mW/°C above 85 °C)	1.83 W
Thermal Resistance (junction to die bottom)	35.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

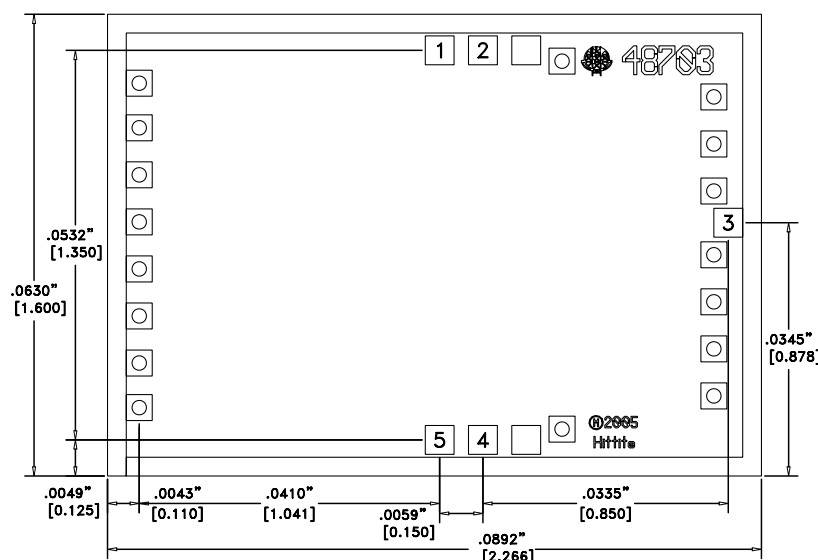
Assembly Diagram



Pad Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2	RFIN	Port is DC blocked.	RFIN 
3	Vctl	Phase shift control pin. Application of voltage between 0 and 10 volts causes the transmission phase to change. The DC equivalent circuit is a series connected diode resistor	
4, 5	RFOUT	Port is DC blocked.	 RFOUT
	GND	The backside of the die must be connected to RF / DC ground.	

Outline Drawing



1. ALL DIMENSIONS ARE IN INCHES [MM]
2. TIE ALL UNLABELED BOND PADS TO GROUND.
3. DIE THICKNESS IS .004"
4. TYPICAL BOND PAD IS .004" SQUARE.
5. BACKSIDE METALIZATION: GOLD.
6. BOND PAD METALIZATION: GOLD.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against $\pm 250V$ ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible $<0.31mm$ (12 mils).