HD74UH00

2-input NAND Gate

HITACHI

ADE-205-014A(Z)
2nd Edition
August 1993

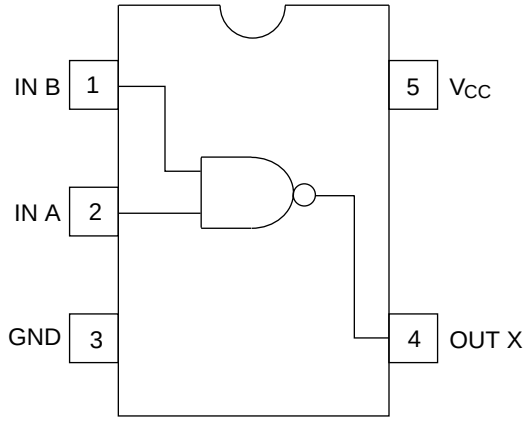
Description

The HD74UH00 is high speed CMOS two input NAND gate using silicon gate CMOS process. With CMOS low power dissipation, it provides high speed equivalent to LS-TTL series. The internal circuit of three stages construction with buffer provides wide noise margin and stable output.

Features

- Encapsulated in very small 5pins package of $2.9 \times 1.6 \times 1.1$ mm, the efficiency to mount on substrate is significantly improved.
- The basic gate function is lined up as hitachi uni logic series.
- Supplied on embos taping for high speed automatic mounting.
- Electrical characteristics equivalent to the HD74HC00
  Supply voltage range: 2 to 6 V
  Operating temperature range: –40 to +85°C
- $| I_{OH} | = I_{OL} = 2$ mA (min)

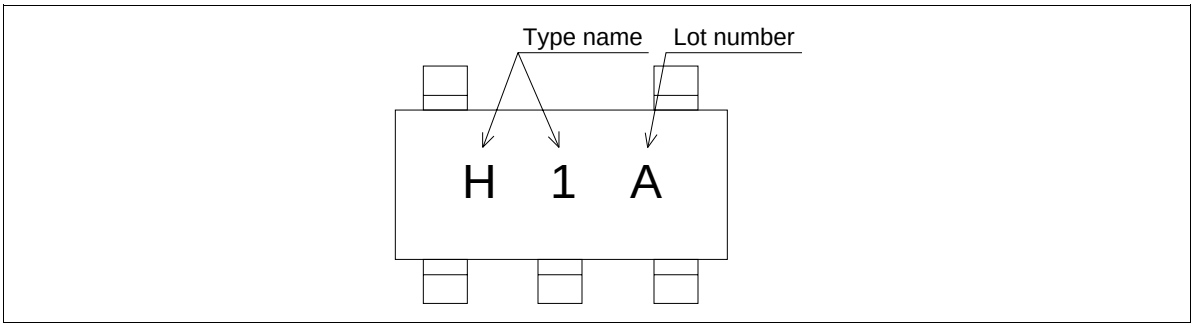
Pin Arrangement



(Top view)

Hitachi semiconductor

Article Indication



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
Output current	I_{OUT}	±25	mA
V_{CC}/GND current	I_{CC}, I_{GND}	±25	mA
Power dissipation	P_T	200	mW
Strage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	Topr	–40 to +85	°C
Input rise/fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V)	ns
		0 to 500 (V_{CC} = 4.5 V)	
		0 to 400 (V_{CC} = 6.0 V)	

Electrical Characteristics

Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit	Test Conditions V_{CC}		
Input voltage	V_{IH}	1.5	—	—	1.5	—	V	2.0		
		3.15	—	—	3.15	—		4.5		
		4.2	—	—	4.2	—		6.0		
	V_{IL}	—	—	0.5	—	0.5	V	2.0		
		—	—	1.35	—	1.35		4.5		
		—	—	1.8	—	1.8		6.0		
Output voltage	V_{OH}	1.9	2.0	—	1.9	—	V	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.4	4.5	—	4.4	—		4.5		
		5.9	6.0	—	5.9	—		6.0		
		4.18	4.31	—	4.31	—		4.5		I_{OH} = –2 mA
		5.68	5.80	—	5.63	—		6.0		I_{OH} = –2.6 mA
	V_{OL}	—	0.0	0.1	—	0.1	V	2.0	V_{IN} = V_{IH}	I_{OL} = 20 µA
		—	0.0	0.1	—	0.1		4.5		
		—	0.0	0.1	—	0.1		6.0		
		—	0.17	0.26	—	0.33		4.5		I_{OL} = 2 mA
		—	0.18	0.26	—	0.33		6.0		I_{OL} = 2.6 mA
Input current	I_{IN}	—	—	±0.1	—	±1.0	µA	6.0	V_{IN} = V_{CC} or GND	
Operating current	I_{CC}	—	—	1.0	—	10.0		6.0	V_{IN} = V_{CC} or GND	

Switching Characteristics

Item	Symbol	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Output rise/fall time	t_{TLH}	—	5	10	ns	See Test circuit
	t_{THL}					
Propagation delay time	t_{PLH}	—	7	15	ns	See Test circuit
	t_{PHL}					

(C_L = 15 pF, t_r = t_f = 6 ns, V_{CC} = 5 V)

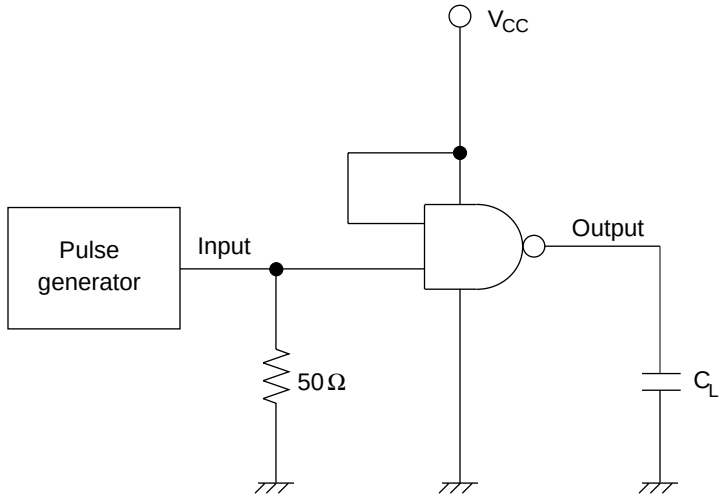
Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit	Test Conditions V_{cc}	
Output rise/fall time	t_{TLH}	—	50	125	—	155	ns	2.0	See under figure
	t_{THL}	—	14	25	—	31		4.5	
		—	12	21	—	26		6.0	
Propagation delay time	t_{PLH}	—	48	100	—	125	ns	2.0	See under figure
	t_{PHL}	—	12	20	—	25		4.5	
		—	9	17	—	21		6.0	
Input capacitance	C_{IN}	—	5	10	—	10	pF	—	
Equivalent capacitance	C_{PD}	—	10	—	—	—		—	

(C_L = 50 pF, $t_r = t_f$ = 6 ns)

Note: C_{PD} is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

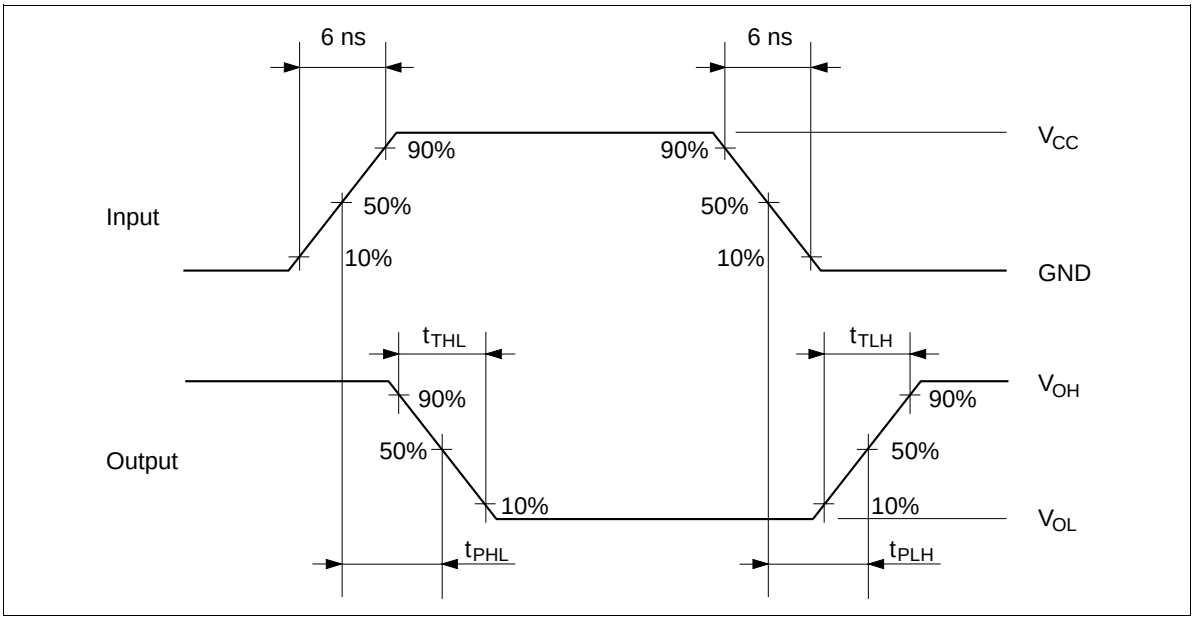
$I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

Test Circuit

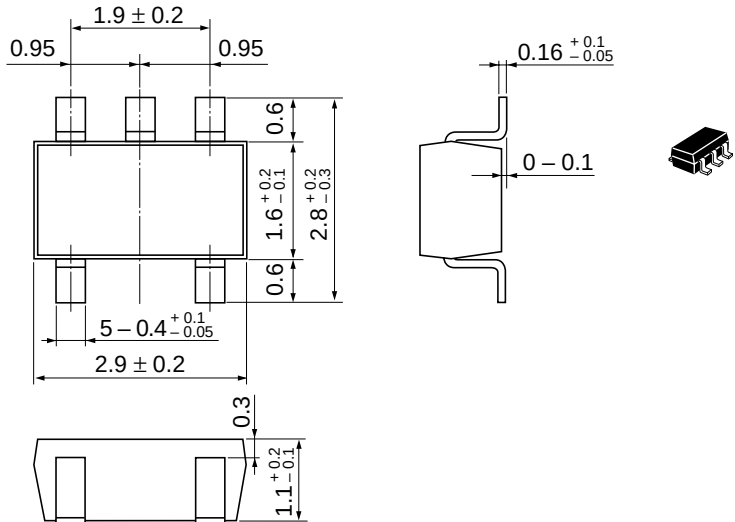


Note: Operating current test time, output is open.

Waveforms


6 ns
6 ns
90%
90%
50%
50%
10%
10%
Input
V_{CC}
GND
t_{THL}
t_{TLH}
90%
90%
50%
50%
10%
10%
Output
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}

Unit: mm



Hitachi Code	MPAK-5
JEDEC	—
EIAJ	—
Weight (reference value)	0.015 g

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