
HD74LVCZ16245A

16-bit Bidirectional Transceivers with 3-state Outputs

HITACHI

ADE-205-233 (Z)
1st. Edition
February 1999

Description

The HD74LVCZ16245A has sixteen two direction buffers, for the fittest at two direction bus lines with three state outputs in a 48 pin package. When (DIR) is high, data flows from the A inputs to the B outputs, and when (DIR) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input (\bar{G}) high level.

When V_{CC} is between 0 and 1.5 V, the device is in the high impedance state during power up or power down.

Low voltage and high speed operation is suitable at battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.7$ to 5.5 V
- All inputs $V_{IH} (\text{Max}) = 5.5$ V (@ $V_{CC} = 0$ to 5.5 V)
- All inputs / outputs $V_{IO} (\text{Max}) = 5.5$ V (@ $V_{CC} = 0$ V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@ $V_{CC} = 3.3$ V, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot > 2.0 V (@ $V_{CC} = 3.3$ V, $T_a = 25^\circ\text{C}$)
- High impedance state during power up and power down
- Power off disables outputs, permitting live insertion
- High output current ± 24 mA (@ $V_{CC} = 3.0$ to 5.5 V)

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Function Table

Inputs		Operation
\overline{G}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Z

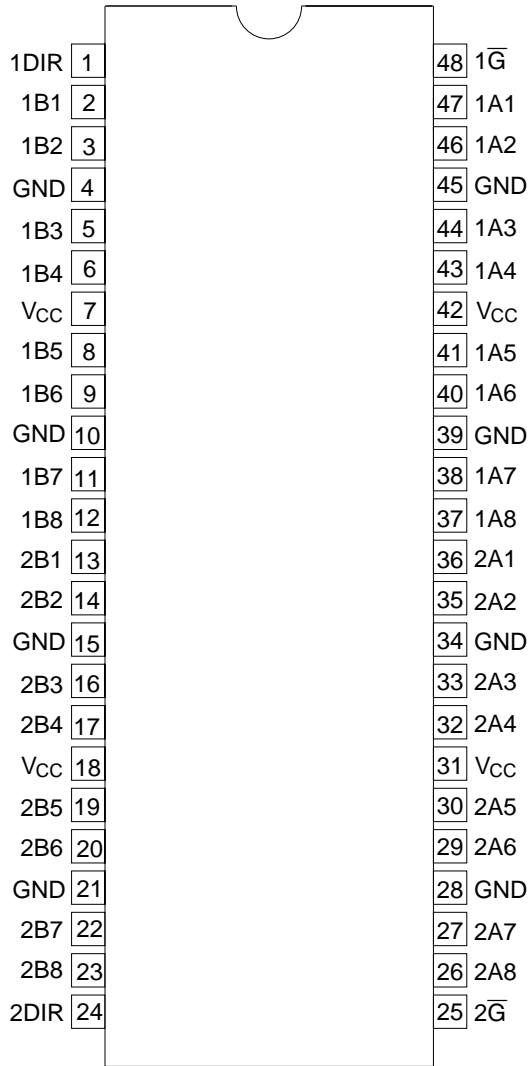
H : High level

L : Low level

X : Immaterial

Z : High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 7.0	V	
Input voltage	V_I	-0.5 to 7.0	V	
Input / output voltage	V_{IO}	-0.5 to 7.0	V	Output "Z" or V_{CC} : OFF
		-0.5 to $V_{CC}+0.5$		Output "H" or "L"
Input diode current	I_{IK}	-50	mA	$V_I < 0$
Output diode current	I_{OK}	-50	mA	$V_O < 0$
Output current	I_O	± 50	mA	
V_{CC} , GND current	I_{CC} or I_{GND}	± 100	mA	
Storage temperature	Tstg	-65 to 150	°C	

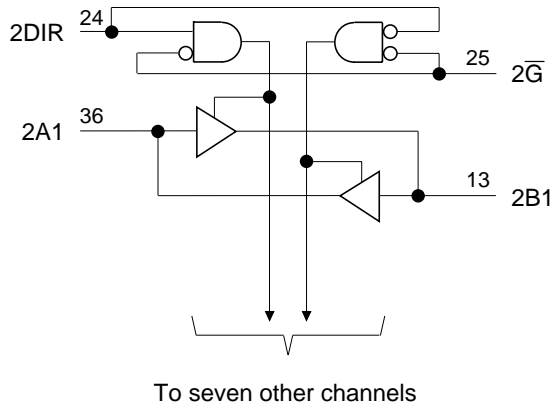
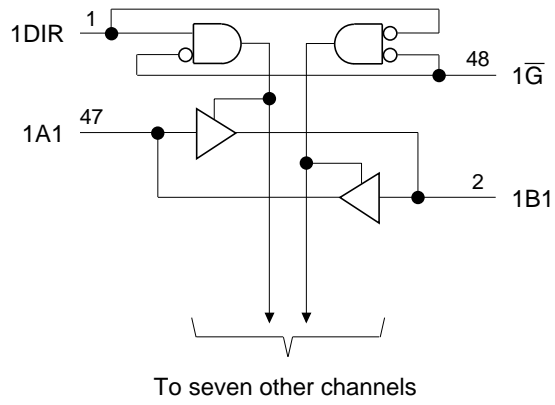
Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2.7 to 5.5	V	At operation
Input voltage	V_I	0 to 5.5	V	
Input / output voltage	V_{IO}	0 to 5.5	V	Output "Z" or V_{CC} : OFF
		0 to V_{CC}		Output "H" or "L"
Output current	I_{OH}	-12	mA	$V_{CC} = 2.7$ V
		-24 ^{*1}		$V_{CC} = 3.0$ to 5.5 V
	I_{OL}	12		$V_{CC} = 2.7$ V
		24 ^{*1}		$V_{CC} = 3.0$ to 5.5 V
Input rise / fall time	t_r, t_f	0 to 6	ns / V	
Operating temperature	Ta	-40 to +85	°C	

Note: 1. Duty cycle $\leq 50\%$

Logic Diagram



Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.7 to 3.6	2.0	—	—	V	
		4.5 to 5.5	V _{CC} ×0.7	—	—		
	V _{IL}	2.7 to 3.6	—	—	0.8		
		4.5 to 5.5	—	—	V _{CC} ×0.3		
Output voltage	V _{OH}	2.7 to 5.5	V _{CC} -0.2	—	—	V	I _{OH} = -100 μA
		2.7	2.2	—	—		I _{OH} = -12 mA
		3.0	2.4	—	—		
		3.0	2.2	—	—		I _{OH} = -24 mA
		4.5	3.8	—	—		
	V _{OL}	2.7 to 5.5	—	—	0.2	I _{OL} = 100 μA	
		2.7	—	—	0.4	I _{OL} = 12 mA	
		3.0	—	—	0.55	I _{OL} = 24 mA	
		4.5	—	—	0.55		
	Input current	I _{IN}	0 to 5.5	—	—	±5	μA
Off state output current	I _{OZ}	2.7 to 5.5	—	—	±5	μA	V _{OUT} = 0 to 5.5 V
	I _{OZPU}	0 to 1.5	—	—	±5		V _{OUT} = 0.5 to 5.5 V,
	I _{OZPD}	1.5 to 0	—	—	±5		Output enable = don't care
Output leak current	I _{OFF}	0	—	—	±5	μA	V _{IN} or V _O = 5.5 V
Quiescent supply current	I _{CC}	2.7 to 3.6	—	—	225	μA	V _{IN} = 3.6 to 5.5 V ¹⁾ , I _O = 0
		2.7 to 5.5	—	—	350		V _{IN} = V _{CC} or GND
	ΔI _{CC}	2.7 to 3.6	—	—	500		V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND
Input capacitance	C _{IN}	3.3	—	4.1	—	pF	V _{IN} = V _{CC} or GND
Input / output capacitance	C _{I/O}	3.3	—	9.2	—	pF	V _{OUT} = V _{CC} or GND

Note: 1. This applies in the disabled state only.

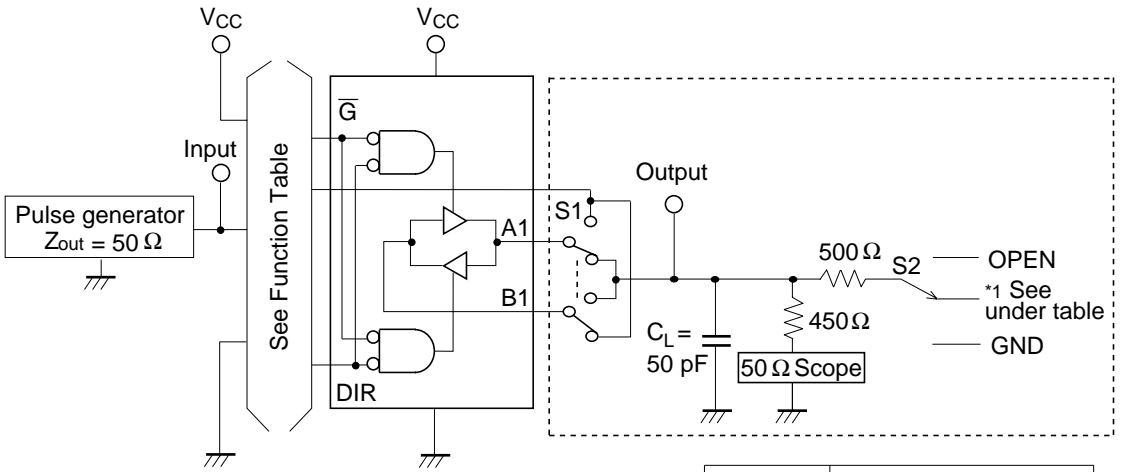
Switching Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Propagation delay time	t _{PLH}	2.7	—	—	5.2	ns	A or B	B or A
	t _{PHL}	3.3±0.3	1.0	—	4.6			
		5.0±0.5	—	—	4.0			
Output enable time	t _{ZH}	2.7	—	—	7.3	ns	\bar{G}	A or B
	t _{ZL}	3.3±0.3	1.5	—	6.3			
		5.0±0.5	—	—	5.2			
Output disable time	t _{HZ}	2.7	—	—	7.5	ns	\bar{G}	A or B
	t _{LZ}	3.3±0.3	1.5	—	6.9			
		5.0±0.5	—	—	6.0			
Between output pin skew ^{**1}	t _{OSLH}	2.7	—	—	—	ns		
	t _{OSHL}	3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			

Note : 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

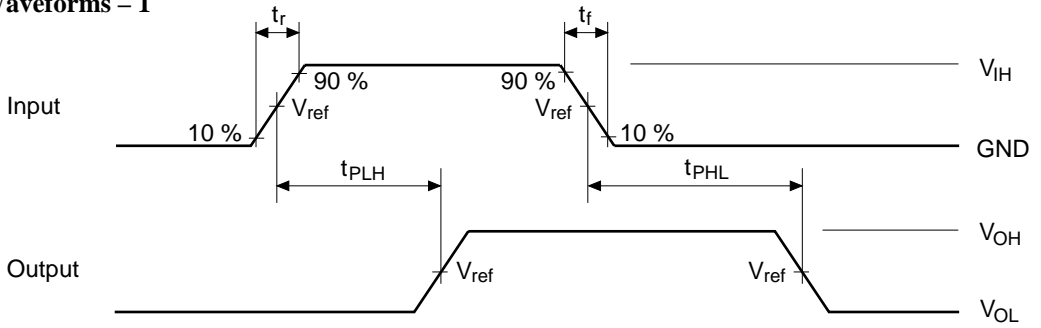
Test Circuit



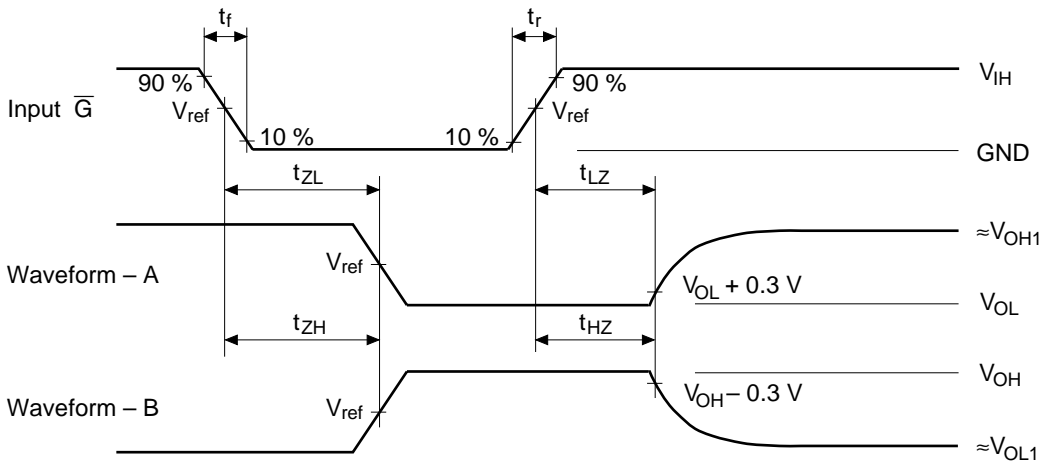
Symbol	S2	
	$V_{CC}=2.7V, 3.3\pm 0.3V$	$V_{CC}=5.0\pm 0.5V$
t_{PLH}/t_{PHL}	OPEN	OPEN
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	6 V	$2 \times V_{CC}$

- Notes:
1. C_L includes probe and jig capacitance.
 2. A2–B2 to A8–B8 are identical to above load circuit.
 3. S1 : Input–Output change switch.

• Waveforms – 1



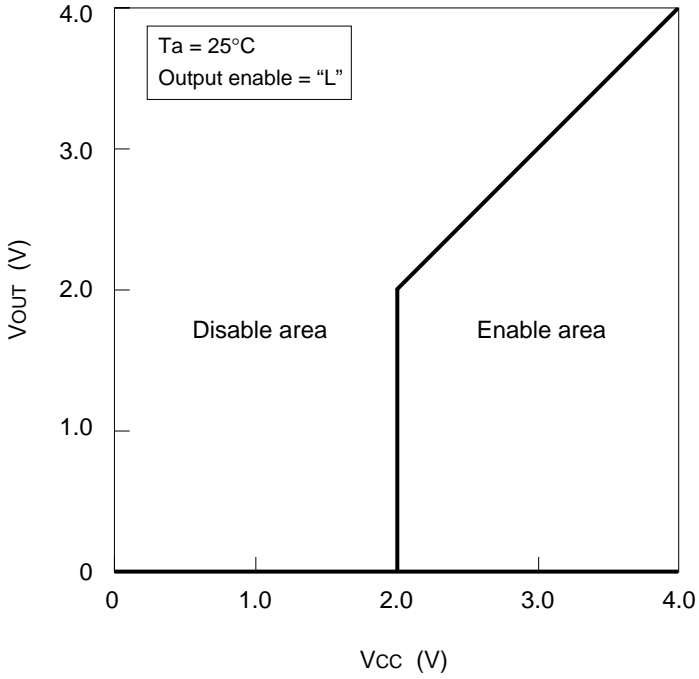
• Waveforms – 2



TEST	V _{CC} =2.7V, 3.3±0.3V	V _{CC} =5.0±0.5V
V _{IH}	2.7 V	V _{CC}
V _{ref}	1.5 V	50%V _{CC}
V _{OH1}	3 V	V _{CC}
V _{OL1}	GND	GND

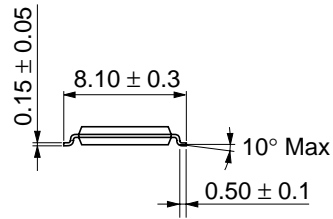
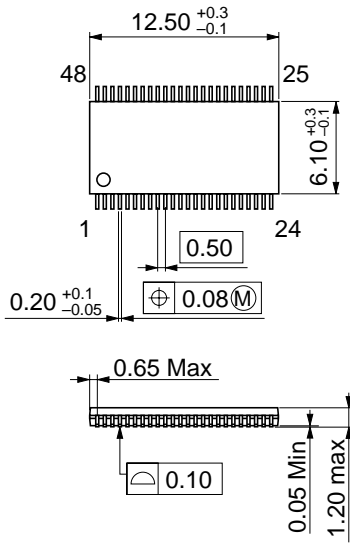
- Notes: 1. Input waveform : PRR = 10 MHz, duty cycle 50%, $t_r = 2.5$ ns, $t_f = 2.5$ ns
 2. Waveform – A shows input conditions such that the output is “L” level when enabled by the output control.
 3. Waveform – B shows input conditions such that the output is “H” level when enabled by the output control.

Power up / down Characteristics



Package Dimensions

Unit : mm



Hitachi code	TTP-48DC
EIAJ code	—
JEDEC code	—

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