
HD74HC674

16-bit Shift Register

HITACHI

Description

The HD74HC674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (data I/O) port provides access for entering serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

1. Hold (do nothing)
2. Write (serially via input/output)
3. Read (serially)
4. Load (parallel via data inputs)




Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

Features

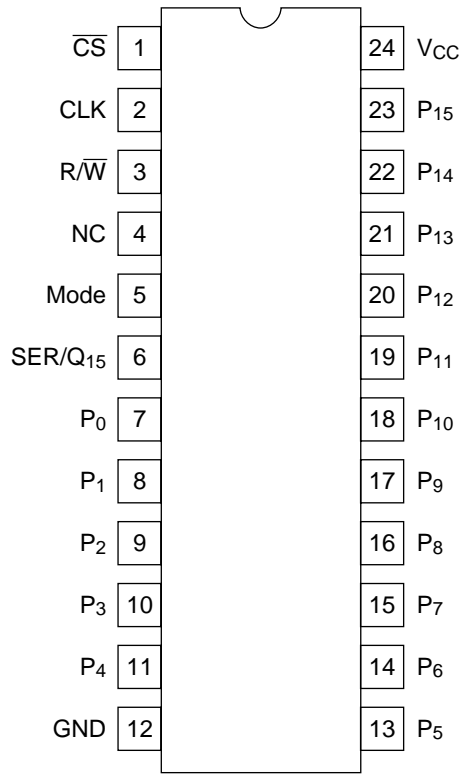
- High Speed Operation: t_{pd} (CLK to SER/Q₁₅) = 17 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Inputs

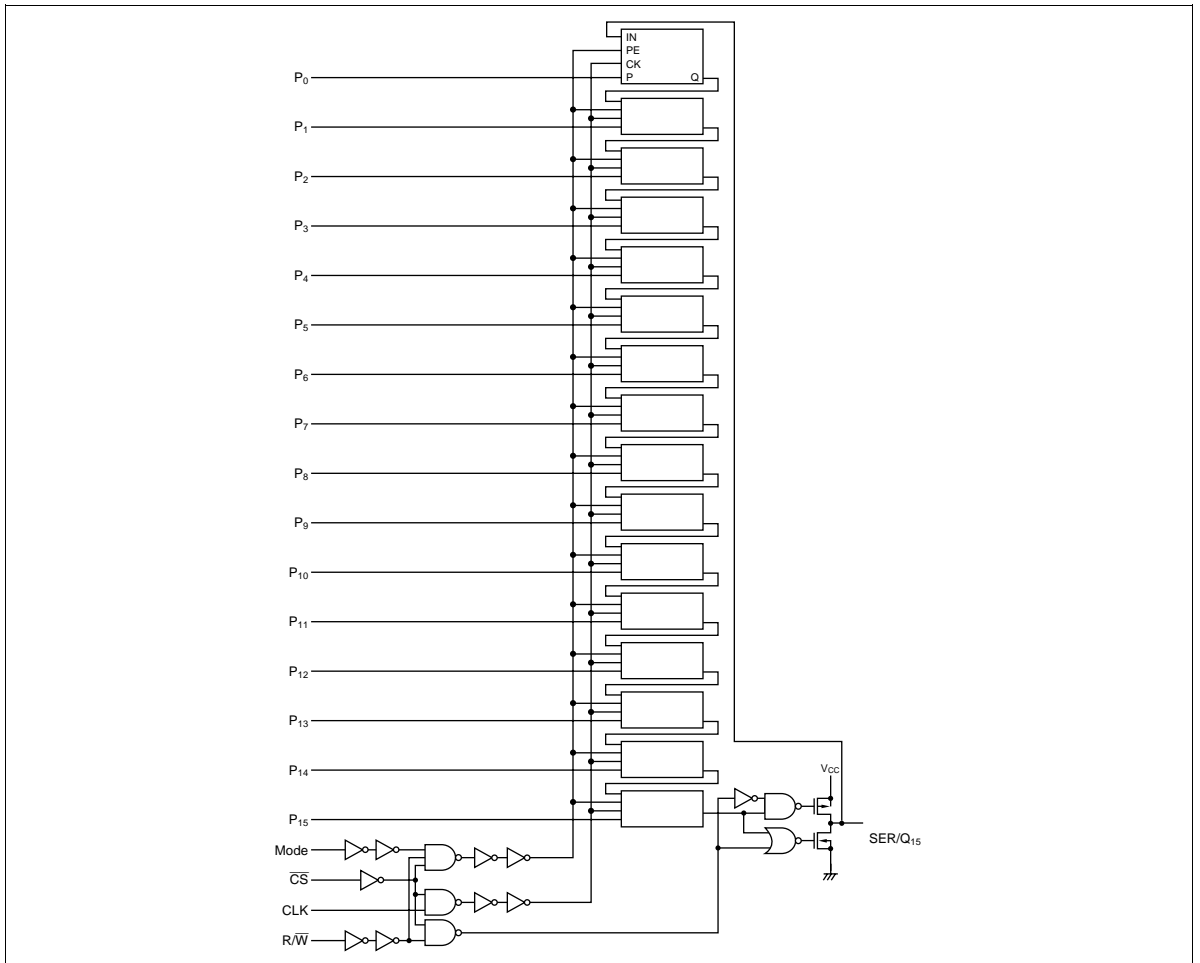
$\overline{\text{CS}}$	R/W	Mode	CLK	SER/Q ₁₅	Operation
H	X	X	X	Z	Do nothing
L	L	X		Z	Shift and write (serial load)
L	H	L		Q _{14n}	Shift and read
L	H	H		P ₁₅	Parallel load

Pin Arrangement



(Top view)

Logic Diagram



DC Characteristics

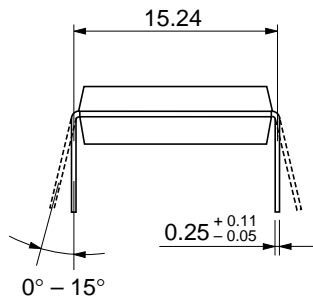
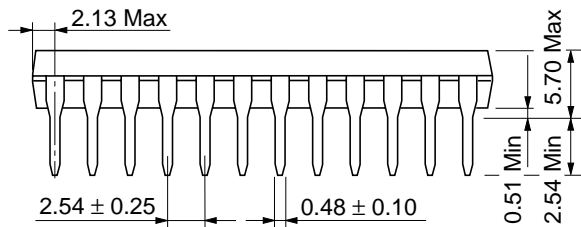
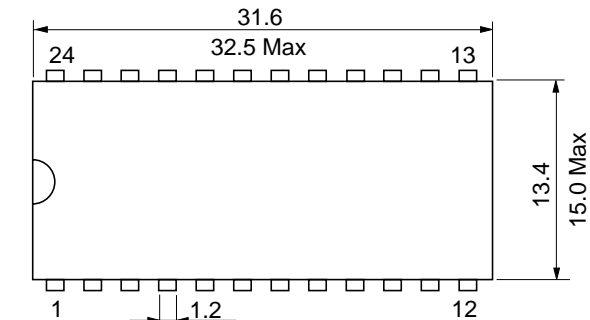
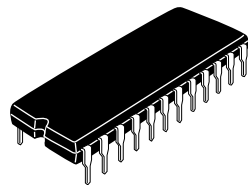
Item	Symbol	V _{CC} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V _{IL}	2.0	—	—	0.5	—	0.5		V
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I _{OH} = -6 mA
		6.0	5.68	—	—	5.63	—		I _{OH} = -7.8 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I _{OL} = 6 mA
		6.0	—	—	0.26	—	0.33		I _{OL} = 7.8 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA
Off-state output current	I _{OZ}	6.0	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	200	—	250	ns	Clock to SER/Q ₁₅
	t_{PHL}	4.5	—	17	40	—	50		
		6.0	—	—	34	—	43		
Output enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
	t_{ZL}	4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
	t_{LZ}	4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	SER/Q ₁₅ to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	100	—	—	125	—	ns	P to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	100	—	—	125	—	ns	Mode to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	100	—	—	125	—	ns	R/W or CS to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) (cont)

Item	Symbol	V_{CC} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min			Max	
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to SER/Q ₁₅	
		4.5	5	—	—	5	—			
		6.0	5	—	—	5	—			
	t_h	t_h	2.0	5	—	—	5	—	ns	Clock to P
			4.5	5	—	—	5	—		
			6.0	5	—	—	5	—		
	t_h	t_h	2.0	5	—	—	5	—	ns	Clock to mode
			4.5	5	—	—	5	—		
			6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns		
	t_{THL}	4.5	—	4	12	—	15			
		6.0	—	—	10	—	13			
Input capacitance	C_{in}	—	—	5	10	—	10	pF		



Hitachi Code	DP-24
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	3.1 g

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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