
HD74HC180

8-bit Odd/Even Parity Generator/Checker

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Description

This universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generator/checker features odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity of 9th-bit input. The wordlength capability is easily expanded by cascading.

Features

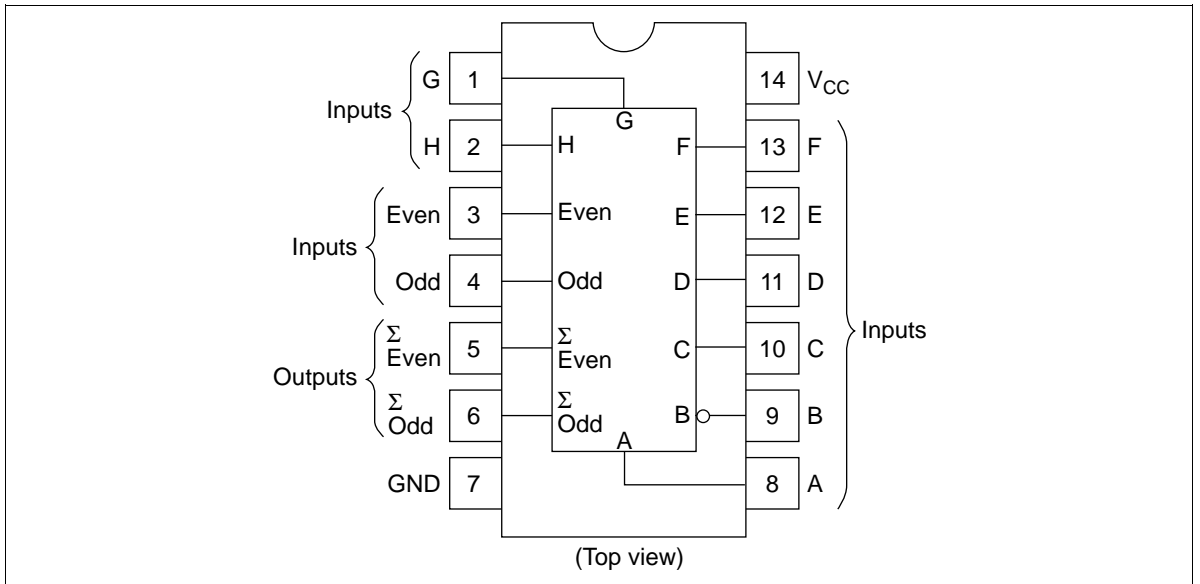
- High Speed Operation:
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max ($T_a = 25^\circ\text{C}$)

Function Table

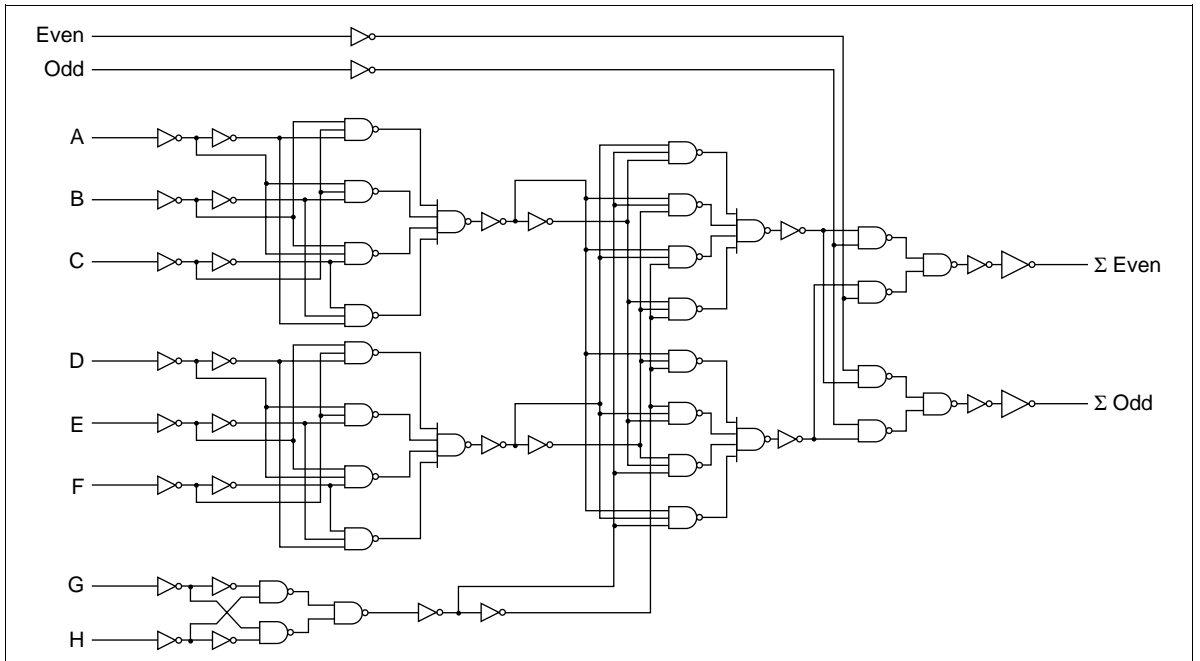
Inputs			Outputs	
Σ of H's at A Thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

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Pin Arrangement



Logic Diagram



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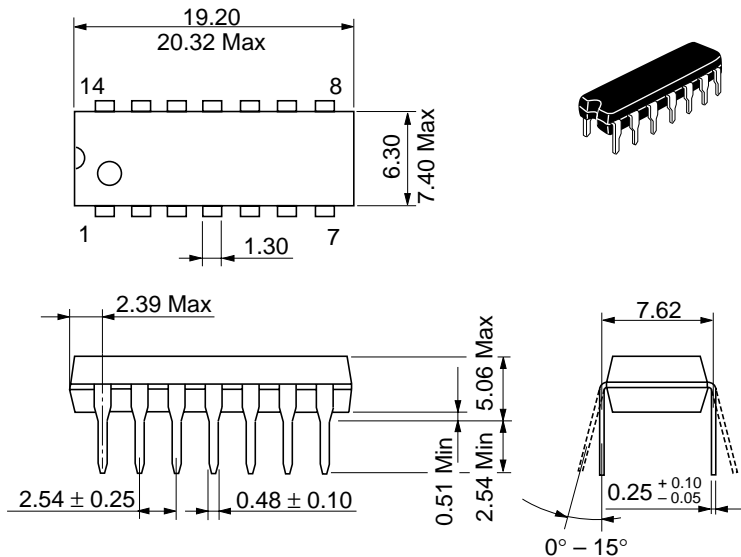
DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
		6.0	—	0.0	0.1	—	0.1			V
	V _{OL}	4.5	—	0.0	0.1	—	0.1	V	I _{OL} = 4 mA	
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
		6.0	—	—	0.26	—	0.33			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

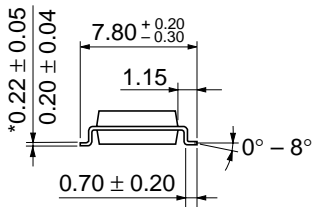
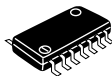
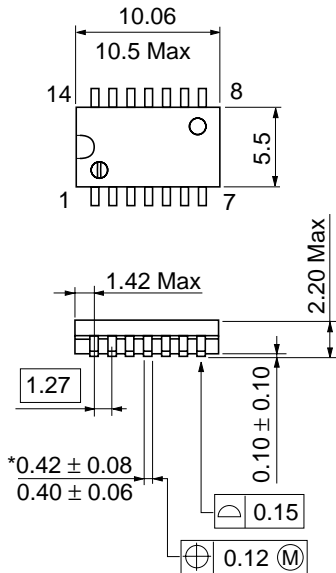
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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t_{PLH}	2.0	—	—	260	—	325	ns	Data (Odd = 0) to Σ Even
		4.5	—	28	52	—	65		
		6.0	—	—	44	—	55		
	t_{PHL}	2.0	—	—	245	—	305	ns	Data (Odd = 0) to Σ Odd
		4.5	—	28	49	—	61		
		6.0	—	—	42	—	52		
	t_{PLH}	2.0	—	—	260	—	325	ns	Data (Even = 0) to Σ Even
		4.5	—	28	52	—	65		
		6.0	—	—	44	—	55		
	t_{PHL}	2.0	—	—	245	—	305	ns	Data (Even = 0) to Σ Odd
		4.5	—	28	49	—	61		
		6.0	—	—	42	—	52		
t_{PLH}	2.0	—	—	110	—	140	ns	Even or Odd to Σ Even or Σ Odd	
	4.5	—	13	22	—	28			
	6.0	—	—	19	—	24			
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	7	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

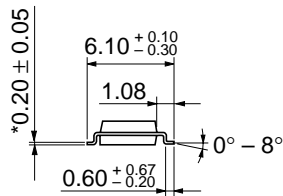
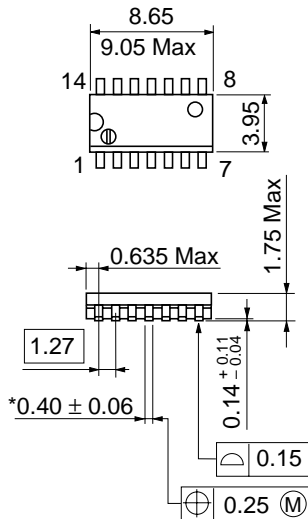


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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