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# HD74BC373A

Octal D Type Transparent Latches With 3 State Outputs

# HITACHI

ADE-205-009A(Z)

Rev. 1

March 1993

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## Description

The HD74BC373A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has eight D type latches with three state outputs in a 20 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

## Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range input pins

Ta = -40 to + 85°C

## Function Table

### Inputs

$\overline{G}$	LE	D	Output Q
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	No change

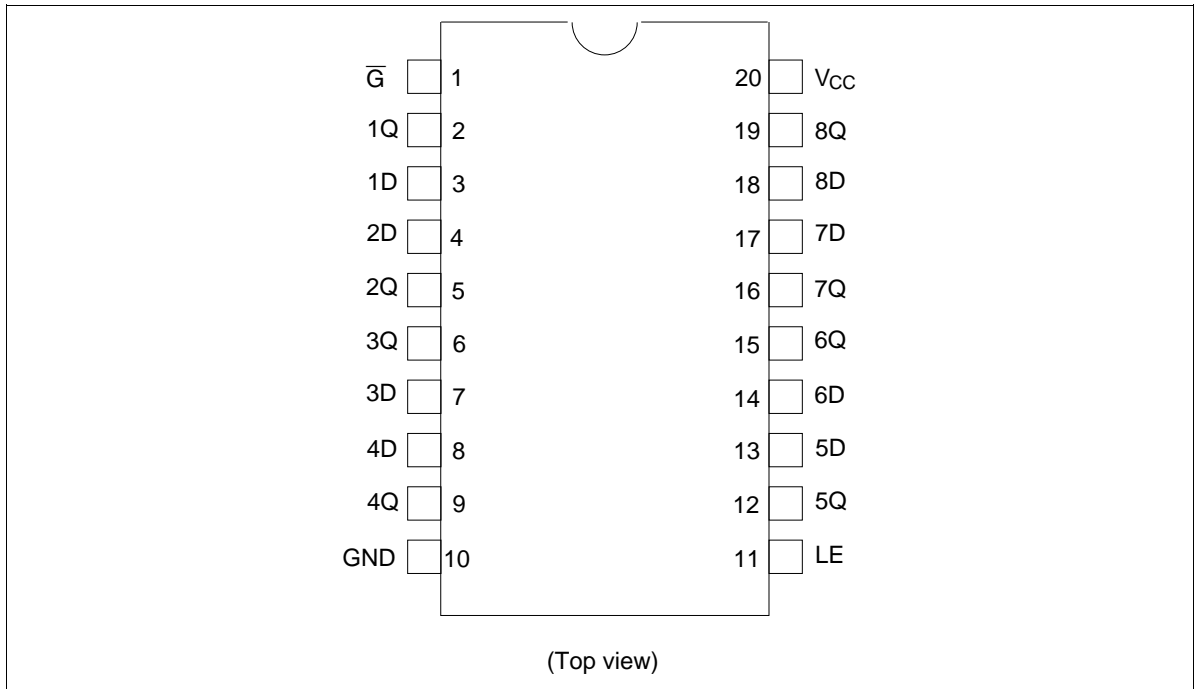
H : High level

L : Low level

X : Immaterial

Z : High impedance

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	-0.5 to +7.0	V
Input diode current	$I_{IK}$	$\pm 30$	mA
Input voltage	$V_{IN}$	-0.5 to +7.5	V
Output voltage	$V_{OUT}$	-0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	-0.5 to +5.5	V
Storage temperature	Tstg	-65 to +150	°C

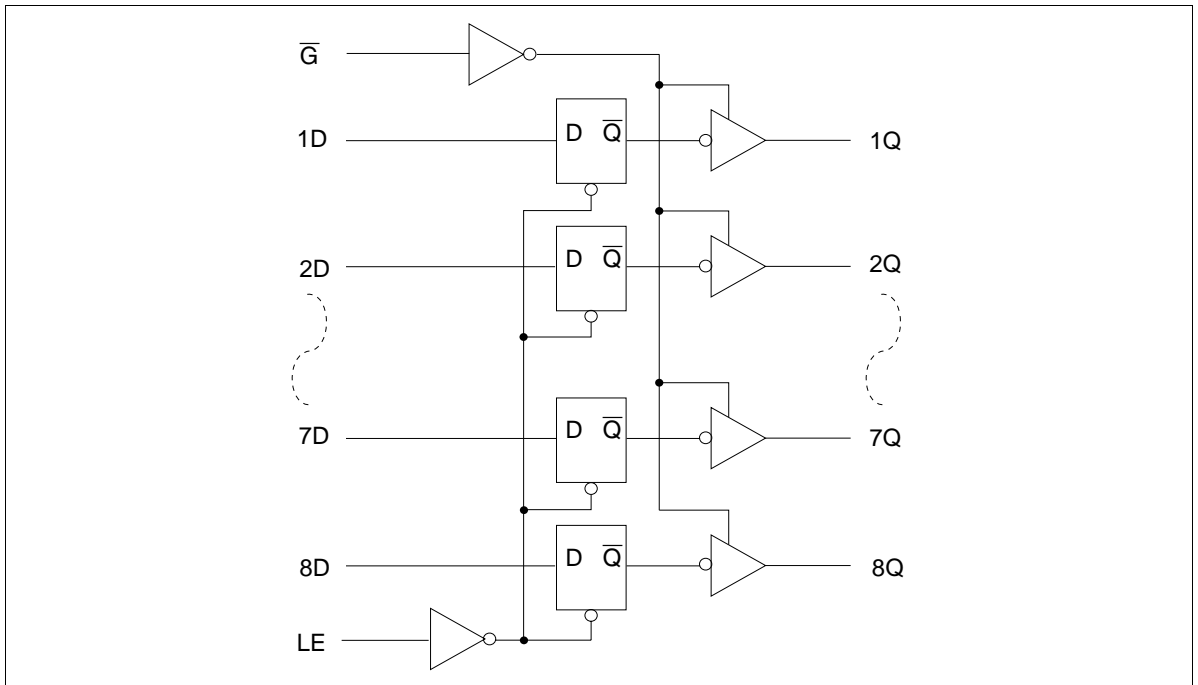
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	$V_{IN}$	0	—	$V_{CC}$	V
Output voltage	$V_{OUT}$	0	—	$V_{CC}$	V
Operating temperature	$T_{opr}$	-40	—	85	°C
Input rise/fall time*1	$t_r, t_f$	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.  
 Waveform: Refer to test circuit of switching characteristics.

**Logic Diagram**



# HD74BC373A

## Electrical Characteristics (Ta = -40°C to +85°C)

Item	Symbol	V <sub>cc</sub> (V)	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>		2.0	—	V	
	V <sub>IL</sub>		—	0.8	V	
Output voltage	V <sub>OH</sub>	4.5	2.4	—	V	I <sub>OH</sub> = -3 mA
		4.5	2.0	—	V	I <sub>OH</sub> = -15 mA
	V <sub>OL</sub>	4.5	—	0.4	V	I <sub>OL</sub> = 24 mA
		4.5	—	0.5	V	I <sub>OL</sub> = 48 mA
Input diode voltage	V <sub>IK</sub>	4.5	—	-1.2	V	I <sub>IN</sub> = -18 mA
Input current	I <sub>I</sub>	5.5	—	-250	μA	V <sub>IN</sub> = 0 V
		5.5	—	1.0	μA	V <sub>IN</sub> = 5.5 V
		5.5	—	100	μA	V <sub>IN</sub> = 7.0 V
Short circuit output current*1	I <sub>OS</sub>	5.5	-100	-225	mA	V <sub>IN</sub> = 0 or 5.5 V
Off state output current	I <sub>OZH</sub>	5.5	—	50	μA	V <sub>O</sub> = 2.7 V
	I <sub>OZL</sub>	5.5	—	-50	μA	V <sub>O</sub> = 0.5 V
Supply current	I <sub>CCL</sub>	5.5	—	29.5	mA	V <sub>IN</sub> = 0 or 5.5 V All outputs is "L"
	I <sub>CCH</sub>	5.5	—	2.5	mA	V <sub>IN</sub> = 0 or 5.5 V All outputs is "H"
	I <sub>CCZ</sub>	5.5	—	2.5	mA	V <sub>IN</sub> = 0 or 5.5 V All outputs is "Z"
	I <sub>CCT</sub> *2	5.5	—	1.5	mA	V <sub>IN</sub> = 3.4 or 0.5 V

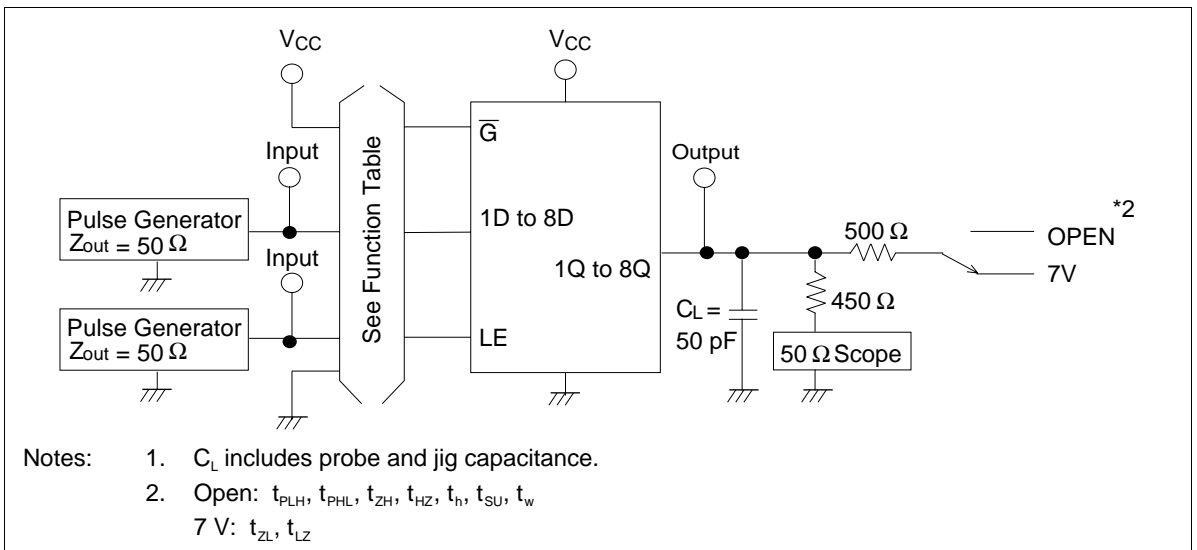
Notes : 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

2. When input by the TTL level, it shows I<sub>CC</sub> increase at per one input pin.

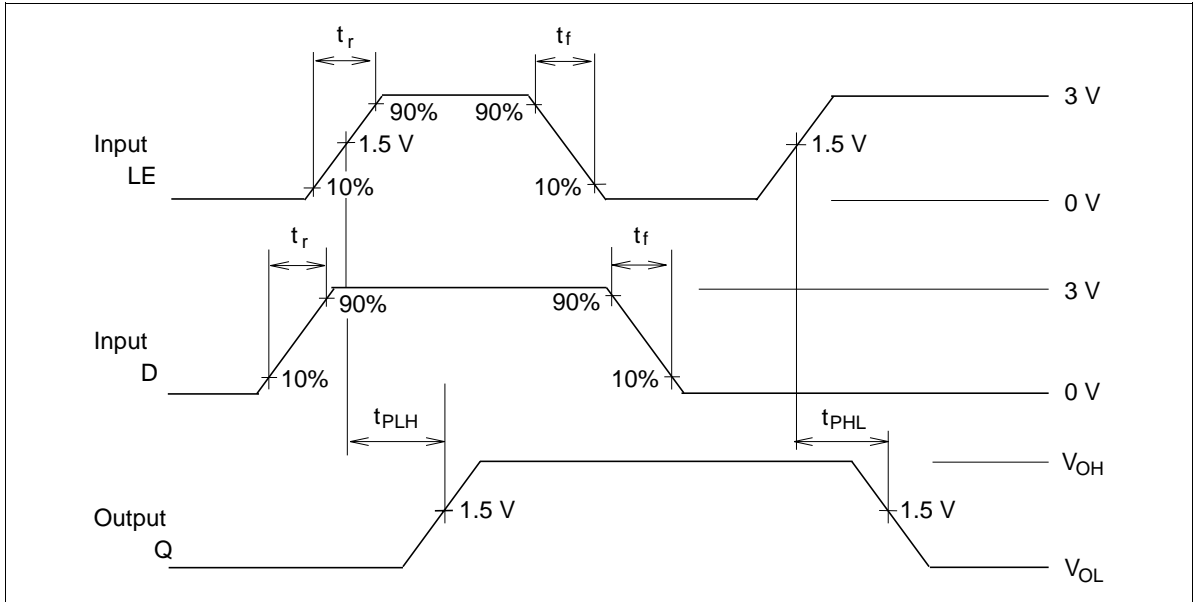
Switching Test Method ( $C_L = 50 \text{ pF}$ )

Item	Symbol	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0 \text{ V}$		$T_a = -40 \text{ to } 85^\circ\text{C}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$		Unit	Test Conditions	
		Min	Max	Min	Max			
Propagation delay time	$D \rightarrow Q$	$t_{PLH}$	3.0	8.0	3.0	10.0	ns	See under figure
		$t_{PHL}$	3.0	8.0	3.0	10.0		
	$LE \rightarrow Q$	$t_{PLH}$	3.0	8.0	3.0	10.0		
		$t_{PHL}$	3.0	8.0	3.0	10.0		
Output enable time		$t_{ZH}$	3.0	9.0	3.0	11.0	ns	
		$t_{ZL}$	3.0	9.0	3.0	11.0		
Output disable time		$t_{HZ}$	3.0	8.0	3.0	10.0	ns	
		$t_{LZ}$	3.0	8.0	3.0	10.0		
Setup time		$t_s(H)$	2.0	—	2.0	—	ns	
		$t_s(L)$	2.0	—	2.0	—		
Hold time		$t_h(H)$	2.0	—	2.0	—	ns	
		$t_h(L)$	2.0	—	2.0	—		
Pulse width		$t_w$	6.0	—	6.0	—	ns	
Input capacitance		$C_{IN}$	3.0(Typ)		—		pF	$V_{IN} = V_{CC} \text{ or GND}$
Output capacitance		$C_O$	15.0(Typ)		—		pF	$V_O = V_{CC} \text{ or GND}$

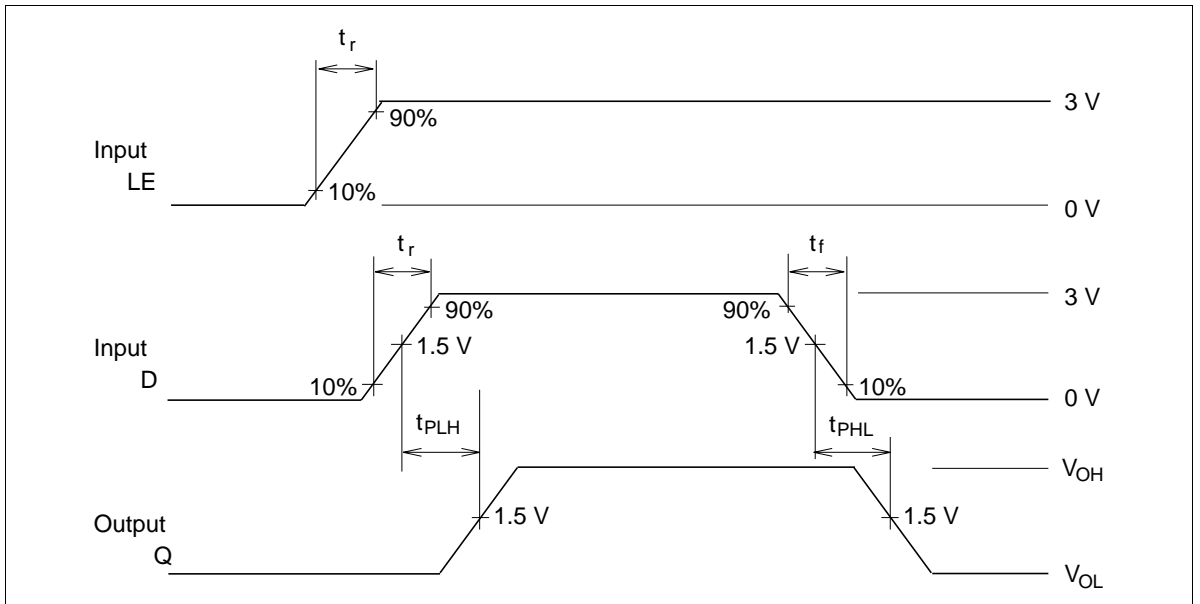
Test Circuit



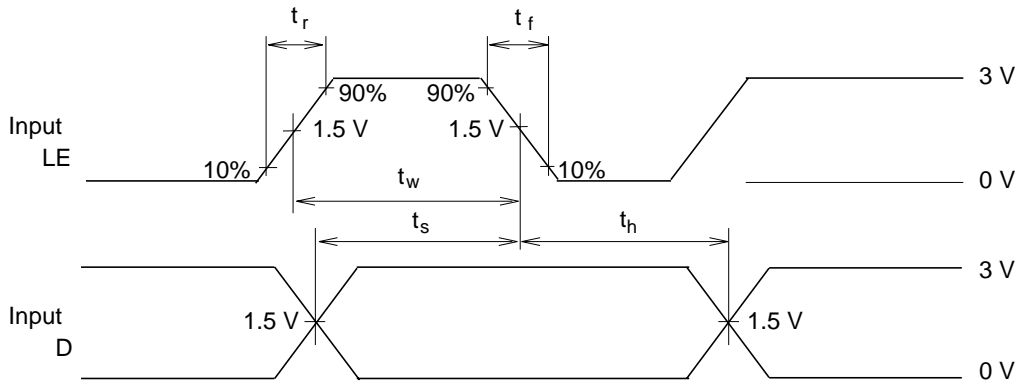
## Waveforms-1



## Waveforms-2

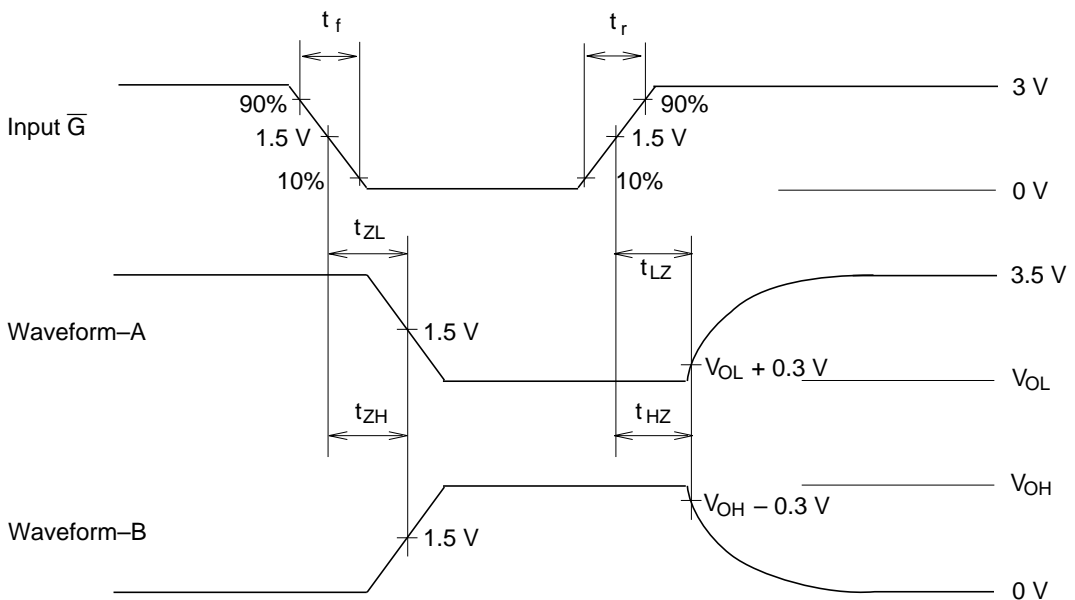


Waveforms-3



- Notes:
1.  $t_r = 2.5$  ns,  $t_f = 2.5$  ns
  2. Input waveform: PRR = 1 MHz, duty cycle 50%

Waveforms-4



- Notes:
1.  $t_r = 2.5$  ns,  $t_f = 2.5$  ns
  2. Input waveform: PRR = 1 MHz, duty cycle 50%
  3. Waveform-A shows input conditions such that the output is "L" level when enable by the output control.
  4. Waveform-B shows input conditions such that the output is "H" level when enable by the output control.

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## Package Dimensions

Unit: mm





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