HD74ALVC162834A

18-bit Universal Bus Driver with 3-state Outputs and Inverted Latch Enable

HITACHI

ADE-205-293A (Z)
2nd. Edition
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Description

The HD74ALVC162834A is an 18-bit universal bus driver designed for 2.3 V to 3.6 V V_{CC} operation.

Data flow from A to Y is controlled by the output enable ($\overline{OE}$). The device operates in the transparent mode when the latch enable ($\overline{LE}$) is low. When $\overline{LE}$ is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If the $\overline{LE}$ is high, the A data is stored in the latch/flip flop on the low to high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high impedance state.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup registor; the minimum value of the registor is determined by the current sinking capability of the driver.

All outputs, which are designed to sink up to 12 mA, include series dumping resistors to reduce overshoot and undershoot.

Features

- Supports PC133 and meets “PC SDRAM registered DIMM specification, Rev. 1.1”
- V_{CC} = 2.3 V to 3.6 V
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±12 mA (@V_{CC} = 3.0 V)
- All outputs have series dumping resistors, so no external resistors are required
- t_{pd} (CLK to Y) = 3.5 ns (Max) (@V_{CC} = 3.3±0.3 V, C_L = 50 pF, Ta = 0 to 85°C)
- t_{pd} (CLK to Y) = 2.5 ns (Max) (@V_{CC} = 3.3±0.3 V, C_L = 30 pF, Ta = 0 to 85°C)

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Function Table

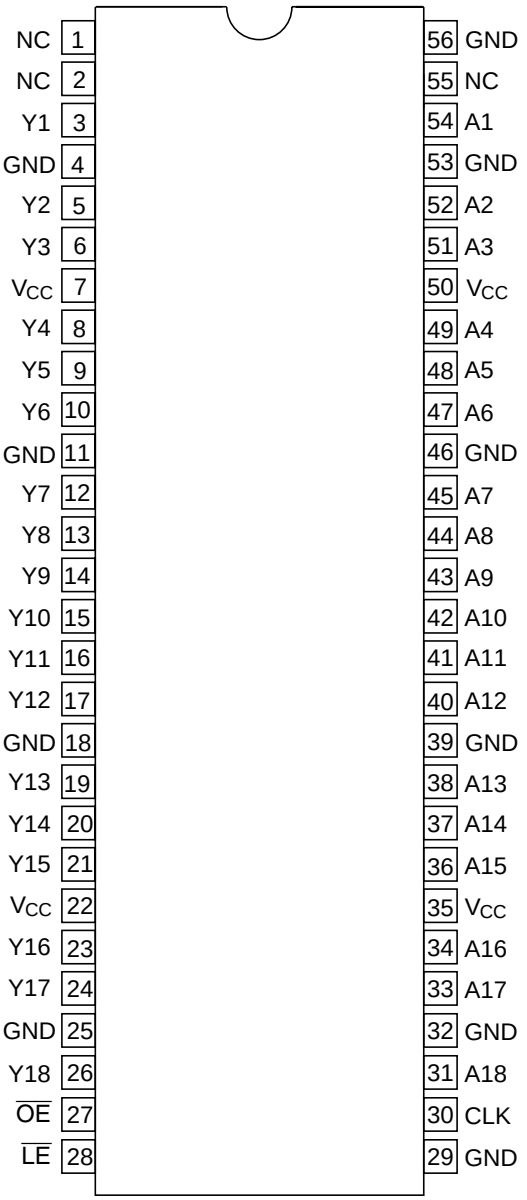
Inputs

$\overline{OE}$	$\overline{LE}$	CLK	A	Output Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0 *1

H : High level
L : Low level
X : Immaterial
Z : High impedance
↑ : Low to high transition

Note: 1. Output level before the indicated steady-state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 4.6	V	
Input voltage range [*1]	V_I	–0.5 to 4.6	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC}+0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	1	W	TSSOP
Storage temperature range	Tstg	–65 to 150	°C	

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating condition” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The input and output positive-voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.

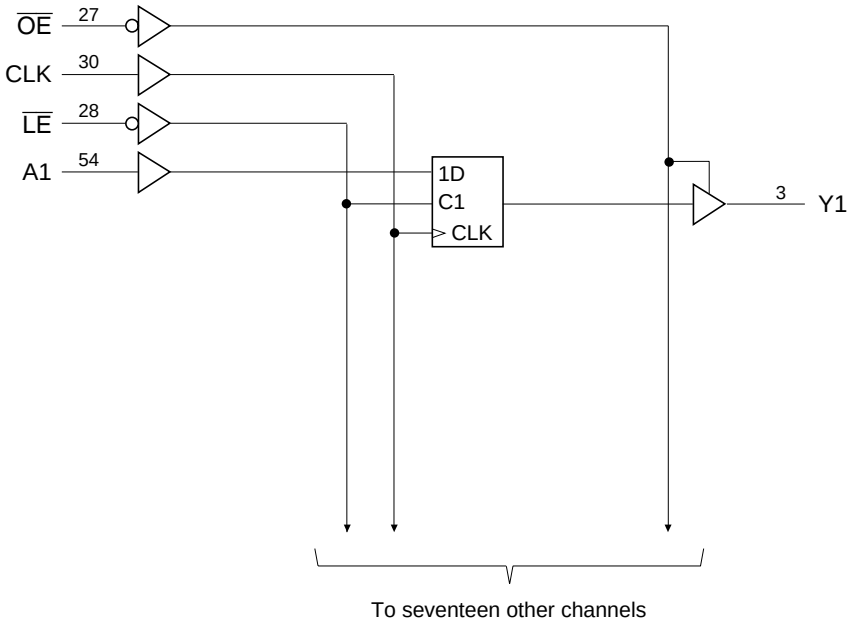
3. The maximum power dissipation is calculated using a junction temperature of 150°C and board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High-level output current	I_{OH}	—	–6	mA	V_{CC} = 2.3 V
		—	–8		V_{CC} = 2.7 V
		—	–12		V_{CC} = 3.0 V
Low-level output current	I_{OL}	—	6	mA	V_{CC} = 2.3 V
		—	8		V_{CC} = 2.7 V
		—	12		V_{CC} = 3.0 V
Input transition rise or fall rate	$\Delta t/\Delta v$	0	10	ns/V	
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating control pins must be held high or low.

Logic Diagram



Electrical Characteristics

			Ta = –40 to 85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Max**	**Unit**	**Test Conditions**
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7	V	
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	2.3 to 3.6	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.3	1.9	—		I_{OH} = –4 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		3.0	2.4	—		I_{OH} = –6 mA, V_{IH} = 2.0 V
		2.7	2.0	—		I_{OH} = –8 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
	V_{OL}	2.3 to 3.6	—	0.2	V	I_{OL} = 100 µA
		2.3	—	0.4		I_{OL} = 4 mA, V_{IL} = 0.7 V
		2.3	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.7 V
		3.0	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.8 V
		2.7	—	0.6		I_{OL} = 8 mA, V_{IL} = 0.8 V
		3.0	—	0.8		I_{OL} = 12 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5.0	µA	V_{IN} = V_{CC} or GND
Off state output current	I_{OZ}	3.6	—	±10	µA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	µA	One input at (V_{CC}–0.6)V, other inputs at V_{CC} or GND

Switching Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	From (Input)	To (Output)
Maximum clock frequency	f_{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	1.0	—	5.0	ns	A	Y
	t_{PHL}	2.7	—	—	5.0			
		3.3±0.3	1.0	—	4.2			
		2.5±0.2	1.4	—	6.3		$\overline{LE}$	Y
		2.7	—	—	6.1			
		3.3±0.3	1.4	—	5.4			
		2.5±0.2	1.4	—	6.3		CLK	Y
		2.7	—	—	6.1			
		3.3±0.3	1.4	—	5.4			
Output enable time	t_{ZH}	2.5±0.2	1.4	—	6.3	ns	$\overline{OE}$	Y
	t_{ZL}	2.7	—	—	6.5			
		3.3±0.3	1.1	—	5.5			
Output disable time	t_{HZ}	2.5±0.2	1.0	—	4.7	ns	$\overline{OE}$	Y
	t_{LZ}	2.7	—	—	4.9			
		3.3±0.3	1.3	—	4.5			
Input capacitance	C_{IN}	3.3	3.3	4.0	4.5	pF	Control inputs	
		3.3	3.0	6.0	9.0		Data inputs	
Output capacitance	C_O	3.3	3.0	7.0	9.0	pF	Y ports	

Switching Characteristics (Ta = –40 to 85°C) (cont)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	From (Input)
Setup time	t_{su}	2.5±0.2	2.2	—	—	ns	Data before CLK↑
		2.7	2.1	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	1.2	—	—		Data before $\overline{LE}$↑
		2.7	1.6	—	—		CLK “H”
		3.3±0.3	1.3	—	—		
		2.5±0.2	1.4	—	—		Data before $\overline{LE}$↑
		2.7	1.5	—	—		CLK “L”
		3.3±0.3	1.2	—	—		
Hold time	t_h	2.5±0.2	0.6	—	—	ns	Data after CLK↑
		2.7	0.6	—	—		
		3.3±0.3	0.7	—	—		
		2.5±0.2	1.2	—	—		Data after $\overline{LE}$↑
		2.7	1.1	—	—		CLK “H” or “L”
		3.3±0.3	1.1	—	—		
Pulse width	t_w	2.5±0.2	3.3	—	—	ns	$\overline{LE}$ “L”
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—		CLK “H” or “L”
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

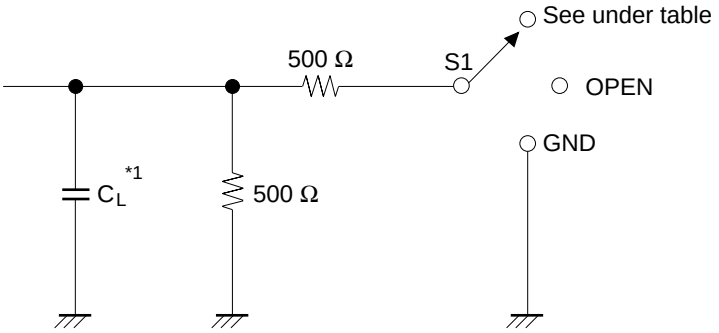
Switching Characteristics (Ta = 0 to 85°C)

Item		Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Propagation delay time	C_L=50pF	t_{PLH}, t_{PHL}	3.3±0.3	1.4	—	3.5	ns	CLK	Y
	C_L=30pF		3.3±0.3	0.7	—	2.5		CLK	Y
Setup time		t_{su}	3.3±0.3	1.0	—	—	ns	Data before CLK↑	
Hold time		t_h	3.3±0.3	0.6	—	—	ns	Data after CLK↑	

Operating Characteristics (Ta = 25°C)

Item		Symbol	V_{CC} = 2.5±0.2 V	V_{CC} = 3.3±0.3 V	Unit	Test Conditions
			Typ	Typ		
Power dissipation capacitance	Outputs enable	C_{pd}	22.0	24.5	pF	C_L = 0, f = 10 MHz
	Outputs disable		5.0	6.0		

Test Circuit

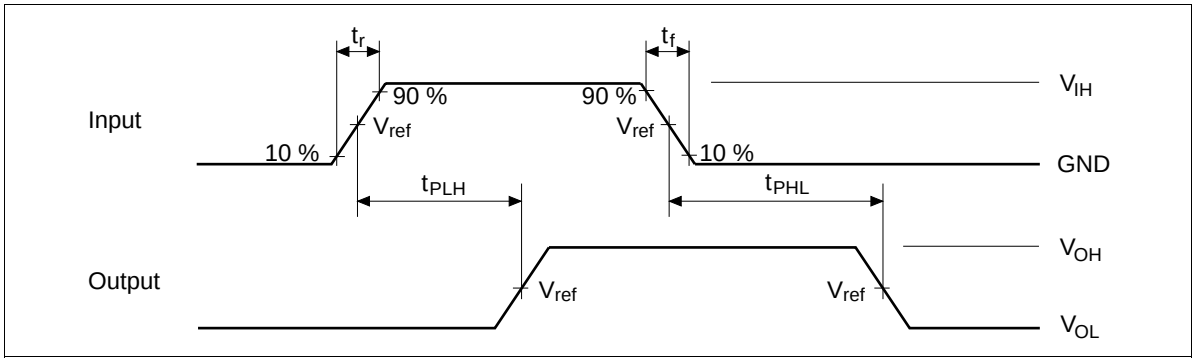


Load Circuit for Outputs

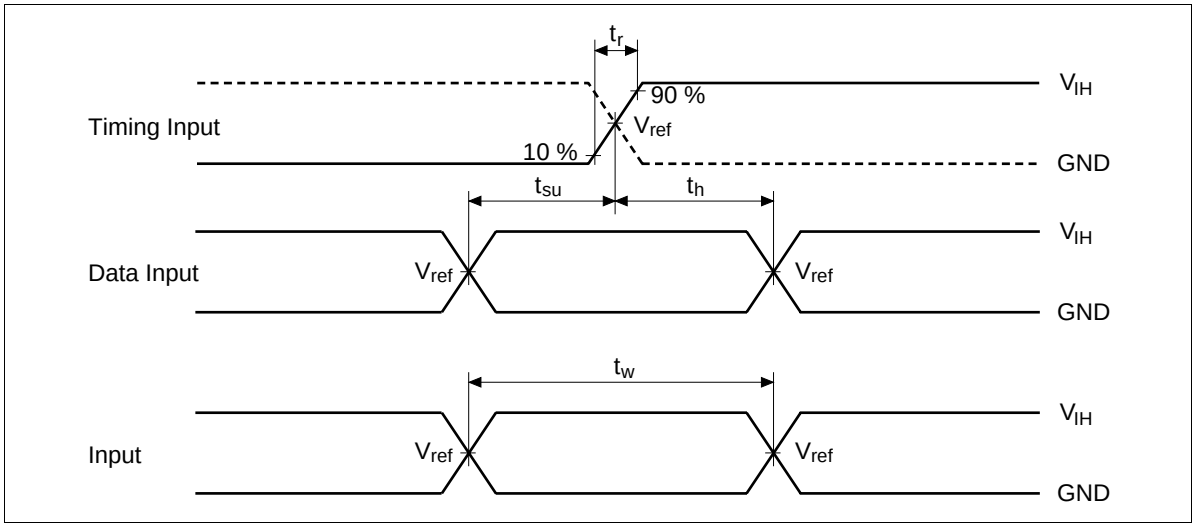
Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
t_{PLH} / t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	$2 \times V_{CC}$	6.0 V
C_L	30 pF	50 pF

Note: 1. C_L includes probe and jig capacitance.

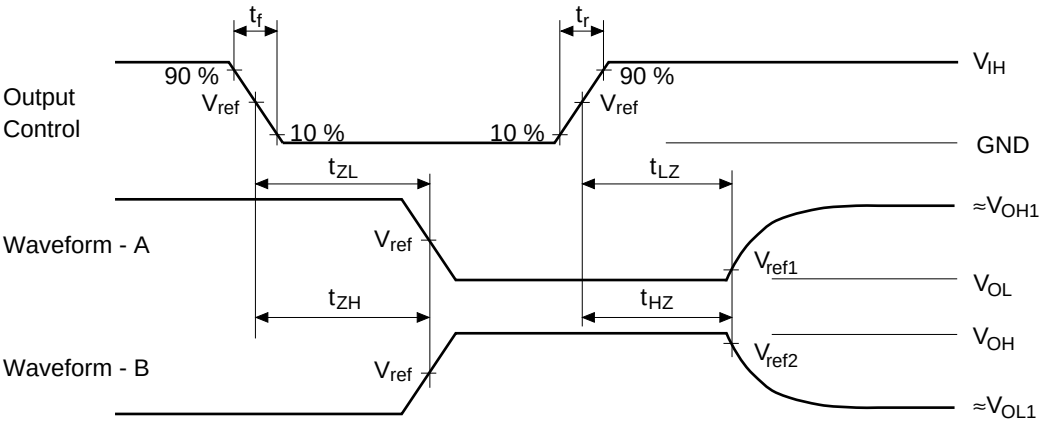
Waveforms – 1



Waveforms – 2



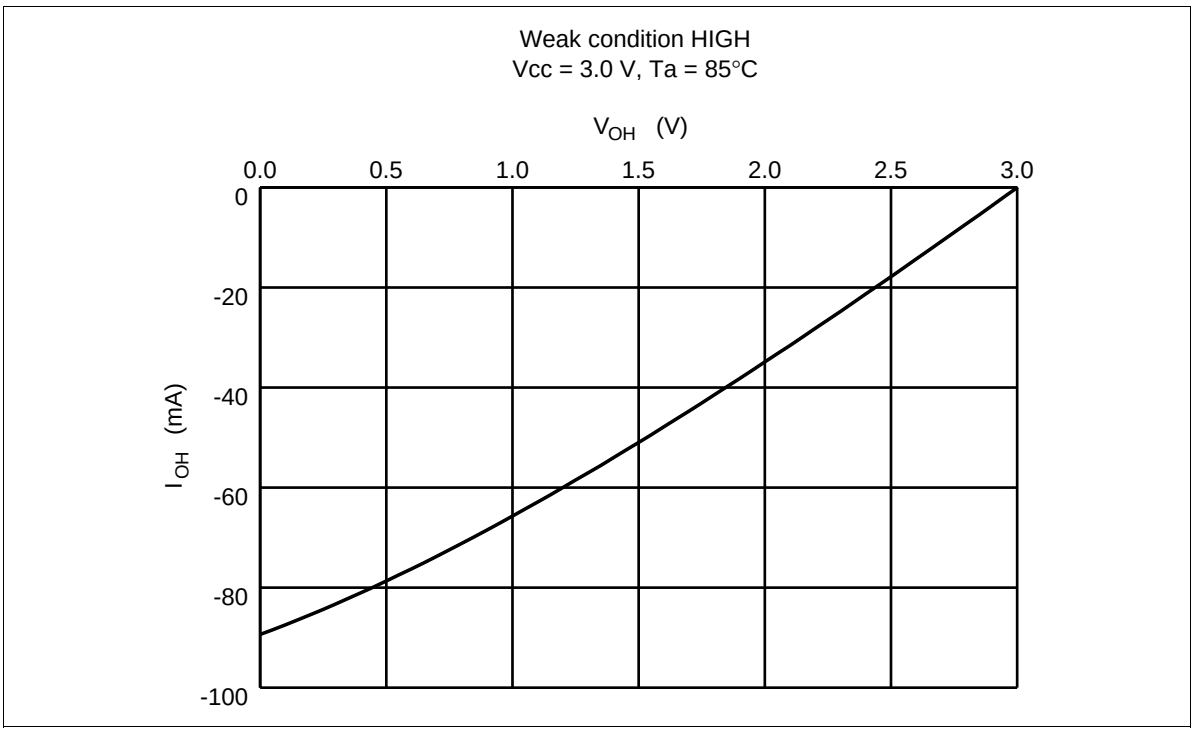
Waveforms – 3

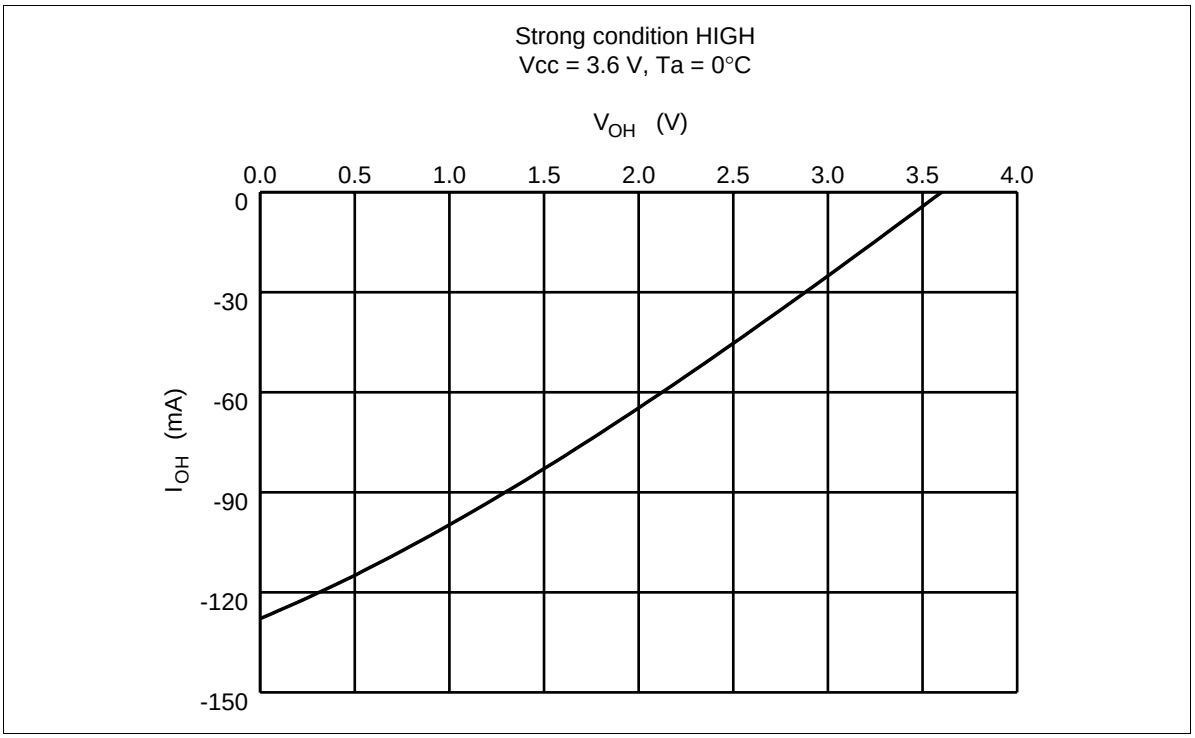


TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	V_{CC}	2.7 V
V_{ref}	1/2 V_{CC}	1.5 V
V_{ref1}	V_{OL} +0.15 V	V_{OL} +0.3 V
V_{ref2}	V_{OH}–0.15 V	V_{OH}–0.3 V
V_{OH1}	V_{CC}	3.0 V
V_{OL1}	GND	GND

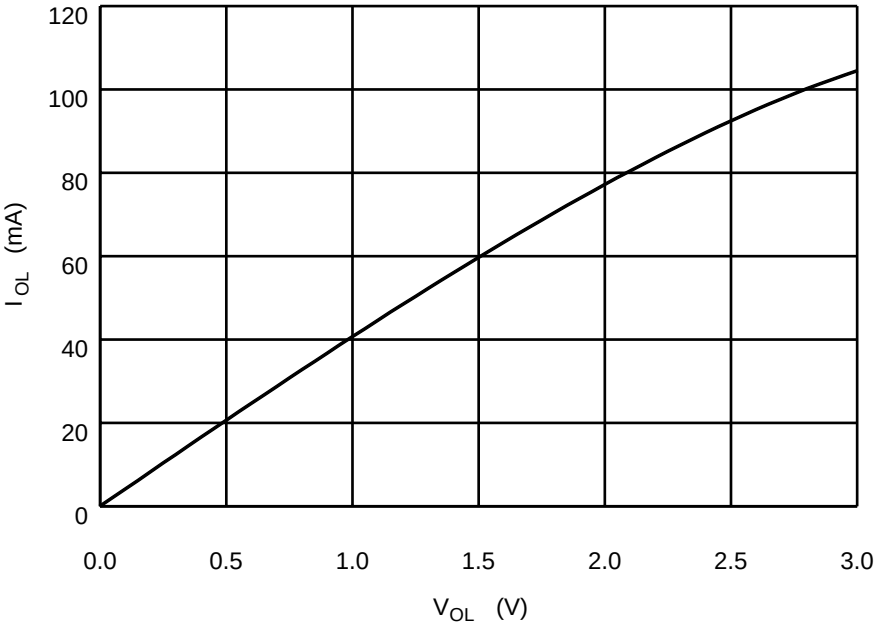
Notes:
1. All input pulses are supplied by generators having the following characteristics :
   PRR ≤ 10 MHz, Zo = 50 Ω, t_r ≤ 2.0 ns, t_f ≤ 2.0 ns. (V_{CC} = 2.5±0.2 V)
   PRR ≤ 10 MHz, Zo = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. (V_{CC} = 2.7 V, 3.3±0.3 V)
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

IV Characteristics for Register Output (Measured value)

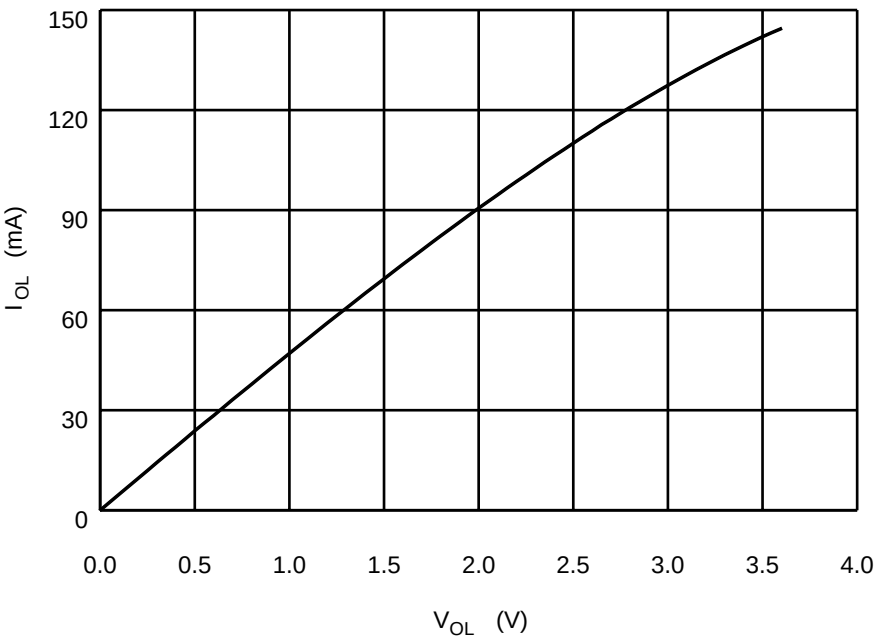




Weak condition LOW
Vcc = 3.0 V, Ta = 85°C

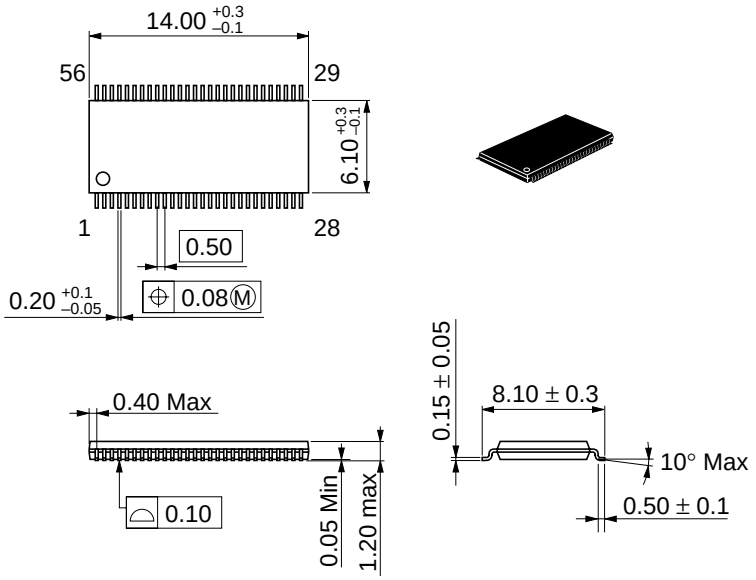


Strong condition LOW
Vcc = 3.6 V, Ta = 0°C



Package Dimensions

Unit : mm



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