HD74AC539

Dual 1-of-4 Decoder with 3-State Output

HITACHI

Description

The HD74AC539 contains two inpedendent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH (P = L) or active LOW (P = H). An active LOW input Enable (\overline{E}) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH signal on the active LOW Output Enable (\overline{OE}) input forces the 3-state outputs to the high impedance state.

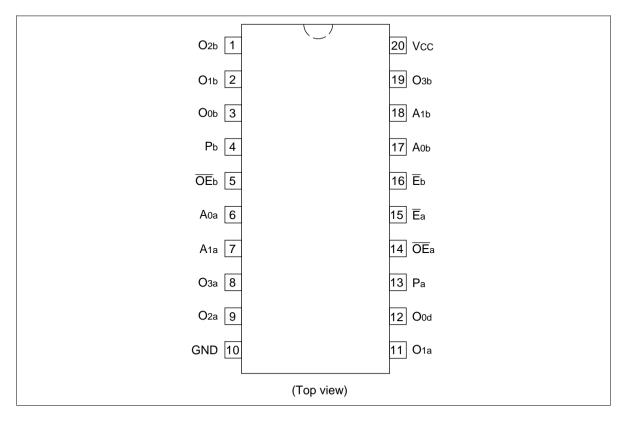
Feature

Outputs Source/Sink 24 mA

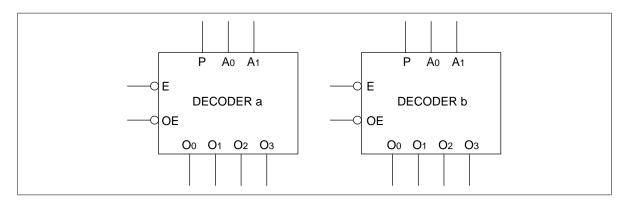


HD74AC539

Pin Arrangement



Logic Symbol



Pin Names

A_{0a} to A_{1a}	Side A Address Inputs
A_{0b} to A_{1b}	Side B Address Inputs
$\overline{E}_a - \overline{E}_b$	Enable Inputs (Active LOW)
\overline{OE}_a , \overline{OE}_b	Output Enable Inputs (Active LOW)
P_a, P_b	Polarity Control Inputs
O_{0a} to O_{3a}	Side A 3-State Outputs
O_{0b} to O_{3b}	Side B 3-State Outputs

Truth Table

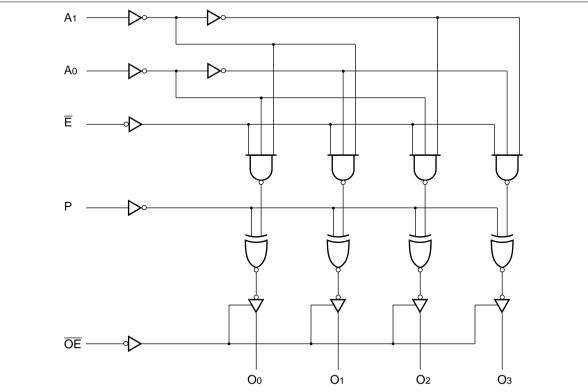
	Inputs				Outpu	uts			
Function	OE	Ē	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	
High impedance	Н	Х	Х	Х	Z	Z	Z	Z	
Disable	L	Н	Х	Х	$O_n = F$)			
Active HIGH output	L	L	L	L	Н	L	L	L	
(P = L)	L	L	L	Н	L	Н	L	L	
	L	L	Н	L	L	L	Н	L	
	L	L	Н	Н	L	L	L	Н	
Active LOW output	L	L	L	L	L	Н	Н	Н	
(P = H)	L	L	L	Н	Н	L	Н	Н	
	L	L	Н	L	Н	Н	L	Н	
	L	L	Н	Н	Н	Н	Н	L	

H: High Voltage Level
L: Low Voltage Level

X : ImmaterialZ : High Impedance

HD74AC539

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{cc}	80	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = Worst case
Maximum quiescent supply current	I _{cc}	8.0	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, $Ta = 25^{\circ}\text{C}$

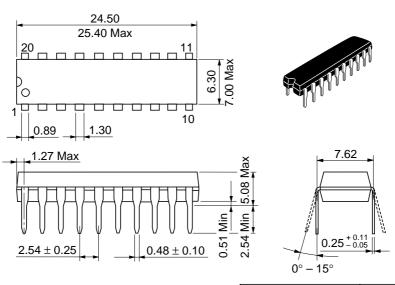
AC Characteristics: HD74AC539

			Ta = +25°C C _L = 50 pF		Ta = -40° C to $+85^{\circ}$ C C _L = 50 pF			
Item	Symbol	V _{cc} (V)*1	Min	Тур	Max	Min	Max	Unit
Propagation delay	t _{PLH}	3.3	1.0	_	15.0	1.0	18.0	ns
A_n to O_n		5.0	1.0	_	10.0	1.0	12.0	
Propagation delay	t _{PHL}	3.3	1.0		15.0	1.0	18.0	ns
A_n to O_n		5.0	1.0	_	10.0	1.0	12.0	
Propagation delay	t _{PLH}	3.3	1.0	_	14.5	1.0	16.5	ns
\overline{E} to O_{n}		5.0	1.0	_	9.5	1.0	11.0	
Propagation delay	t _{PHL}	3.3	1.0	_	13.5	1.0	15.5	ns
\overline{E} to O_{n}		5.0	1.0	_	9.0	1.0	11.5	
Propagation delay	t _{PLH}	3.3	1.0	_	16.0	1.0	19.0	ns
P to O _n		5.0	1.0	_	11.5	1.0	12.5	
Propagation delay	t _{PHL}	3.3	1.0	_	16.0	1.0	19.0	ns
P to O _n		5.0	1.0	_	11.5	1.0	12.5	
Propagation delay	t _{zH}	3.3	1.0	_	10.0	1.0	11.5	ns
\overline{OE} to O_{n}		5.0	1.0	_	8.0	1.0	9.0	
Propagation delay	t _{zL}	3.3	1.0	_	9.5	1.0	11.0	ns
\overline{OE} to O_{n}		5.0	1.0	_	7.5	1.0	8.5	
Propagation delay	t _{HZ}	3.3	1.0	_	11.5	1.0	13.0	ns
\overline{OE} to O_{\scriptscriptstylen}		5.0	1.0	_	9.5	1.0	10.5	_
Propagation delay	t _{LZ}	3.3	1.0	_	10.5	1.0	12.0	ns
OE to O _n		5.0	1.0	_	8.5	1.0	9.5	

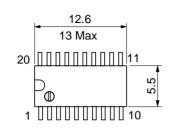
Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

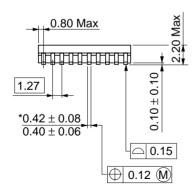
Capacitance

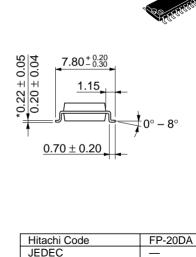
Item	Symbol	Тур	Unit	Condition	
Input capacitance	C _{IN}	4.5	pF	$V_{cc} = 5.5 \text{ V}$	
Power dissipation capacitance	C_{PD}	60	pF	$V_{CC} = 5.0 \text{ V}$	



Hitachi Code	DP-20N
JEDEC	_
EIAJ	Conforms
Weight (reference value)	1.26 g







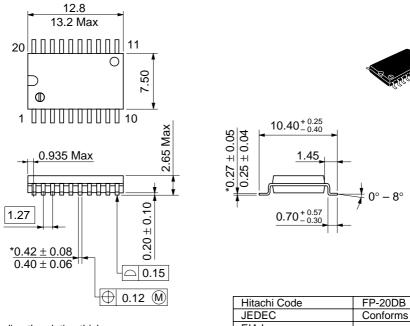
Weight (reference value)

Conforms

0.31 g

EIAJ

*Dimension including the plating thickness
Base material dimension

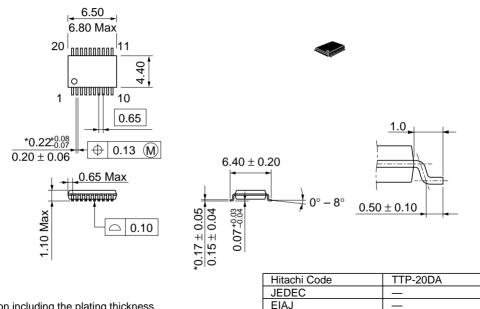


*Dimension including the plating thickness

Base material dimension

*EIAJ

Weight (reference value) 0.52 g



Weight (reference value)

0.07 g

*Dimension including the plating thickness
Base material dimension

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