GLT6100L16

Ultra Low Power 64k x 16 CMOS SRAM

May 2000(Rev. 0.3)

Features :

- Low-power consumption.
  -Active: 40mA Icc at 55ns.
  -Stand by :
  5 µA (CMOS input / output)
  1 µA (CMOS input / output, SL)
- Single +2.7 to 3.3V Power Supply.
- Equal access and cycle time.
- 55/70/85/100 ns access time.
- Tri-state output.
- Automatic power-down when deselected.
- Multiple center power and ground pins for improved noise immunity.
- Individual byte controls for both Read and Write cycles.
- Available in 44pin TSOPII Package.

Description :

The GLT6100L16 is a low power CMOS Static RAM organized as 65,536 words by 16 bits. Easy memory expansion is provided by an active LOW $\overline{\textbf{CE}}$ and $\overline{\textbf{OE}}$ pin.

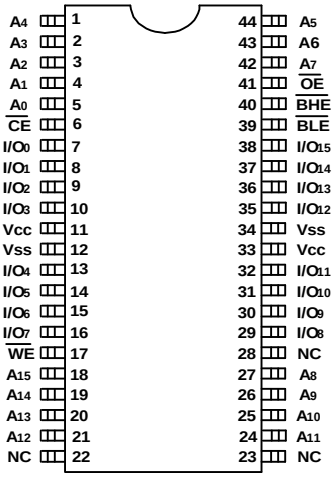
This device has an automatic power – down mode feature when deselected. Separate Byte Enable controls ($\overline{\textbf{BLE}}$ and $\overline{\textbf{BHE}}$) allow individual bytes to be accessed. BLE controls the lower bits I/O0 – I/O7. BHE controls the upper bits I/O8 – I/O15.

Writing to these devices is performed by taking Chip Enable $\overline{\textbf{CE}}$ with Write Enable $\overline{\textbf{WE}}$ and byte Enable ($\overline{\textbf{BLE}}$ / $\overline{\textbf{BHE}}$) Low.

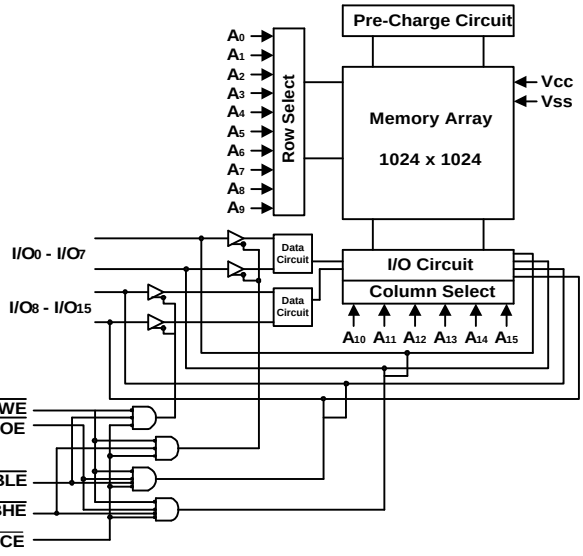
Reading from the device is performed by taking Chip Enable CE with Output enable $\overline{\textbf{OE}}$ and byte Enable ($\overline{\textbf{BLE}}$ / $\overline{\textbf{BHE}}$) Low while Write Enable $\overline{\textbf{WE}}$ is held HIGH.

Pin Configurations :

GLT6100L16



Function Block Diagram :



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Pin Descriptions:

Name	Function
$A_0 – A_{15}$	Address Inputs
$\overline{CE}_1$ and CE_2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$I/O_0 – I/O_{15}$	Data Input and Data Output
V_{CC}	3V Power Supply
GND	Ground
NC	No Connection

Truth Table:

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O0-I/O7	I/O8-I/O15	Power	Mode
H	X	X	X	X	High-Z	High-Z	Standby	Standby
L	L	H	L	H	Data Out	High-Z	Active	Low byte Read
L	L	H	H	L	High-Z	Data Out	Active	High Byte Read
L	L	H	L	L	Data Out	Data Out	Active	Word Read
L	X	L	L	L	Data In	Data In	Active	Word Write
L	X	L	L	H	Data In	High-Z	Active	Low Byte Write
L	X	L	H	L	High-Z	Data In	Active	High byte Write
L	H	H	X	X	High-Z	High-Z	Active	Output Disable
L	X	X	H	H	High-Z	High-Z	Active	Output Disable

Absolute Maximum Ratings*

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	4.6	V
Power Dissipation	P_T	-	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	°C
Temperature Under Bias	Tbias	-40	+85	°C

*Note : Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions (TA = -25°C to + 85°C**)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
	V_{IL}	-0.5*	-	0.6	V

* V_{IL} min = -2.0V for pulse width less than $t_{RC}/2$.
** For Industrial Temperature.

DC Operating Characteristics (Vcc=2.7 to 3.3V , T_A =-25°C to + 85°C)

Parameter	Sym.	Test Conditions		55		70		85		100		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, Vin = Gnd to V_{CC}			1		1		1		1	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}$ =V_{IH} or V_{CC} = Max, V_{OUT} = Gnd to V_{CC}			1		1		1		1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}$ =V_{IL} ,V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0			3		3		3		3	mA
Average Operating Current	I_{CC1}	I_{OUT} = 0mA, Min Cycle, 100% Duty			40		35		30		30	mA
	I_{CC2}	$\overline{CE}$ ≤ 0.2V I_{OUT} = 0mA, Cycle Time=1µs, 100% = Duty			3		3		3		3	mA
Standby Power Supply Current(TTL Level)	I_{SB}	$\overline{CE}$ =V_{IH}			0.5		0.5		0.5		0.5	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE}$ ≥ V_{CC}-0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}-0.2V	GLT6100L16LL		5		5		5		5	µA
			GLT6100L16SL		1		1		1		1	µA
Output Low Voltage	V_{OL}	I_{OL} = 2 mA			0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA		2.4		2.4		2.4		2.4		V

Data Retention

Parameter	Sym.	Test Conditions	Min.	Max.	Unit
V_{CC} for Data retention	V_{DR}	$\overline{CE}$ ≥ V_{CC} -0.2V	2.0	-	V
Data Retention Current	I_{CCDR}			1	µA
Chip Deselect to Data Retention Time	t_{CDR}	V_{IN} ≥ V_{CC} -0.2V or	0	-	ns
Operating Recovery Time(2)	t_R	V_{IN} ≤ 0.2V	t_{RC}	-	ns

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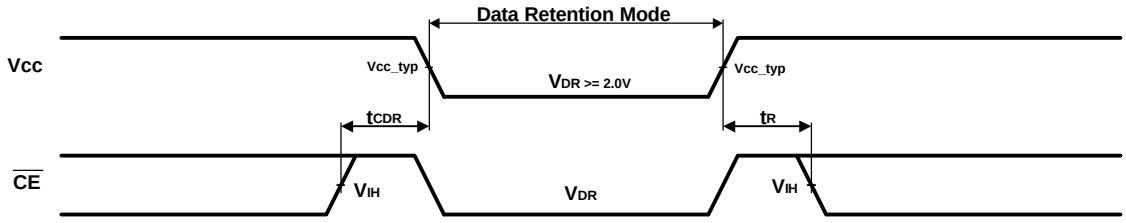
Data Retention Waveform (TA = -25°C to + 85°C)

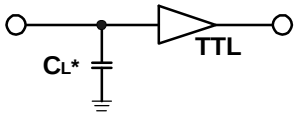


AC Test Conditions

Input Pulse Levels	0.6V to 2.2V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.4V

Output Load Condition
55ns / 70ns / 85ns C_L = 30pf + 1TTL Load
Load 100ns C_L = 100pf + 1TTL Load

AC Test Loads and Waveforms

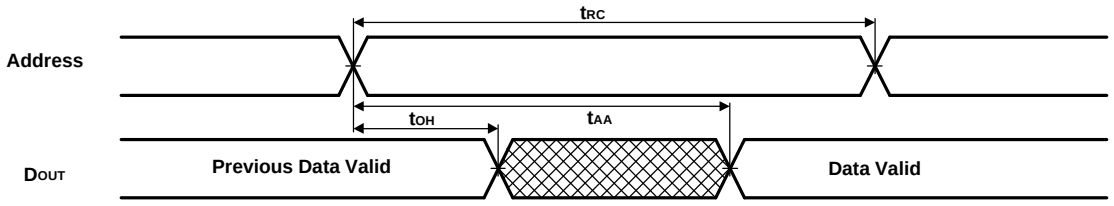


*Including Scope and Jig Capacitance

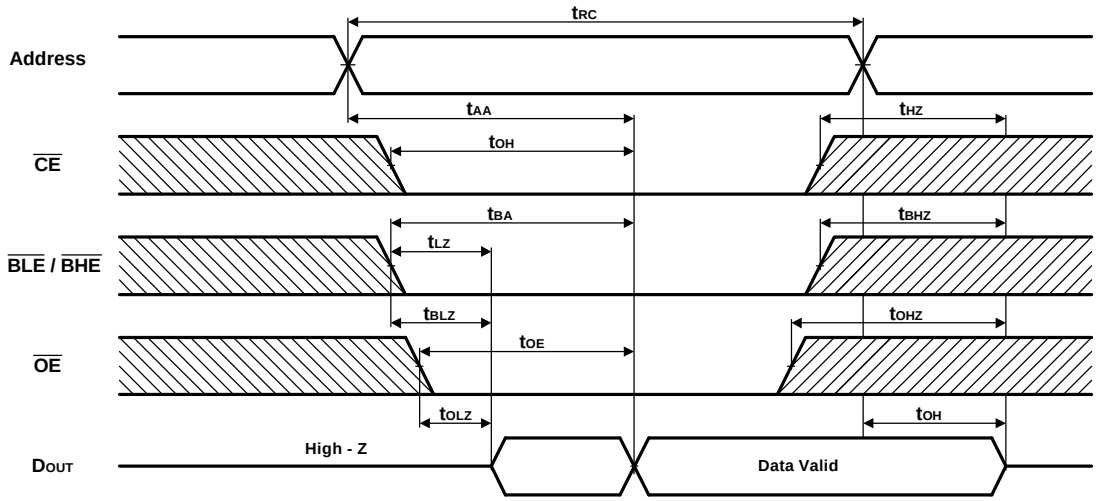
Read Cycle (9)(Vcc=2.7V to 3.3V, T_A = -25°C to + 85°C)

Parameter	Symbol	55		70		85		100		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	55		70		85		100		ns	
Address Access Time	t_{AA}		55		70		85		100	ns	
Chip Enable Access Time	t_{ACE}		55		70		85		100	ns	
Output Enable Access Time	t_{OE}		35		40		40		50	ns	
Output Hold from address Change	t_{OH}	10		10		10		10		ns	
Chip Enable to Output in Low-Z	t_{LZ}	10		10		10		10		ns	4,5
Chip Disable to Output in High-Z	t_{HZ}		25		30		35		40	ns	3,4,5
Output Enable to Output in Low-Z	t_{OLZ}	5		5		5		5		ns	
Output Disable to Output in High-Z	t_{OHZ}		25		25		30		35	ns	
$\overline{BLE}$, $\overline{BHE}$ Enable to Output in Low-Z	t_{BLZ}	5		5		5		5		ns	4,5
$\overline{BLE}$, $\overline{BHE}$ Disable to Output in High-Z	t_{BHZ}		25		25		30		35	ns	3,4,5
$\overline{BLE}$, $\overline{BHE}$ Access Time	t_{BA}		35		40		40		50	ns	

Timing Waveform of Read Cycle 1 (Address Controlled)



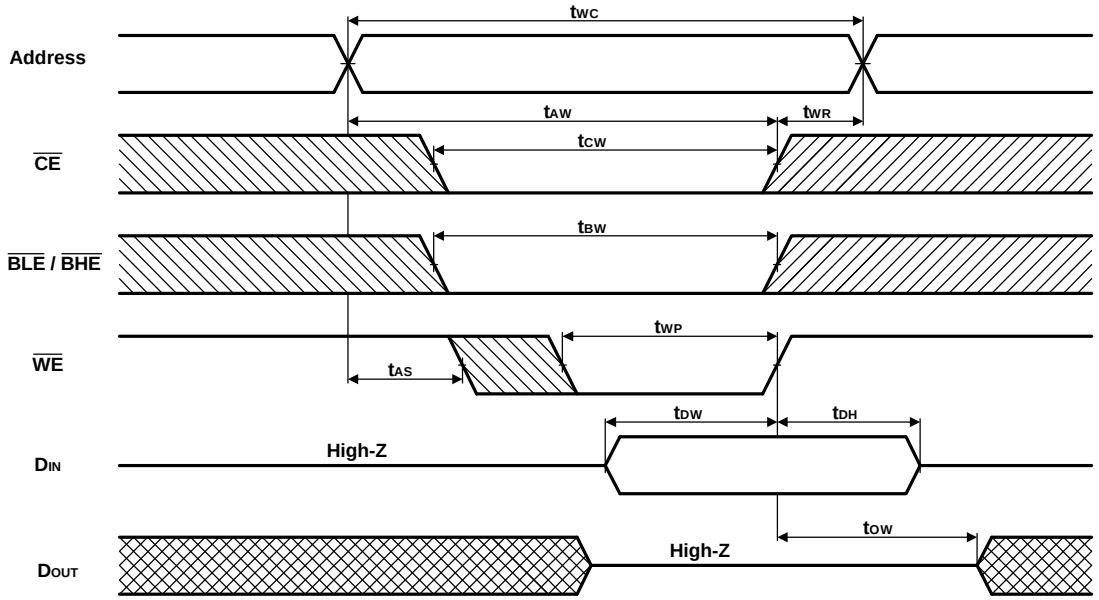
Timing Waveform of Read Cycle 2 (14~16)



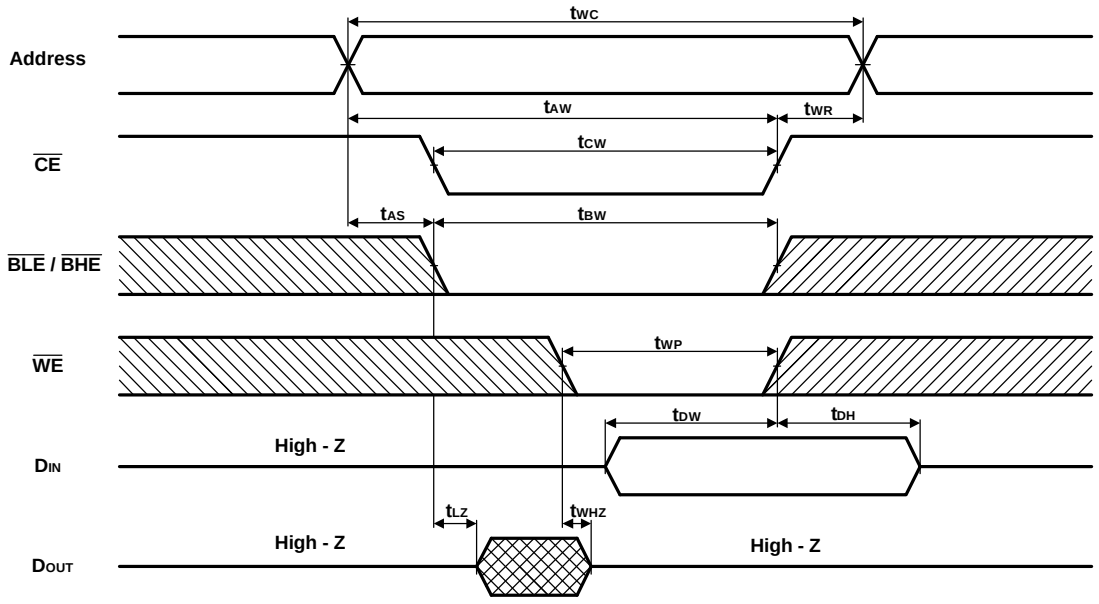
Write Cycle (11)(Vcc=2.7V to 3.3V, T_A = -25°C to + 85°C)

Parameter	Symbol	55		70		85		100		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	55		70		85		100		ns	
Chip Enable to Write End	t_{CW}	50		60		70		80		ns	
Address Setup to Write End	t_{AW}	50		60		70		80		ns	
Address Setup Time	t_{AS}	0		0		0		0		ns	
Write Pulse Width	t_{WP}	45		50		60		70		ns	
Write Recovery Time	t_{WR}	0		0		0		0		ns	
Data Valid to Write End	t_{DW}	25		30		35		40		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enable to Output in High-Z	t_{WHZ}		25		30		35		40	ns	
Output Active from Write End	t_{OW}	5		5		5		5		ns	
$\overline{BLE}$, $\overline{BHE}$ Setup to Write End	t_{BW}	50		60		70		80		ns	

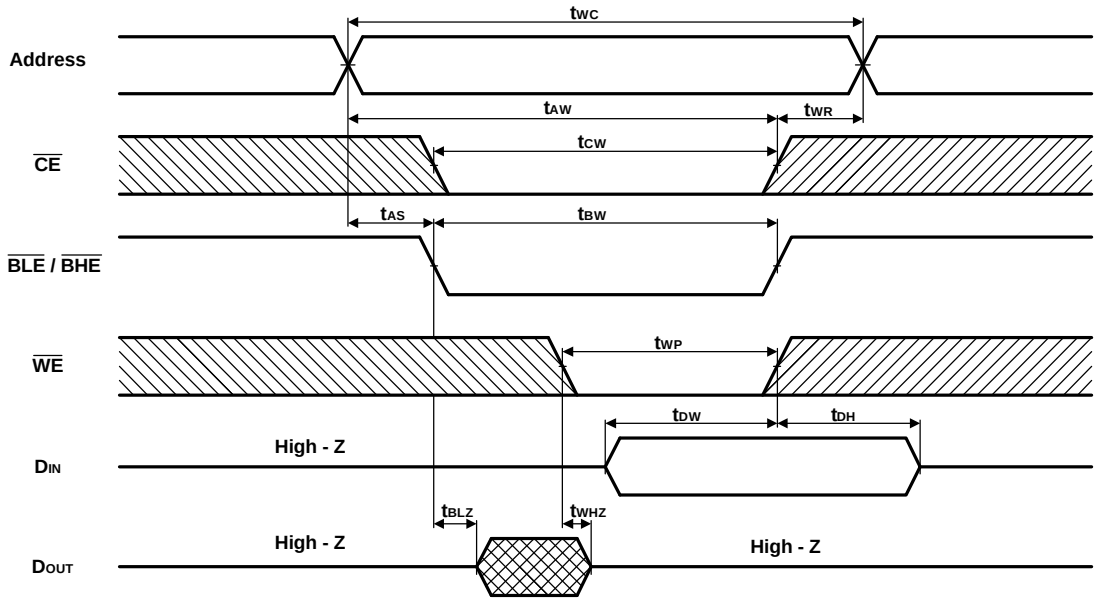
Timing Waveform of Write Cycle 1 (Address Controlled)(22~25,28)



Timing Waveform of Write Cycle 2 ($\overline{CE}$ Controlled)(22~26,28)



Timing Waveform of Write Cycle 3 ($\overline{BLE}$ / $\overline{BHE}$ Controlled)[22~26,28]



Notes :

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see AC Test Condition.
4. This parameter is tested with CL = 5pF. Transition is measured ± 500mV from steady – state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.
12. $\overline{WE}$ are high for read cycle.
13. All read cycle timing is referenced from the last valid address to the first transition address.
14. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition referenced to V_{OH} or V_{OL} levels.
15. At any given temperature and voltage condition t_{HZ}(max.) is less than t_{LZ} (min.) both for a given device and from device to device.
16. Transition is measured ± 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
17. Device is continuously selected with $\overline{CE}$ = V_{IL}.
18. Address valid prior to coincident with $\overline{CE}$ transition Low.
19. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read write cycle.
20. For test conditions, see AC Test Condition.
21. All write timing is referenced from the last valid address to the first transition address.
22. A write occurs during the overlap of a low $\overline{CE}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CE}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CE}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
23. t_{CW} is measured from the later of $\overline{CE}$ going low to end of write.
24. t_{AS} is measured from the address valid to the beginning of write.
25. t_{WR} is measured from the end of write to the address change.
26. If $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output Low-Z state.
27. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
28. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
29. D_{OUT} is the read data of the new address.
30. When $\overline{CE}$ is low : I/O pins are in the outputs state. The input signals in the opposite phase leading to the output should not be applied.
31. For test conditions, see AC Test Condition.

Ordering Information

Part Number	*SPEED*	*POWER*	*PACKAGE*
GLT6100L16LL-55TC	55ns	Normal	TSOPII 32L
GLT6100L16LL-70TC	70ns	Normal	TSOPII 32L
GLT6100L16LL-85TC	85ns	Normal	TSOPII 32L
GLT6100L16LL-100TC	100ns	Normal	TSOPII 32L
GLT6100L16SL-55TC	55ns	Normal	TSOPII 32L
GLT6100L16SL-70TC	70ns	Normal	TSOPII 32L
GLT6100L16SL-85TC	85ns	Normal	TSOPII 32L
GLT6100L16SL-100TC	100ns	Normal	TSOPII 32L

Parts Numbers (Top Mark) Definition :

GLT 6 100 L 16 LL- 55 TC

4 : DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM

-SRAM
064 : 64K
256 : 256K
512 : 512K
100 : 1M
-DRAM
10 : 1M(C/EDO)*
11 : 1M(C/FPM)*
12 : 1M(H/EDO)*
13 : 1M(H/FPM)*
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
*See note

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.1V

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

SPEED
-SRAM
10 : 10ns
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
ST : sTSOP (Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP

LL : Low Low power
L : Low power
SL : Super Low power

Note : C→CDROM , H→HDD.
Example :
1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

44 pin Small Outline J-form Package (TSOPII)