# *GENLINX™ II* GX9533
## Serial Digital 8x9 Crosspoint

DATA SHEET



### FEATURES

- **operation beyond 622Mb/s**
- **accepts SMPTE and PECL input levels**
- **fully differential signal path**
- **on-chip PECL current loads eliminate need for external pull-down resistors**
- **capable of driving 100Ω differential loads**
- **very low 500mW power consumption**
- **additional expansion port input for construction of larger matrices**
- **auxiliary monitoring output**
- **easy to configure**
- **double latched address inputs with separate load and configure**
- **TTL/CMOS compatible control logic inputs**
- **single 5V power supply**

### APPLICATIONS

Serial digital video switching; datacom or telecom switching.

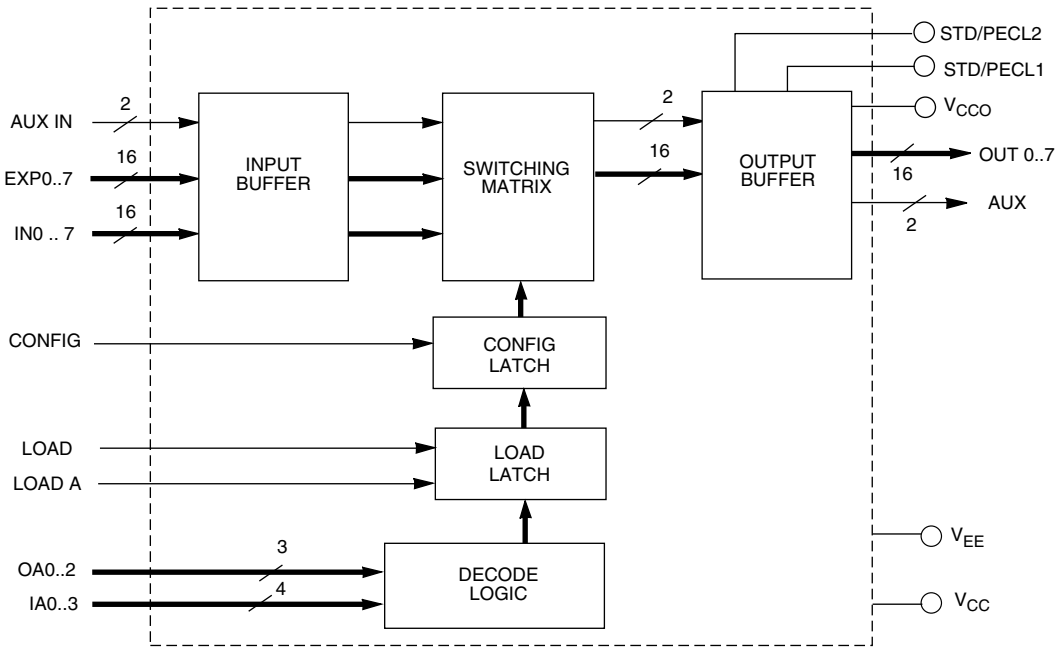
### DESCRIPTION

The GX9533 is a high speed 8x9 serial digital crosspoint. An expansion input port eases the design of larger switching matrices by reducing PCB layers and eliminating the need for cascaded secondary switching. Decode logic and double level latching to configure the matrix are included on chip. Separate LOAD and CONFIGURE inputs allow for asynchronous configuration and synchronous switching. These latches can also be made transparent for asynchronous switching by pulling the LOAD and CONFIGURE pins high.

In the power saving (PS) mode, the GX9533 has a very low power consumption of 500mW. This is accomplished by driving a 400mV output swing into the on-chip 200Ω differential load termination in the expansion port of the next GX9533. This architecture provides a significant power savings and the elimination of external load resistors or impedance matching resistors. In applications where standard PECL levels are necessary, the GX9533 can be configured in "PECL Mode", to drive 800mV p-p into a 100Ω differential load. The power consumption in this mode increases to 860mW.

### ORDERING INFORMATION

| PART NUMBER | PACKAGE | TEMPERATURE |
|---|---|---|
| GX9533-CQY | 100 pin MQFP Tray | 0°C to 70°C |
| GX9533-CTY | 100 pin MQFP Tape | 0°C to 70°C |




**BLOCK DIAGRAM**



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## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | VALUE |
|---|---|
| Supply Voltage ($V_S = V_{CC}$-$V_{EE}$) | 5.5V |
| Input Voltage Range (any input) | -0.3 to ($V_{CC}$+0.3)V |
| Power Dissipation | 975mW |
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature Range (soldering, 10 sec) | 260°C |

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5V, $V_{EE}$ = 0V, $T_A$ = 0 to 70°C unless otherwise shown.

| PARAMETER | | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | | | 4.75 | 5.0 | 5.25 | V |
| ECL Input Voltage Swing | | | 200 | 800 | 1200 | mV p-p |
| ECL Common Mode Input Voltage Range | | with 1200mV input signal swing | 2500 | - | $V_{CC}$-600 | mV |
| Logic Input Voltage | High | | 2.0 | - | $V_{CC}$ | V |
| | Low | | 0 | - | 0.8 | V |

## POWER SAVE 1 MODE

$R_{SET}$ = 4kΩ

| PARAMETER | | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current | | $R_L$ = 100Ω | - | 115 | 150 | mA |
| Output Common Mode Voltage | | | $V_{CC}$-1200 | - | $V_{CC}$-800 | mV |
| Output Voltage Swing | | | 300 | 450 | 600 | mV |
| Output Voltage | High | | $V_{CC}$-950 | - | $V_{CC}$-600 | mV |
| | Low | | $V_{CC}$-1400 | - | $V_{CC}$-1000 | mV |

## POWER SAVE 2 MODE

$R_{SET}$ = 6kΩ

| PARAMETER | | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current | | $R_L$ = 200Ω | - | 100 | 130 | mA |
| Output Common Mode Voltage | | | $V_{CC}$-1200 | - | $V_{CC}$-800 | mV |
| Output Voltage Swing | | | 300 | 450 | 600 | mV |
| Output Voltage | High | | $V_{CC}$-950 | - | $V_{CC}$-600 | mV |
| | Low | | $V_{CC}$-1400 | - | $V_{CC}$-1000 | mV |

## PECL MODE

$R_{SET}$ = 2kΩ

| PARAMETER | | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current | | $R_L$ = 100Ω | - | 170 | 185 | mA |
| Output Common Mode Voltage | | | $V_{CC}$-1450 | - | $V_{CC}$-1050 | mV |
| Output Voltage Swing | | | 700 | 800 | 900 | mV |
| Output Voltage | High | | $V_{CC}$-1200 | - | $V_{CC}$-650 | mV |
| | Low | | $V_{CC}$-1850 | - | $V_{CC}$-1450 | mV |



## AC ELECTRICAL CHARACTERISTICS

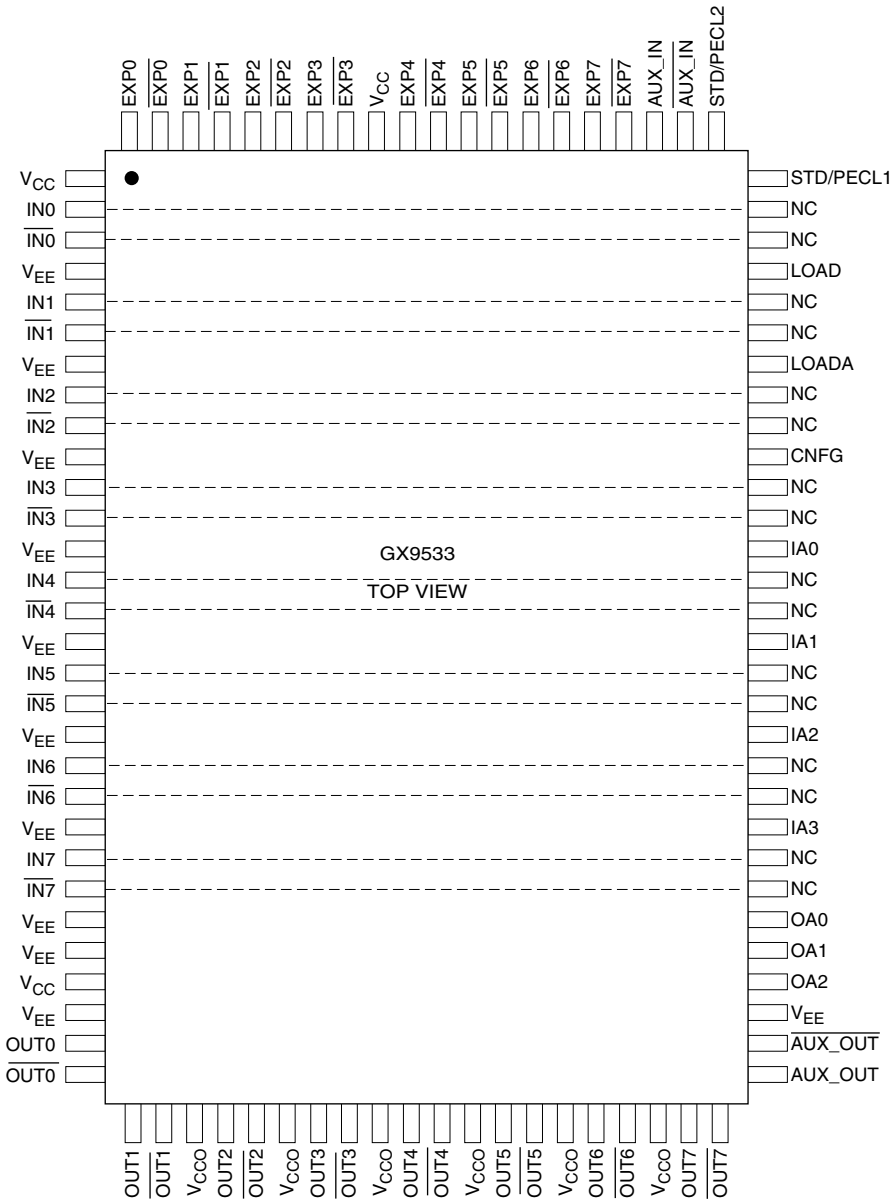
$V_{CC}$ = 5.0V, $V_{EE}$ = 0V, $T_A$ = 0 to 70°C unless otherwise shown.

| PARAMETER | | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Maximum Input Data Rate | | | For 90% eye opening | - | 850 | - | Mb/s |
| Additive Jitter | Standard Input | | 143 to 622 Mb/s, all hostile crosstalk | - | 80 | - | ps p-p |
| | Expansion Input | | | - | 70 | - | ps p-p |
| Data In to Data Out Delay | Standard Input | $t_{DLY}$ | Average of all channels | - | 1.7 | - | ns |
| | Expansion Input | | | - | 1.1 | - | ns |
| Propagation Delay Match | Standard Input | | | - | 350 | - | ps |
| | Expansion Input | | | - | 250 | - | ps |
| CONFIGURE to Data Out Delay | Main Out | $t_{CD}$ | | - | 10 | - | ns |
| | AUX Out | | | - | 11 | - | ns |
| LOAD/LOADA Pulse Width | | $t_{LP}$ | | 20 | - | - | ns |
| CONFIGURE Pulse Width | | $t_{CP}$ | | 20 | - | - | ns |
| $IA_N$ to LOAD/LOADA High Setup Time | | $t_{ILS}$ | | 30 | - | - | ns |
| LOAD/LOADA to $IA_N$ Low Hold Time | | $t_{ILH}$ | | 0 | - | - | ns |
| $OA_N$ to LOAD High Setup Time | | $t_{OLS}$ | | 30 | - | - | ns |
| LOAD to $OA_N$ Low Hold Time | | $t_{OLH}$ | | 0 | - | - | ns |
| LOAD High to CONFIGURE High | | $t_{LC}$ | | 0 | - | - | ns |
| Output Rise/Fall Time | | | | - | 700 | - | ps |

NOTE

1. Use RMS addition to calculate additive jitter through cascaded devices.

## PIN CONNECTIONS




## PIN DESCRIPTIONS

| SYMBOL | TYPE | DESCRIPTION |
|---|---|---|
| IN0 to IN7, $\overline{IN0}$ to $\overline{IN7}$ | I | Differential data inputs. |
| OUT0 to OUT7, $\overline{OUT0}$ to $\overline{OUT7}$ | O | Differential data outputs. |
| AUX_OUT, $\overline{AUX\_OUT}$ | O | Auxiliary port output. |
| AUX_IN, $\overline{AUX\_IN}$ | I | Auxiliary port input. |
| OA0 to OA2 | I | Output address select. |
| IA0 to IA3 | I | Input address select. |
| LOAD | I | Loads input & output address. |
| LOADA | I | Loads auxiliary input address. |
| STD/ECL1, STD/ECL2 | | Resistor connection for Power Save mode or PECL mode. Refer to Table 3. |

## PIN DESCRIPTIONS

| SYMBOL | TYPE | DESCRIPTION |
|---|---|---|
| CNFG | I | Switch configuration. |
| EXP0 to EXP7, $\overline{EXP0}$ to $\overline{EXP7}$ | I | Expansion port inputs. |
| $V_{CC}$ | | Positive power supply. |
| $V_{CCO}$ | | Positive power supply (PECL outputs). |
| $V_{EE}$ | | Negative power supply. |

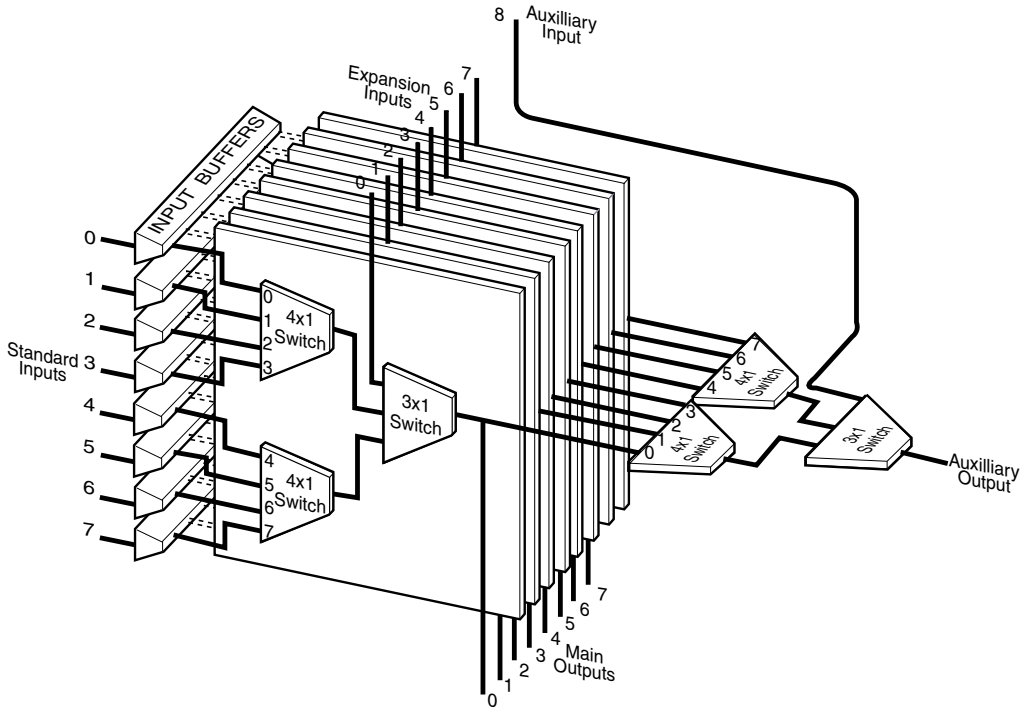



Fig. 1 Data Flow Diagram

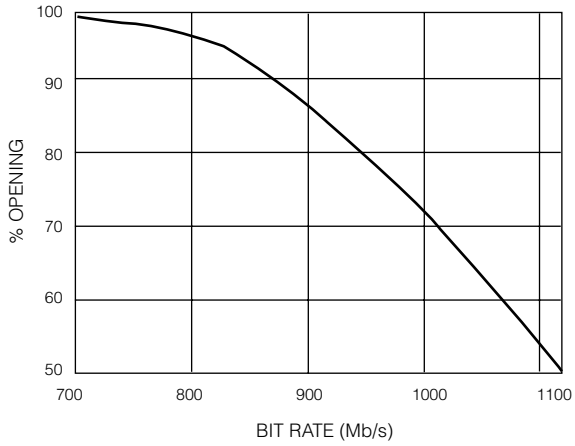



Fig. 2 Typical Eye Opening vs. Bit Rate

## DETAILED DESCRIPTION

### DIFFERENTIAL INPUTS

The inputs to the GX9533 will accept both SMPTE 259M as well as PECL input levels. The fully differential data path provides low jitter data rates of up to 700Mb/s.

The main inputs (IN0..7) and expansion inputs (EXP0..7) are normally connected to a biased differential data source. The GX9533 inputs are not self biased, so unused inputs should be connected as shown in Figure 3 or Figure 4.

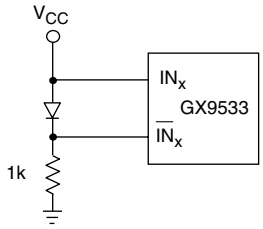



Fig. 3 Preferred Termination Of Unused Inputs

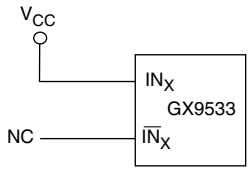



Fig. 4 Alternate Termination of Unused Inputs

Terminating the inputs as shown in Figure 3 will provide the highest noise immunity, since there is no possibility of noise coupling into the unconnected input pin.

### I/O ADDRESS SELECTION

The GX9533 has a versatile LOAD/CONFIGURE architecture which simplifies IN/OUT switch configuration.

An output is normally connected to an input by a two stage process:

#### Stage One: Loading The Configuration Into Latches

1. The output address is selected on the OA pins as shown in Table 1.
2. The input address is selected on the IA pins as shown in Table 2.
3. A LOAD pulse then transfers the output and input addresses into the GX9533 LOAD latch.

The above three steps can be repeated up to eight times in order to configure the latch for all eight outputs.

During step 3 above, if the LOADA pulse is also strobed, the latch is configured to connect the selected input to the ninth, auxiliary output.

TABLE 1: Output Address Selection

| OA2 | 0A1 | 0A0 | OUTPUT PORT |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

TABLE 2: Input Source Address Selection

| IA3 | IA2 | IA1 | IA0 | INPUT PORT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | X | X | EXP |
| 1 | 1 | X | X | Quiet Mode |

Note that a QUIET mode is available as shown in Table 2. In QUIET mode, the outputs are latched in a DC state with $OUT_X = 1$ and $\overline{OUT}_X = 0$.

#### Stage Two: Configuring The Matrix

A CONFIGURE strobe is applied to transfer the contents of the LOAD latch into the CONFIG latch. This action will cause the data flow through the GX9533 to be switched to the new configuration. Refer to Figure 6 for detailed timing information.

Note that any single output can be asynchronously switched by having LOAD (or LOADA if desired) held high while CONFIG is strobed.

### OUTPUT LEVEL SELECT

A single resistor, $R_{SET}$, is used to set the amplitude of all differential outputs. Table 3 shows the value of $R_{SET}$ vs output drive capability.

TABLE 3: $R_{SET}$ vs $V_{OUT}$

| $R_{SET}$ | $V_{OUT}$ (mV) | OUTPUT $R_L$ | MODE |
|---|---|---|---|
| 2k | 800 | 100 | PECL |
| 4k | 450 | 100 | Power Save 1 |
| 6k | 450 | 200 | Power Save 2 |

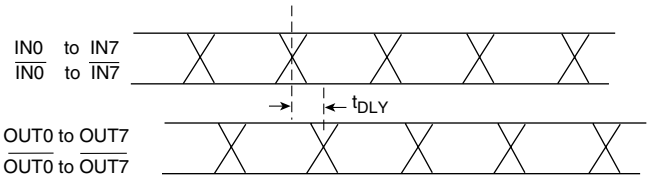



Fig. 5 GX9533 Data Latency

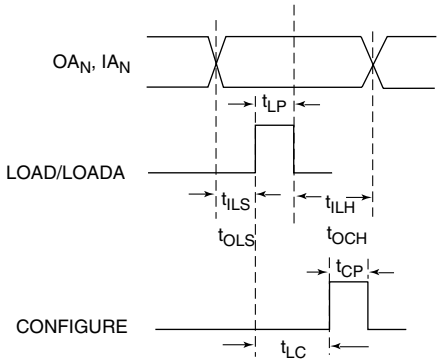



Fig. 6 LOAD/LOADA and Configure Timing

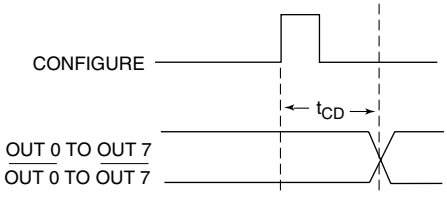



Fig. 7 Configure to Data Out Delay

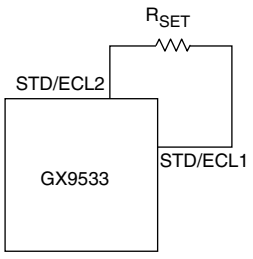



Fig. 8 GX9533 $R_{SET}$ Connection

## USING THE GX9533 TO EXPAND LARGER MATRICES

The GX9533 pin-out and architecture provides a number of advantages over other crosspoint switches in the area of switching matrix board layout.

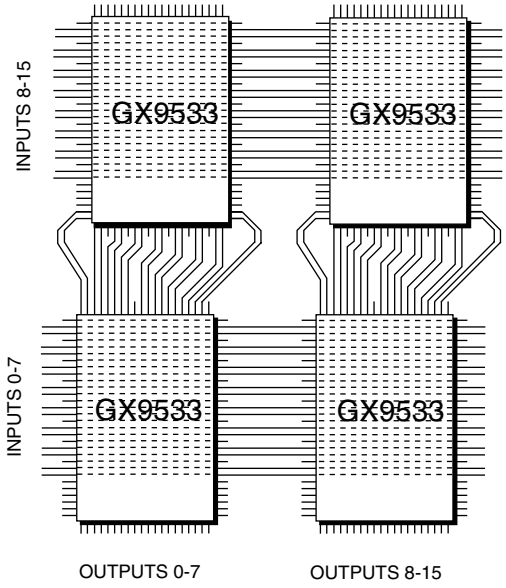



Fig. 9 Crosspoint Matrix Expansion - 16x16 Crosspoint Matrix

### BUS THROUGH™ PIN CONNECTIONS

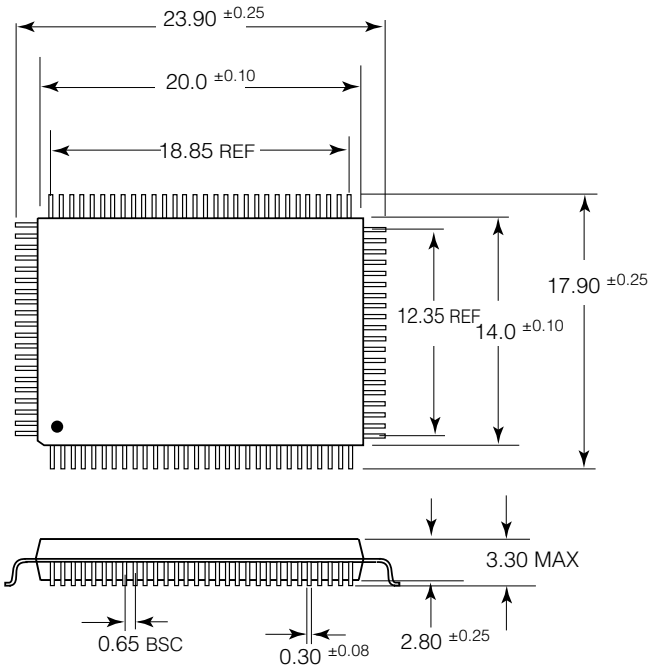
To easily facilitate a switching matrix design where inputs can be bussed across a matrix of crosspoint devices, Gennum's crosspoint device has "NC" pins opposite the input pins as shown by the dotted lines in the pin-out diagram above. This design allows bussing of inputs without having to use "vias" to get below the top layer of the printed circuit board.

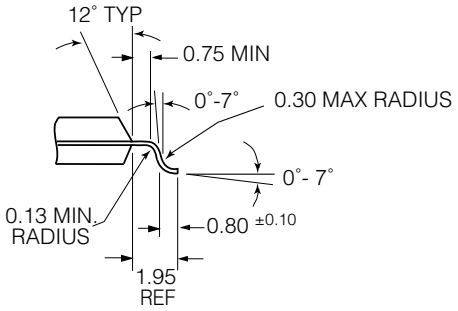
### EXPANSION PORT INPUT

The expansion inputs provide the following benefits:

- by not having to run traces from the outputs of the crosspoint switch to a common output bus, crosstalk between output channels can be greatly reduced.
- fewer circuit board layers are required because the outputs of each device simply line up
- there are no transmission line effects caused by connecting High-Z outputs to an output bus
- because the output signal is being routed from the top of the switching matrix to the bottom through the devices, inputs can be simply bussed across the board without having to worry about input/output crosstalk.

## PACKAGE DIMENSIONS




100 pin MQFP
Dimensions in millimeters

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