ICS1733
Preliminary/Confidential
Device Information

QuickSaver® Intelligent Conditioning/charge Solution for Rechargeable Lithium-Ion Batteries

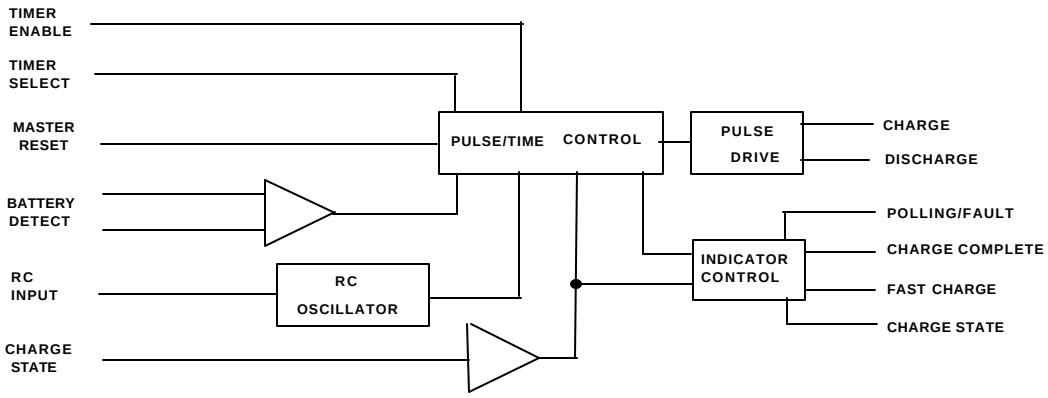
General Description

The ICS1733 is a 16 pin 5V CMOS IC that provides a pulse conditioning charge technique, charge stage indications, and with external sense circuits, provides battery status information and an option for reducing charge time on partially charged lithium-ion batteries. The ICS1733 pulse condition charge technique provides charging systems the capability to appreciably reduce the rate at which lithium-ion battery capacity declines. A reduction in the capacity fade rate aids in maintaining product run time, extending the service life of the battery, and lessens dependency on replacement and spare batteries.

Four Stage Conditioning Charge Sequence

The normal ICS1733 charging sequence consists of four stages that enables an appropriate external current/voltage regulator to pulse charge. The first stage is a soft-start conditioning charge which gradually increases the on duty cycle to the current/voltage regulator in the first several minutes after the initiation of a charge. Next a near full duty cycle conditioning charge is applied. In both stages charge CHG pin 1 simply turns on and off an external current/voltage source. The external current/voltage regulator provides the current and voltage requirements specified by battery manufacturer. The near full-on condition stage continues until the fast conditioning charge timer expires. Full Conditioning Charge indicator (FCN) pin 10 is active through out the first two stages.

Block Diagram



Four Stage Conditioning Charge Sequence (continued)

The normal ICS1733 charging sequence consists of four stages that enables an appropriate external current/voltage regulator to pulse charge. The first stage is a soft-start conditioning charge which gradually increases the on duty cycle to the current/voltage regulator in the first several minutes upon initiation of a charge. Next a near full duty cycle conditioning charge is applied. In both stages charge CHG pin 1 simply turns on and off an external current/voltage source. The external current/voltage regulator provides the current and voltage requirements specified by battery manufacturer. The near full-on condition stage continues until the ICS1733 full conditioning charge timer expires. Fast Conditioning Charge Indicator (FCN) pin 10 is active through out the first two stages.

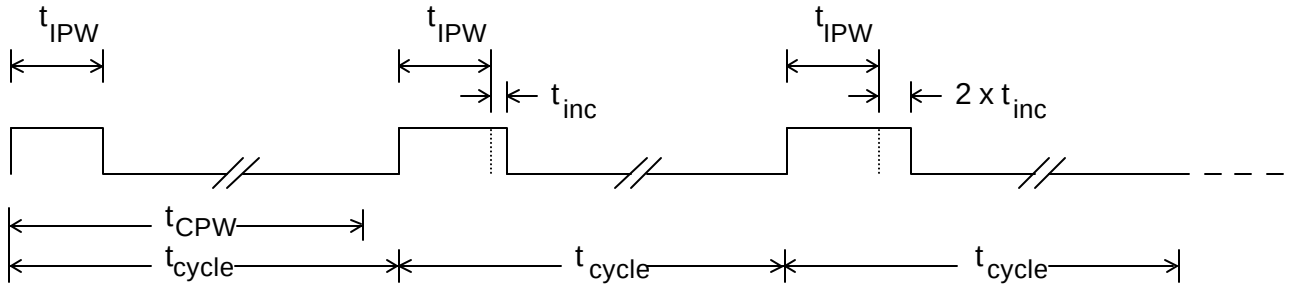
Timer select (TSEL) pin 7 works with external sense circuits to provide a reduced timer setting for batteries over 2/3rds full. Charge Status Sense (CSS) pin 12 works with external sense circuits to bypass the first two stages of the sequence, to immediately indicate that the battery is already full when charge is initiated. The immediate charge complete indication is provided by Charge Complete Indicator (CCN) pin 4. Application circuits are forthcoming as to how to use these two features.

Stage 1: Soft-Start Conditioning Charge

Over-discharged cells do not accept charge as readily as cells with a normal, minimal amount of charge. The soft-start stage gradually increases the duty cycle of the external current/voltage regulator at the beginning of charge. The pulse width increases every cycle until the duty cycle applied for the full condition charge pulse width (t_{CPW}) shown below. The soft-start pulse width increases by t_{inc} over 120 cycles that is determined by

$$t_{inc} = \frac{t_{CPW} - t_{IPW}}{120}.$$

The discharge conditioning pulse mentioned previously is not present during soft-start.



Cycle to cycle increase of the soft-start conditioning charge pulse widths.

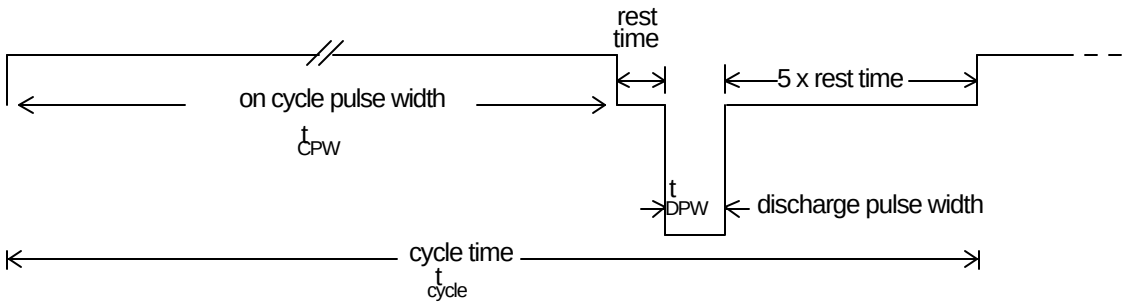
Timing Characteristics

R = 24 kΩ, C= 100 pF with typical tolerances (reduce ranges with lower tolerance R,C)

Parameter	Symbol	Range	Units
Clock Frequency		500 to 700	KHz
Master Reset Pulse Duration		1 to 1.4	Sec
Fast Reset Duration (info on later)		100 to 150	usec
Charge Pulse Width	t_{CPW}	1.3 to 1.8	Sec
Discharge Pulse Width		7.5 to 10	ms
Rest Time	Rest time	6 to 8	ms
Cycle Time	t_{cycle}	1.6 to 2.1	Sec
Soft Start Initial Pulse Width	t_{IPW}	330 to 480	ms
Soft Start Length		3 to 4.25	Min
Soft Start Incremental Pulse Width	t_{inc}	7.5 to 10	ms

Stage 2: Full Condition Charge /Discharge Pulsing

The ICS1733 provides a series of charge and discharge pulses from (CHG) pin 1 and discharge (DCHG) pin 2 respectively. The pulsed technique consists of a relatively long charge pulse, which is supplied to the external voltage/current source from (CHG) pin 1. A brief discharge pulse follows from discharge (DCHG) pin 2 that switches a discharge resistor across the battery using an external transistor.



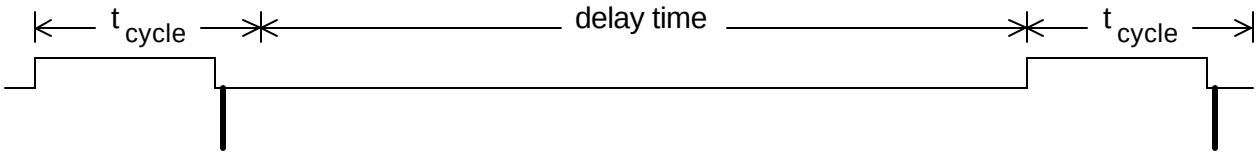
Full Conditioning Charge cycle showing charge into (on cycle) and out of the battery (discharge)

The discharge current is produced using an external transistor that switches in an external resistor across the battery. The amplitude of the discharge resistor is normally set at the ampere-hour rating of the battery. If the battery is 1.25 amp hour, the discharge current is set at 1.25A using the battery's nameplate voltage to select components.

The discharge pulse is a relatively brief, fixed ratio to the cycle time. The ratio is .00465 or .465% of the cycle time. The external transistor and discharge resistor are relatively small due to the discharge function's low duty cycle. The external transistor is selected based on its pulsed ratings while the resistor is conservatively selected based on the RMS current it carries. Since the discharge current pulse is rectangular, the RMS current is equal to the peak current times the square root of the duty cycle. The RMS current is less 7% of the peak current.

Stage 3: Conditioning Topping Charge

The topping charge provides additional opportunity to add extra charge with continued discharge pulse conditioning. The ICS1733 conditioning pulsed method accomplished this by eliminating the stress constant voltage, unidirectional current flow causes. The topping conditioning charge consists of the same pulsed technique, including the same discharge pulse conditioning as used during the full condition charge stage (stage 2), except the time between the charge/discharge pulse sequence has been significantly extended shown in diagram below. The duty cycle for the topping charge at different charge rates is given in the section titled *Timer Selection*. The charge complete indicator (CCN) is active during this stage and the maintenance stage that follows.



Timing diagram for topping and maintenance conditioning charges.

Stage 4: Conditioning Maintenance Charge

The conditioning maintenance charge stage offsets the relatively small, natural self-discharge Li-Ion batteries exhibit as well as offsets any current drain effects from the charger and sense circuits. The same pulsed technique including the discharge pulse conditioning used during the topping charge stage is used, except the delay between the charge/discharge pulses is once again expanded. The maintenance charge stage maintains the battery at full charge without the added stress constant voltage unidirectional charging causes. The charge complete indicator (CCN) is active throughout this stage.

External Voltage/Current Source Considerations

The external current/voltage regulator must provides the current and voltage amplitudes, tolerances, fault protection, etc. as required by the battery manufacturer. The external current/voltage regulator must respond reasonably well and remain stable as it is turned on and off by the ICS1733 charge enable (CHG) pin 1. Transient response can't be allowed to violate the current and voltage characteristics required by the battery manufacturer.

A logic HIGH at the CHG pin 1 is used to enable the external current/voltage regulator. A logic LOW at CHG pin 1 is used to turn off the external current/voltage regulator. Appropriate interface circuits may be required for level shifting and logic reversal depending on the current/regulator configuration.

Battery Detection

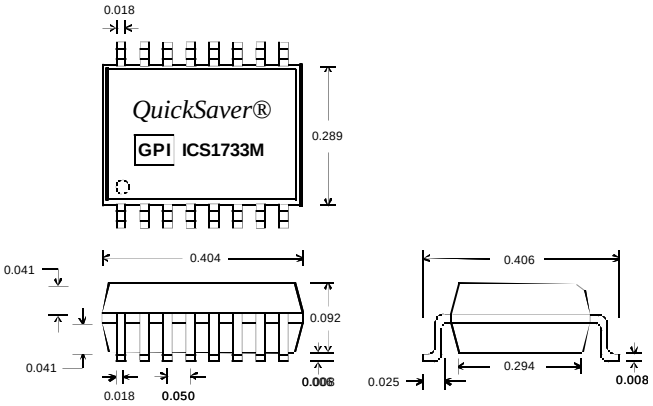
The following options can be used to detect the presence of a battery. The simplest and often times least expensive method for charger stand applications involves a small mechanical switch in the battery well. The switch contacts provide a signal to the ICS1733 indicating the battery is physically present. Master Reset (MRN) pin 9 can be used for this purpose. When the battery is removed, MRN is switched and held at ground holding the ICS1733 in reset, keeping the external current/voltage regulator off. Upon installation of the battery the MRN is released and the ICS1733 begins the pulse charge sequence mentioned previously. This approach is shown on the ICS1733 BASIC EVALUATION CIRCUIT DIAGRAM.

Pin Identification, Type and Description

Pin	ID	*Type	Description
1	CHG	OUTPUT	Active high (PFET)/Active low (NFET) TTL compatible 25 mA max. drive is used to turn on and off an external current/voltage regulator to pulse charge battery
2	DCHG	OUTPUT	Active high (PFET)/ Active low (NFET) TTL compatible 25 mA max. drive is used to turn on and off external transistor to briefly pulse discharge battery during charge
3	PFN	OUTPUT	Polling /Fault indicator. NFET drain rated at 40 mA max provides active low to turn on external indicator showing the battery is missing or there is an open circuit.
4	CCN	OUTPUT	Charge Complete indicator. NFET drain rated at 40 mA max provides active low to turn on external indicator when the battery is detected as already full at the start of charge (info later), and when in the topping and maintenance condition charge stages.
5	FCN	OUTPUT	Full Condition Charge indicator. NFET drain rated at 40 mA max provides active low to turn on external indicator indicating the device is applying soft-start or near full conditioning charge
6	CSN	OUTPUT	Charge State indicator. NFET drain rated at 40 mA max provides active low to activate a reduced timed charge, indicate approximate battery state of charge, and assist with battery detection. (information to be provided later)
7	TSEL	INPUT	Tri-state input for setting full conditioning charge stage timer. The TSEL timer input can be mechanically or electronically set. Left open circuit, TSEL floats to 2.3 V. For a logic high, a pull-up to V_{DD} is required.
8	VSS	GROUND	The return or ground of the 5V supply is connected to VSS providing ground for all logic, output driver, analog, and output indicator circuits.
9	MRN	INPUT	Master Reset input has an internal pull-up of 75 kΩ. A logic low on the MRN pin is applied to shutdown and released for restart. An internal power-up reset automatically occurs at initial power up. Debouncing for switch applications is provided internally.
10	RC	INPUT	Sets the frequency on the internal clock. Typically 24 kΩ is connected between this pin and V_{DD} and a 100 pF capacitor is connected between this pin and ground.
11	ENB	INPUT	Enables the full conditioning charge stage timer
12	CSS	INPUT	Charge State Sense. Uses external sense circuit to indicate approximate charge state
13	BDR1	INPUT	External reference input to this pin provides means to detect the presence of a battery.
14	BDR2	INPUT	External reference input to this pin provides means to detect the presence of a battery.
15	N/U	Not Unused	Connect to ground
16	VDD	INPUT	+5 VDC +/- 5% is connected to the VDD pin. The current demand is 11mA maximum A bypass capacitor to ground is required at the pins or nearby

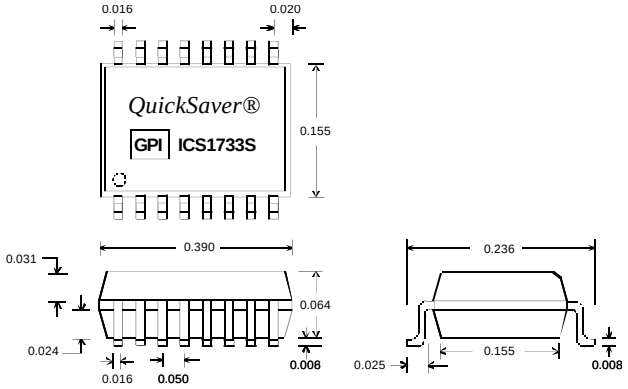
Pin Descriptions

* Input and output pins all have internal ESD protection diodes to VDD and VSS for 2KV protection per MIL STD 883 method 3015.7. Depending on the application, set-up, board layout, etc. additional ESD protection may be required



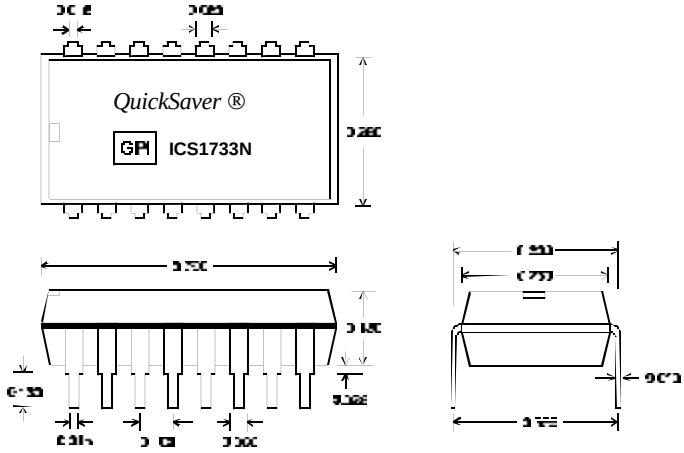
All package dimensions are in inches.

16-Pin SOIC Package (300 mil)



All package dimensions are in inches.

16-Pin SOIC Package (150 mil)



16-Pin DIP Package (300 mil)

Ordering Information:
ICS1733M, ICS1733MT,
ICS1733S, ICS1733ST, ICS1733N

Example:
ICS 1733 ST

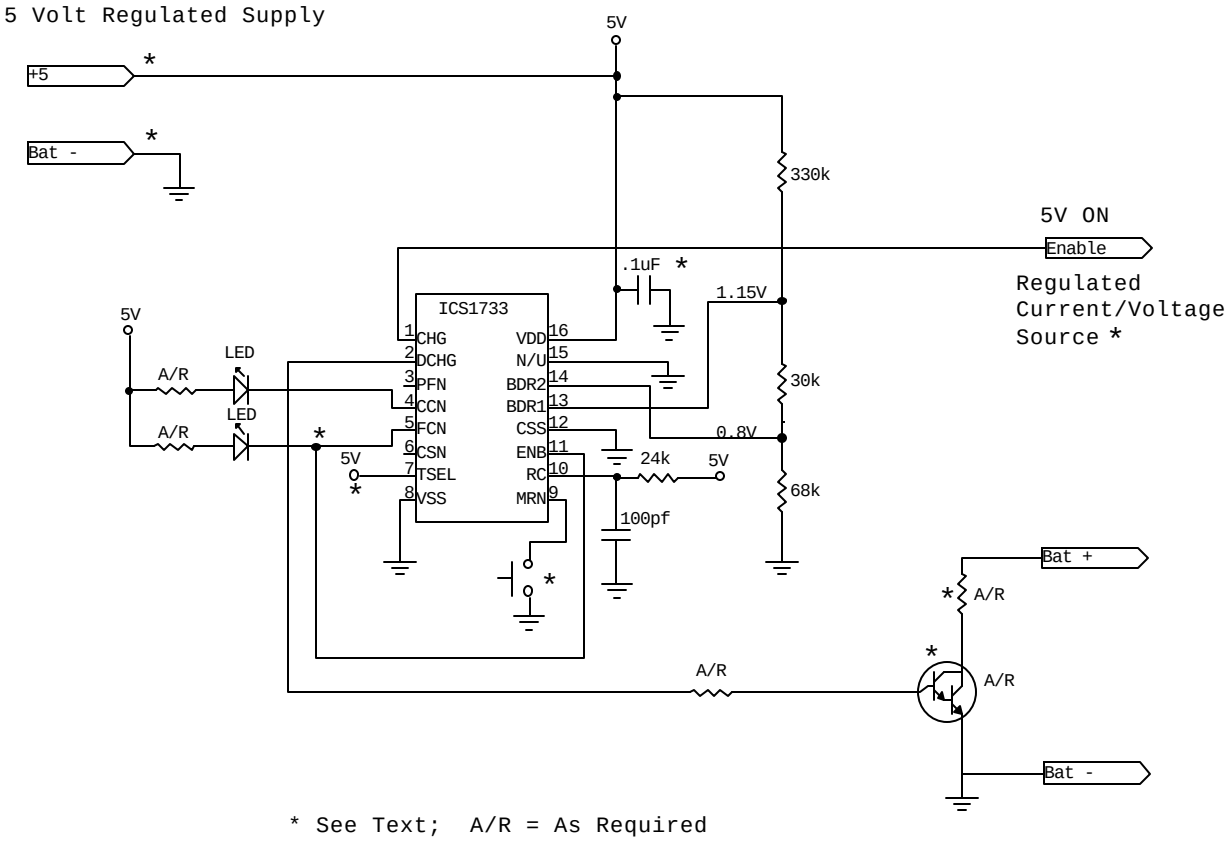
Package type: N= DIP (Plastic)
M= 300 mil SOIC
S= 150 mil SOIC
MT= 300 mil SOIC Tape and Reel
ST= 150 mil SOIC Tape and Reel

Device type: Consists of 3 to 5 digits or numbers

Prefix: ICS = Intelligent Charging Solution standard device

ICS1733 Evaluation Information

The circuit diagram below is for evaluating the benefit of reduced capacity fade the ICS1733 provides a charging system for charging Li-ion batteries. The circuit as shown will not perform any special functions such as electronic battery detection, immediate indication of an already full battery, indication that the battery is over more than 2/3rd full, etc. These functions re quire additional external sense circuits. Information will be provided at a later date. The ICS1733 in the circuit below is configured to run a full condition charge for 2 ¼ hours followed by the topping and maintenance conditioning charges previously mentioned. The 2¼ hours may be decreased approximately 20% to about 2 hours by changing the 24KΩ RC pin timing resistor to 20KΩ. Similarly, the 2 ¼ hours may be increased by 25% to about 2.75 hours by changing the 24KΩ 30KΩ.



ICS1733 BASIC EVALUATION CIRCUIT

Full Condition Charge Timer Settings, Topping and Maintenance Duty Cycles

R = 24 kΩ, C= 100 pF with typical tolerances (the range below can be reduced using lower tolerance devices for R,C)

TSEL	Full Cond. Time	Topping Charge Duty Cycle	Maintenance Charge Duty Cycle
L	*30 to 40 min	2.5%	.62%
H	110 to 145 min	9.1%	2.5%
Z	300 to 400 min	20%	5.9%

* Note: The 30 to 40 minute timer is an option for charging a battery that is more than 2/3rds full. It is not an option suggesting that an empty battery can be charged to full in this short of a time. More information to be provided later.

Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	85	°C
Storage Temperature	-55 to 150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those listed in this document is not implied. Exposure to absolute maximum rating conditions for extended periods will affect product reliability.

IMPORTANT NOTICE

Galaxy Power, Inc. (GPI) makes no claims about the capability of any battery to accept a fast charge. GPI strongly recommends that the battery manufacturer be consulted before fast charging. GPI shall be held harmless for any misapplication of this device such as: exceeding the rated specifications of the battery manufacturer; personal or product damage caused by the he charging device, circuit, or system itself; unsafe use, application, and/or manufacture of a charge system using this device.

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