

FLASH MEMORY

CMOS

32 M (4M × 8/2M × 16) BIT

MirrorFlash™*

MBM29PL32TM/BM 90/10

DESCRIPTION

The MBM29PL32TM/BM is a 32M-bit, 3.0 V-only Flash memory organized as 4M bytes by 8 bits or 2M words by 16 bits. The MBM29PL32TM/BM is offered in 48-pin TSOP(1) and 48-ball FBGA. The device is designed to be programmed in-system with the standard 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

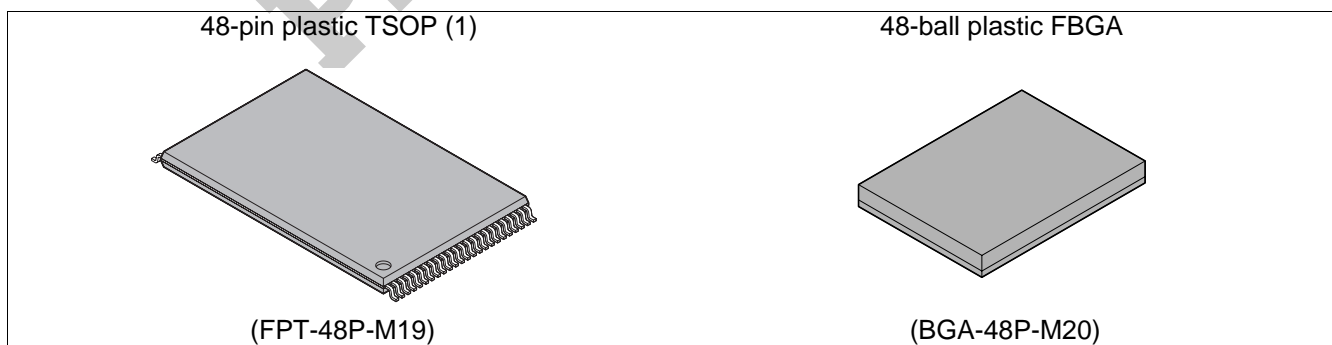
The standard MBM29PL32TM/BM offers access times of 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable (\overline{CE}), write enable (\overline{WE}), and output enable (\overline{OE}) controls.

(Continued)

PRODUCT LINE UP

| Part No. | MBM29PL32TM/BM | |
|---------------------------------|----------------|----------------|
| | 90 | 10 |
| V_{CC} | 3.0 V to 3.6 V | 3.0 V to 3.6 V |
| Max Address Access Time | 90 ns | 100 ns |
| Max \overline{CE} Access Time | 90 ns | 100 ns |
| Max Page Read Access Time | 25 ns | 30 ns |

PACKAGES



* : MirrorFlash™ is a trademark of Fujitsu Limited.

(Continued)

The MBM29PL32TM/BM supports command set compatible with JEDEC single-power-supply EEPROMS standard. Commands are written into the command register. The register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29PL32TM/BM is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm™ which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm™ which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. All sectors are erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ₇, by the Toggle Bit feature on DQ₆. Once the end of a program or erase cycle has been completed, the devices internally return to the read mode.

Fujitsu Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The devices electrically erase all bits within a sector simultaneously via hot-hole assisted erase. The words are programmed one word at a time using the EPROM programming mechanism of hot electron injection.

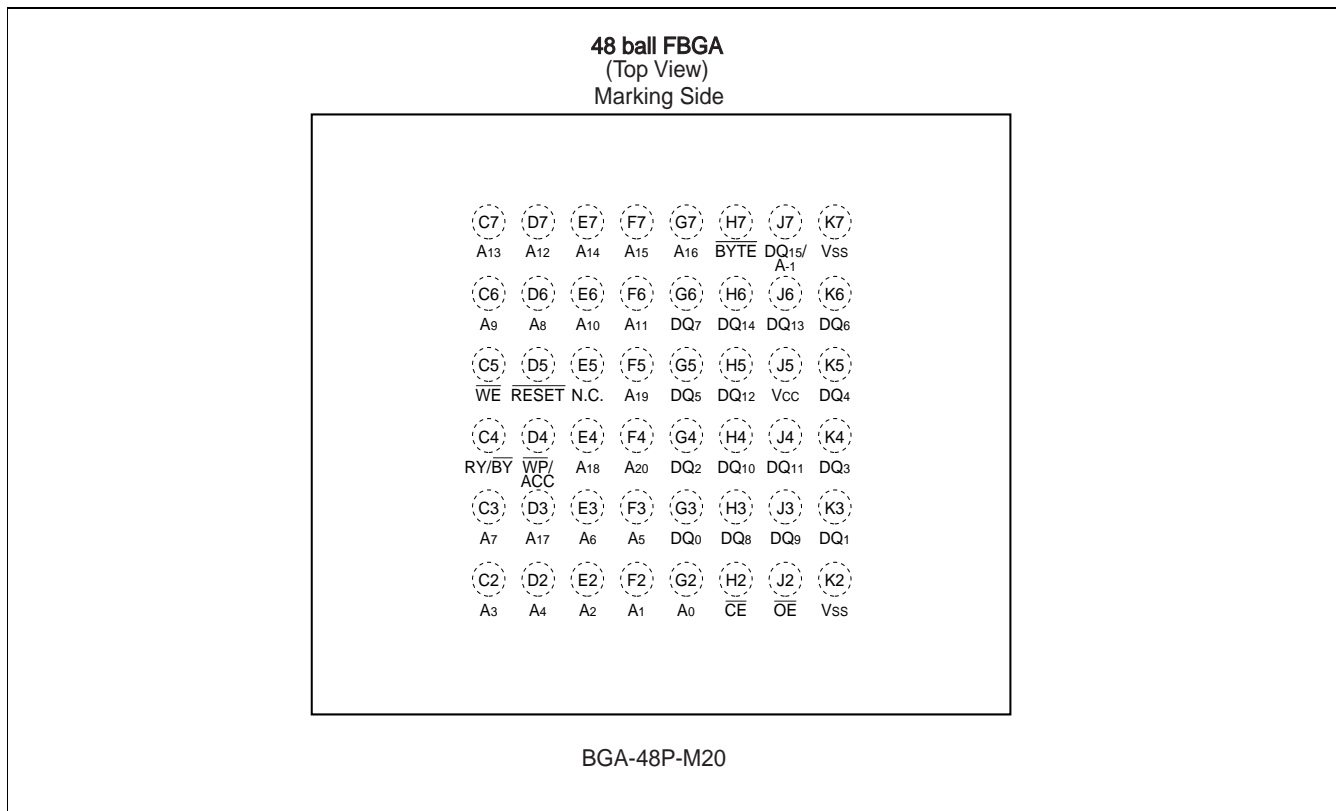
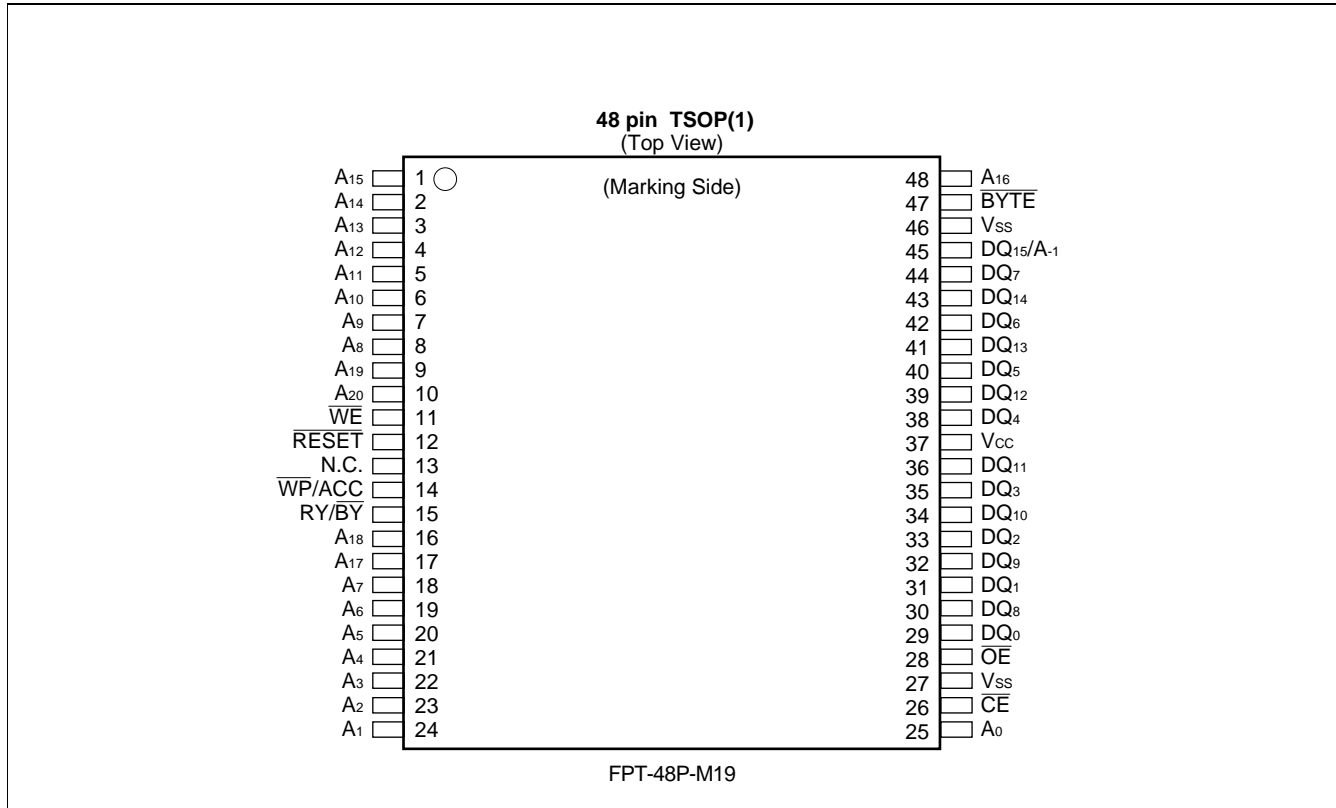
■ FEATURES

- **0.23 μm Process Technology**
- **Single 3.0 V read, program and erase**
Minimizes system level power requirements
- **Industry-standard pinouts**
48-pin TSOP (1) (Package suffix: TN - Normal Bend Type)
48-ball FBGA(Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance Page mode**
Fast 8 bytes / 4 words access capability
- **Sector erase architecture**
Eight 8K byte and sixty-three 64K byte sectors
Eight 4K word and sixty-three 32K word sectors
Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Boot Code Sector Architecture**
T = Top sector
B = Bottom sector
- **HiddenROM**
256 bytes / 128 words of HiddenROM, accessible through a "HiddenROM Entry" command sequence
Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}/\text{ACC}$ input pin**
At V_{IL} , allows protection of outermost two 8K bytes / 4K words sectors, regardless of sector protection/unprotection status
At V_{ACC} , increases program performance
- **Embedded Erase^{TM*} Algorithms**
Automatically pre-programs and erases the chip or any sector
- **Embedded Program^{TM*} Algorithms**
Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/BY)**
Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
When addresses remain stable, automatically switches themselves to low power mode
- **Program Suspend/Resume**
Suspends the program operation to allow a read in another address
- **Low V_{CC} write inhibit $\leq 2.5 \text{ V}$**
- **Erase Suspend/Resume**
Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector Group Protection**
Hardware method disables any combination of sector groups from program or erase operations
- **Sector Group Protection Set function by Extended sector protect command**
- **Fast Programming Function by Extended Command**
- **Temporary sector group unprotection**
Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin
This feature allows code changes in previously locked sectors
- **In accordance with CFI (Common Flash Memory Interface)**

* : Embedded EraseTM and Embedded ProgramTM are trademarks of Advanced Micro Devices, Inc.

MBM29PL32TM/BM_{90/10}

■ PIN ASSIGNMENTS



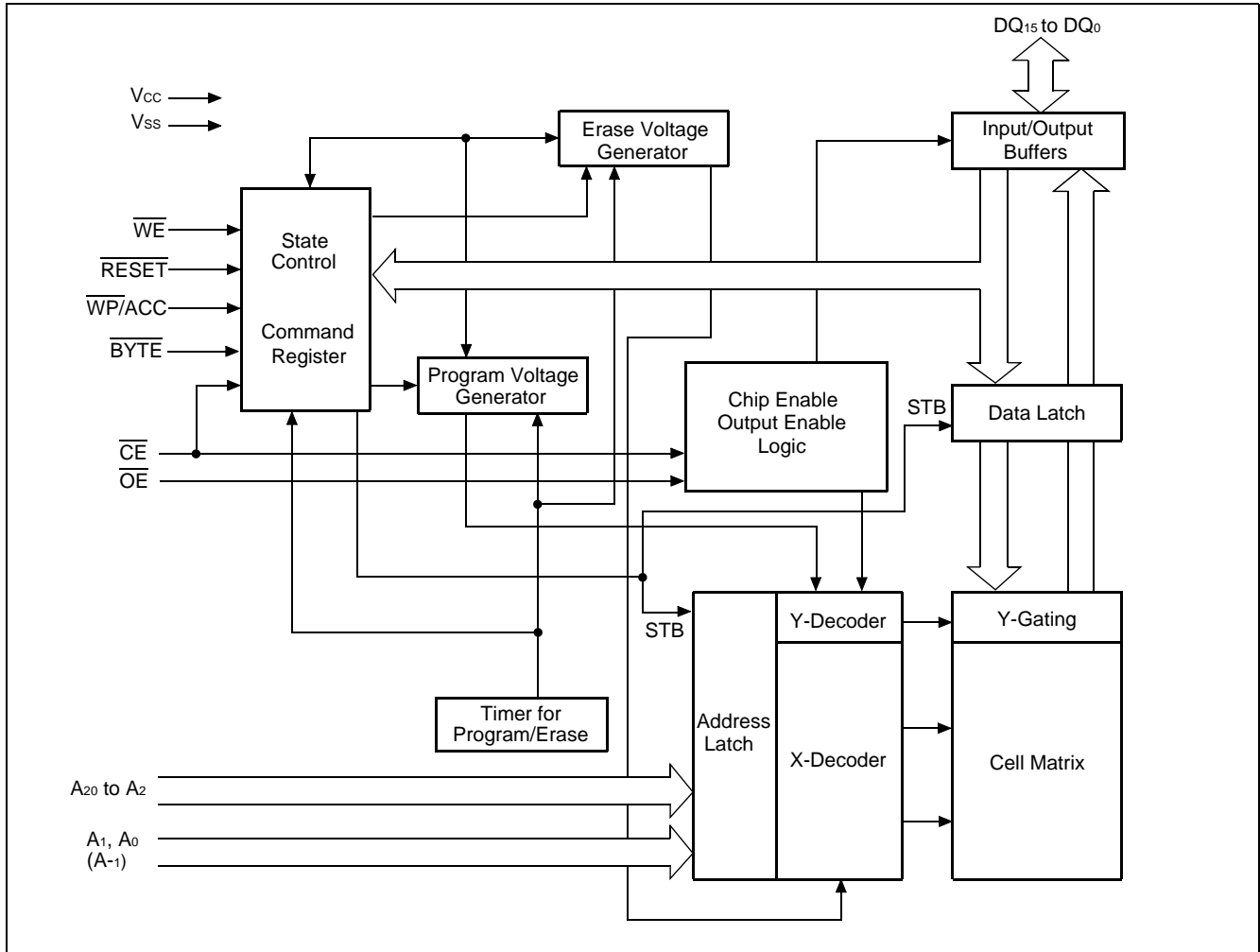
■ PIN DESCRIPTIONS

MBM29PL32TM/BM Pin Configuration

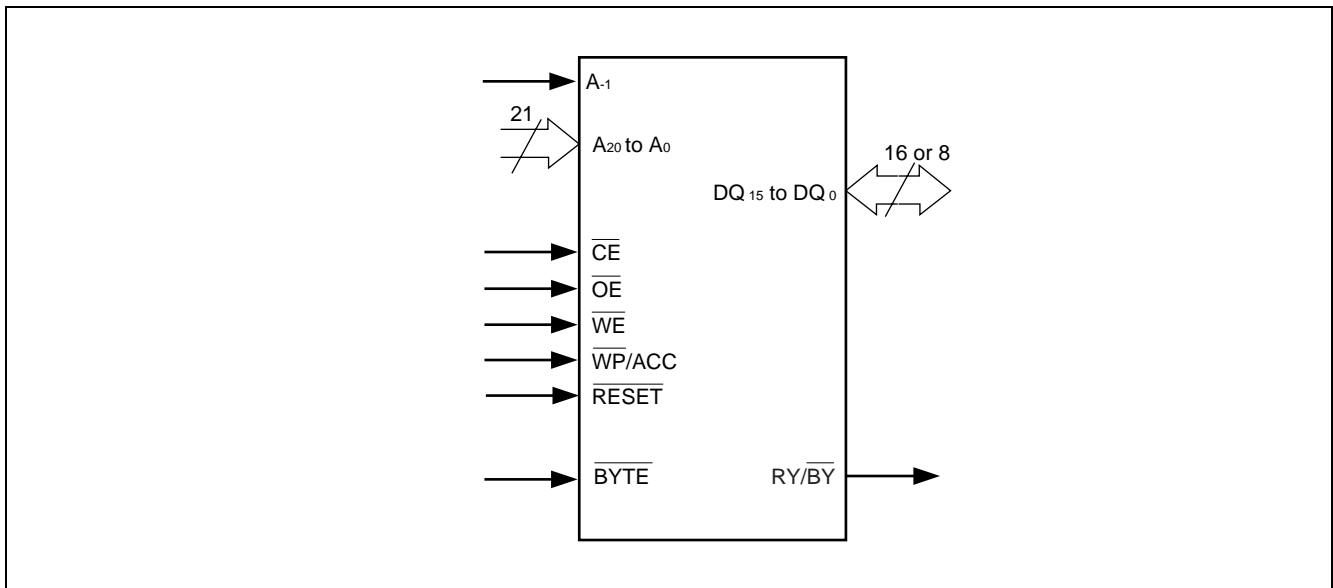
| Pin | Function |
|---|--|
| A ₂₀ to A ₀ , A ₋₁ | Address Inputs |
| DQ ₁₅ to DQ ₀ | Data Inputs/Outputs |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{WE}}$ | Write Enable |
| $\overline{\text{WP/ACC}}$ | Hardware Write Protection/Program Acceleration |
| $\overline{\text{RESET}}$ | Hardware Reset Pin/Temporary Sector Group Unprotection |
| $\overline{\text{BYTE}}$ | Select Byte or Word mode |
| RY/ $\overline{\text{BY}}$ | Ready/Busy Output |
| V _{CC} | Device Power Supply |
| V _{SS} | Device Ground |
| N.C. | No Internal Connection |

MBM29PL32TM/BM_{90/10}

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29PL32TM/BM User Bus Operations (Word Mode : $\overline{\text{BYTE}} = V_{IH}$)

| Operation | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A ₀ | A ₁ | A ₂ | A ₃ | A ₆ | A ₉ | DQ ₀ to DQ ₁₅ | $\overline{\text{RESET}}$ | $\overline{\text{WP/ACC}}$ |
|--|------------------------|------------------------|------------------------|----------------|----------------|----------------|----------------|----------------|-----------------|-------------------------------------|---------------------------|----------------------------|
| Standby | H | X | X | X | X | X | X | X | X | Hi-Z | H | X |
| Autoselect Manufacture Code* ¹ | L | L | H | L | L | L | L | L | V _{ID} | Code | H | X |
| Autoselect Device Code* ¹ | L | L | H | H | L | L | L | L | V _{ID} | Code | H | X |
| Read | L | L | H | A ₀ | A ₁ | A ₂ | A ₃ | A ₆ | A ₉ | D _{OUT} | H | X |
| Output Disable | L | H | H | X | X | X | X | X | X | Hi-Z | H | X |
| Write (Program/Erase) | L | H | L | A ₀ | A ₁ | A ₂ | A ₃ | A ₆ | A ₉ | *4 | H | *5 |
| Enable Sector Group Protection* ² | L | H | L | L | H | L | L | L | X | *4 | V _{ID} | H |
| Temporary Sector Group Unprotection | X | X | X | X | X | X | X | X | X | *4 | V _{ID} | H |
| Reset (Hardware) | X | X | X | X | X | X | X | X | X | Hi-Z | L | X |
| Sector Write Protection* ³ | X | X | X | X | X | X | X | X | X | X | H | L |

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.
Hi-Z = High-Z, V_{ID} = 11.5 to 12.5V

- *1 : Manufacturer and device codes may also be accessed via a command register write sequence. See "MBM29PL32TM/BM Standard Command Definitions".
- *2 : Refer to Sector Group Protection.
- *3 : Protects the outermost two 4K words sectors
- *4 : D_{IN} or D_{OUT} as required by command sequence, data pulling, or sector protect algorithm
- *5 : If $\overline{\text{WP/ACC}} = V_{IL}$, the outermost two sectors remain protected.
If $\overline{\text{WP/ACC}} = V_{IH}$, the outermost two sectors will be protected or unprotected as determined by the method specified in "Sector Group Protection" in page 23.

MBM29PL32TM/BM_{90/10}

MBM29PL32TM/BM User Bus Operations (Byte Mode : $\overline{\text{BYTE}} = V_{IL}$)

| Operation | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | DQ _{15/} A ₋₁ | A ₀ | A ₁ | A ₂ | A ₃ | A ₆ | A ₉ | DQ ₀ to DQ ₇ | $\overline{\text{RESET}}$ | $\overline{\text{WP/}}$ ACC |
|--|------------------------|------------------------|------------------------|--------------------------------------|----------------|----------------|----------------|----------------|----------------|-----------------|---------------------------------------|---------------------------|--------------------------------|
| Standby | H | X | X | X | X | X | X | X | X | X | Hi-Z | H | X |
| Autoselect Manufacture Code* ¹ | L | L | H | L | L | L | L | L | L | V _{ID} | Code | H | X |
| Autoselect Device Code* ¹ | L | L | H | L | H | L | L | L | L | V _{ID} | Code | H | X |
| Read | L | L | H | A ₋₁ | A ₀ | A ₁ | A ₂ | A ₃ | A ₆ | A ₉ | D _{OUT} | H | X |
| Output Disable | L | H | H | X | X | X | X | X | X | X | Hi-Z | H | X |
| Write (Program/Erase) | L | H | L | A ₋₁ | A ₀ | A ₁ | A ₂ | A ₃ | A ₆ | A ₉ | *4 | H | *5 |
| Enable Sector Group Protection* ² | L | H | L | L | L | H | L | L | L | X | *4 | V _{ID} | H |
| Temporary Sector Group Unprotection | X | X | X | X | X | X | X | X | X | X | *4 | V _{ID} | H |
| Reset (Hardware) | X | X | X | X | X | X | X | X | X | X | Hi-Z | L | X |
| Sector Write Protection* ³ | X | X | X | X | X | X | X | X | X | X | X | H | L |

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Hi-Z = High-Z, V_{ID} = 11.5 to 12.5V

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See "MBM29PL32TM/BM Standard Command Definitions".

*2 : Refer to Sector Group Protection.

*3 : Protects the outermost two 8K bytes sectors

*4 : D_{IN} or D_{OUT} as required by command sequence, data pulling, or sector protect algorithm

*5 : If $\overline{\text{WP/ACC}} = V_{IL}$, the outermost two sectors remain protected.

If $\overline{\text{WP/ACC}} = V_{IH}$, the outermost two sectors will be protected or unprotected as determined by the method specified in "Sector Group Protection" in page 23.

MBM29PL32TM/BM Standard Command Definitions*1

| Command Sequence | | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|---------------------------------------|-----------|------------------------|-----------------------|------|------------------------|--------|-----------------------|------|-----------------------------|--------|-----------------------|------|-----------------------|------|
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Reset*2 | Word/Byte | 1 | XXh | F0h | — | — | — | — | — | — | — | — | — | — |
| Reset*2 | Word | 3 | 55h | AAh | 2AAh | 55h | 55h | F0h | RA*13 | RD*13 | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |
| Autoselect (Device ID) | Word | 3 | 55h | AAh | 2AAh | 55h | 55h | 90h | 00h*13 | 04h*13 | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |
| Program | Word | 4 | 55h | AAh | 2AAh | 55h | 55h | A0h | PA | PD | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |
| Chip Erase | Word | 6 | 55h | AAh | 2AAh | 55h | 55h | 80h | 55h | AAh | 2AAh | 55h | 55h | 10h |
| | Byte | | AAh | | 55h | | AAh | | 55h | | AAh | | | |
| Sector Erase | Word | 6 | 55h | AAh | 2AAh | 55h | 55h | 80h | 55h | AAh | 2AAh | 55h | SA | 30h |
| | Byte | | AAh | | 55h | | AAh | | 55h | | | | | |
| Program/Erase Suspend*3 | | 1 | XXh | B0h | — | — | — | — | — | — | — | — | — | — |
| Program/Erase Resume*3 | | 1 | XXh | 30h | — | — | — | — | — | — | — | — | — | — |
| Set to Fast Mode*4 | Word | 3 | 55h | AAh | 2AAh | 55h | 55h | 20h | — | — | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |
| Fast Program*4 | Word/Byte | 2 | XXh | A0h | PA | PD | — | — | — | — | — | — | — | — |
| Reset from Fast Mode*5 | Word/Byte | 2 | XXh | 90h | XXh | 00h*12 | — | — | — | — | — | — | — | — |
| Write to Buffer | Word | 20 | 55h | AAh | 2AAh | 55h | SA | 25h | SA | 0Fh | PA | PD | WBL | PD |
| | Byte | | AAh | | 55h | | SA | | 0Fh | | PA | | PD | |
| Program Buffer to Flash (Confirm) | | 1 | SA | 29h | — | — | — | — | — | — | — | — | — | — |
| Write to Buffer Abort Rese*6 | Word | 3 | 55h | AAh | 2AAh | 55h | XXh | F0h | — | — | — | — | — | — |
| | Byte | | AAh | | 55h | | XXh | | | | | | | |
| Extended Sector Group Protection*7,*8 | Word | 4 | XXh | 60h | SGA | 60h | SGA | 40h | SGA*13 | SD*13 | — | — | — | — |
| | Byte | | XXh | | 60h | | SGA | | 40h | | | | | |
| Query*9 | Word | 1 | 55h | 98h | — | — | — | — | — | — | — | — | — | — |
| | Byte | | AAh | | 98h | | — | | — | | — | | — | |
| HiddenROM Entry*10 | Word | 3 | 55h | AAh | 2AAh | 55h | 55h | 88h | — | — | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |
| HiddenROM Program*10,*11 | Word | 4 | 55h | AAh | 2AAh | 55h | 55h | A0h | PA | PD | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |
| HiddenROM Exit*11 | Word | 4 | 55h | AAh | 2AAh | 55h | 55h | 90h | XXh | 00h | — | — | — | — |
| | Byte | | AAh | | 55h | | AAh | | | | | | | |

Sector Group Protection Verify Autoselect Codes

| Type | | A ₂₀ to A ₁₂ | A ₆ | A ₃ | A ₂ | A ₁ | A ₀ | A ₋₁ *1 | Code (HEX) | |
|---------------------------|-------------|------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|-----------------|-------|
| Manufacturer's Code | | X | V _{IL} | V _{IL} | V _{IL} | V _{IL} | V _{IL} | V _{IL} | 04h | |
| Device Code | Word | X | V _{IL} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | X | 227Eh | |
| | Byte | X | V _{IL} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 7Eh | |
| Extended Device Code*2 | MBM29PL32TM | Word | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IL} | X | 221Ah |
| | | Byte | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IL} | V _{IL} | 1Ah |
| | | Word | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IH} | X | 2201h |
| | | Byte | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IH} | V _{IL} | 01h |
| | MBM29PL32BM | Word | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IL} | X | 221Ah |
| | | Byte | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IL} | V _{IL} | 1Ah |
| | | Word | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IH} | X | 2200h |
| | | Byte | X | V _{IL} | V _{IH} | V _{IH} | V _{IH} | V _{IH} | V _{IL} | 00h |
| Sector Group Protection*4 | | Sector Group Addresses | V _{IL} | V _{IL} | V _{IL} | V _{IH} | V _{IL} | V _{IL} | *3 | |

*1 : A₋₁ is for Byte mode.

*2 : At Word mode, a read cycle at address 01h (at Byte mode, 02h) outputs device code. When 227Eh (at Byte mode, 7Eh) is output, it indicates that reading two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of 0Eh (at Byte mode, 1Ch), as well as at 0Fh (at Byte mode, 1Eh).

*3 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*4 : Toggle \overline{CE} , provided SGA = fix and \overline{WE} = fix.
The data in the first cycle is invalid. The data in the second one is valid.

Sector Address Table (MBM29PL32TM)

| Sector | Sector Address | | | | | | | | | Sector Size (Kbytes/ Kwords) | (x8) Address Range | (x16) Address Range |
|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------------------|-----------------------|------------------------|
| | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | | |
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 000000h to 00FFFFh | 000000h to 007FFFh |
| SA1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 010000h to 01FFFFh | 008000h to 00FFFFh |
| SA2 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000h to 02FFFFh | 010000h to 017FFFh |
| SA3 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000h to 03FFFFh | 018000h to 01FFFFh |
| SA4 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000h to 04FFFFh | 020000h to 027FFFh |
| SA5 | 0 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000h to 05FFFFh | 028000h to 02FFFFh |
| SA6 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000h to 06FFFFh | 030000h to 037FFFh |
| SA7 | 0 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000h to 07FFFFh | 038000h to 03FFFFh |
| SA8 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000h to 08FFFFh | 040000h to 047FFFh |
| SA9 | 0 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000h to 09FFFFh | 048000h to 04FFFFh |
| SA10 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| SA11 | 0 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| SA12 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| SA13 | 0 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| SA14 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| SA15 | 0 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000h to 0FFFFFh | 078000h to 07FFFFh |
| SA16 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000h to 10FFFFh | 080000h to 087FFFh |
| SA17 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000h to 11FFFFh | 088000h to 08FFFFh |
| SA18 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000h to 12FFFFh | 090000h to 097FFFh |
| SA19 | 0 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000h to 13FFFFh | 098000h to 09FFFFh |
| SA20 | 0 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000h to 14FFFFh | 0A0000h to 0A7FFFh |
| SA21 | 0 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000h to 15FFFFh | 0A8000h to 0AFFFFh |
| SA22 | 0 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000h to 16FFFFh | 0B0000h to 0B7FFFh |
| SA23 | 0 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000h to 17FFFFh | 0B8000h to 0BFFFFh |
| SA24 | 0 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000h to 18FFFFh | 0C0000h to 0C7FFFh |
| SA25 | 0 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000h to 19FFFFh | 0C8000h to 0CFFFFh |
| SA26 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh |
| SA27 | 0 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh |
| SA28 | 0 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh |
| SA29 | 0 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh |
| SA30 | 0 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh |
| SA31 | 0 | 1 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 1F0000h to 1FFFFFh | 0F8000h to 0FFFFFh |

(Continued)

MBM29PL32TM/BM_{90/10}

| Sector | Sector Address | | | | | | | | | Sector Size (Kbytes/ Kwords) | (×8) Address Range | (×16) Address Range |
|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------------------|-----------------------|------------------------|
| | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | | |
| SA32 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 200000h to 20FFFFh | 100000h to 107FFFh |
| SA33 | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 210000h to 21FFFFh | 108000h to 10FFFFh |
| SA34 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 220000h to 22FFFFh | 110000h to 117FFFh |
| SA35 | 1 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 230000h to 23FFFFh | 118000h to 11FFFFh |
| SA36 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 240000h to 24FFFFh | 120000h to 127FFFh |
| SA37 | 1 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 250000h to 25FFFFh | 128000h to 12FFFFh |
| SA38 | 1 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 260000h to 26FFFFh | 130000h to 137FFFh |
| SA39 | 1 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 270000h to 27FFFFh | 138000h to 13FFFFh |
| SA40 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 280000h to 28FFFFh | 140000h to 147FFFh |
| SA41 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 290000h to 29FFFFh | 148000h to 14FFFFh |
| SA42 | 1 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 2A0000h to 2AFFFFh | 150000h to 157FFFh |
| SA43 | 1 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 2B0000h to 2BFFFFh | 158000h to 15FFFFh |
| SA44 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 2C0000h to 2CFFFFh | 160000h to 167FFFh |
| SA45 | 1 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 2D0000h to 2DFFFFh | 168000h to 16FFFFh |
| SA46 | 1 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 2E0000h to 2EFFFFh | 170000h to 177FFFh |
| SA47 | 1 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 2F0000h to 2FFFFFh | 178000h to 17FFFFh |
| SA48 | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 300000h to 30FFFFh | 180000h to 187FFFh |
| SA49 | 1 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 310000h to 31FFFFh | 188000h to 18FFFFh |
| SA50 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 320000h to 32FFFFh | 190000h to 197FFFh |
| SA51 | 1 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 330000h to 33FFFFh | 198000h to 19FFFFh |
| SA52 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 340000h to 34FFFFh | 1A0000h to 1A7FFFh |
| SA53 | 1 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 350000h to 35FFFFh | 1A8000h to 1AFFFFh |
| SA54 | 1 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 360000h to 36FFFFh | 1B0000h to 1B7FFFh |
| SA55 | 1 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 370000h to 37FFFFh | 1B8000h to 1BFFFFh |
| SA56 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 380000h to 38FFFFh | 1C0000h to 1C7FFFh |
| SA57 | 1 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 390000h to 39FFFFh | 1C8000h to 1CFFFFh |
| SA58 | 1 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 3A0000h to 3AFFFFh | 1D0000h to 1D7FFFh |
| SA59 | 1 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 3B0000h to 3BFFFFh | 1D8000h to 1DFFFFh |
| SA60 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 3C0000h to 3CFFFFh | 1E0000h to 1E7FFFh |
| SA61 | 1 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 3D0000h to 3DFFFFh | 1E8000h to 1EFFFFh |
| SA62 | 1 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 3E0000h to 3EFFFFh | 1F0000h to 1F7FFFh |
| SA63 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 8/4 | 3F0000h to 3F1FFFh | 1F8000h to 1F8FFFh |
| SA64 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 8/4 | 3F2000h to 3F3FFFh | 1F9000h to 1F9FFFh |

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MBM29PL32TM/BM_{90/10}

(Continued)

| Sector | Sector Address | | | | | | | | | Sector Size (Kbytes/ Kwords) | (×8) Address Range | (×16) Address Range |
|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------------------|-----------------------|------------------------|
| | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | | |
| SA65 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 8/4 | 3F4000h to 3F5FFFh | 1FA000h to 1FAFFFh |
| SA66 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 8/4 | 3F6000h to 3F7FFFh | 1FB000h to 1FBFFFh |
| SA67 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 8/4 | 3F8000h to 3F9FFFh | 1FC000h to 1FCFFFh |
| SA68 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 8/4 | 3FA000h to 3FBFFFh | 1FD000h to 1FDFFFh |
| SA69 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8/4 | 3FC000h to 3FDFFFh | 1FE000h to 1FEFFFh |
| SA70 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8/4 | 3FE000h to 3FFFFFh | 1FF000h to 1FFFFFh |

Note : The address range is A₂₀ : A₋₁ if in Byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$) .
 The address range is A₂₀ : A₀ if in Word mode ($\text{BYTE} = V_{\text{IH}}$) .

Sector Address Table (MBM29PL32BM)

| Sector | Sector Address | | | | | | | | | Sector Size (Kbytes/ Kwords) | (×8) Address Range | (×16) Address Range |
|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------------------|-----------------------|------------------------|
| | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | | |
| SA70 | 1 | 1 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 3F0000h to 3FFFFFFh | 1F8000h to 1FFFFFFh |
| SA69 | 1 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 3E0000h to 3FFFFFFh | 1F0000h to 1F7FFFh |
| SA68 | 1 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 3D0000h to 3DFFFFh | 1E8000h to 1EFFFFh |
| SA67 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 3C0000h to 3CFFFFh | 1E0000h to 1E7FFFh |
| SA66 | 1 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 3B0000h to 3BFFFFh | 1D8000h to 1DFFFFh |
| SA65 | 1 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 3A0000h to 3AFFFFh | 1D0000h to 1D7FFFh |
| SA64 | 1 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 390000h to 39FFFFh | 1C8000h to 1CFFFFh |
| SA63 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 380000h to 38FFFFh | 1C0000h to 1C7FFFh |
| SA62 | 1 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 370000h to 37FFFFh | 1B8000h to 1BFFFFh |
| SA61 | 1 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 360000h to 36FFFFh | 1B0000h to 1B7FFFh |
| SA60 | 1 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 350000h to 35FFFFh | 1A8000h to 1AFFFFh |
| SA59 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 340000h to 34FFFFh | 1A0000h to 1A7FFFh |
| SA58 | 1 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 330000h to 33FFFFh | 198000h to 19FFFFh |
| SA57 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 320000h to 32FFFFh | 190000h to 197FFFh |
| SA56 | 1 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 310000h to 31FFFFh | 188000h to 18FFFFh |
| SA55 | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 300000h to 30FFFFh | 180000h to 187FFFh |
| SA54 | 1 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 2F0000h to 2FFFFFFh | 178000h to 17FFFFh |
| SA53 | 1 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 2E0000h to 2EFFFFh | 170000h to 177FFFh |
| SA52 | 1 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 2D0000h to 2DFFFFh | 168000h to 16FFFFh |
| SA51 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 2C0000h to 2CFFFFh | 160000h to 167FFFh |
| SA50 | 1 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 2B0000h to 2BFFFFh | 158000h to 15FFFFh |
| SA49 | 1 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 2A0000h to 2AFFFFh | 150000h to 157FFFh |
| SA48 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 290000h to 29FFFFh | 148000h to 14FFFFh |
| SA47 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 280000h to 28FFFFh | 140000h to 147FFFh |
| SA46 | 1 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 270000h to 27FFFFh | 138000h to 13FFFFh |
| SA45 | 1 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 260000h to 26FFFFh | 130000h to 137FFFh |
| SA44 | 1 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 250000h to 25FFFFh | 128000h to 12FFFFh |
| SA43 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 240000h to 24FFFFh | 120000h to 127FFFh |
| SA42 | 1 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 230000h to 23FFFFh | 118000h to 11FFFFh |
| SA41 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 220000h to 22FFFFh | 110000h to 117FFFh |
| SA40 | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 210000h to 21FFFFh | 108000h to 10FFFFh |
| SA39 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 200000h to 20FFFFh | 100000h to 107FFFh |
| SA38 | 0 | 1 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 1F0000h to 1FFFFFFh | 0F8000h to 0FFFFFFh |

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| Sector | Sector Address | | | | | | | | | Sector Size (Kbytes/ Kwords) | Address Range (×8) | Address Range (×16) |
|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------------------|-----------------------|------------------------|
| | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | | |
| SA37 | 0 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh |
| SA36 | 0 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh |
| SA35 | 0 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh |
| SA34 | 0 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh |
| SA33 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh |
| SA32 | 0 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000h to 19FFFFh | 0C8000h to 0CFFFFh |
| SA31 | 0 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000h to 18FFFFh | 0C0000h to 0C7FFFh |
| SA30 | 0 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000h to 17FFFFh | 0B8000h to 0BFFFFh |
| SA29 | 0 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000h to 16FFFFh | 0B0000h to 0B7FFFh |
| SA28 | 0 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000h to 15FFFFh | 0A8000h to 0AFFFFh |
| SA27 | 0 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000h to 14FFFFh | 0A0000h to 0A7FFFh |
| SA26 | 0 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000h to 13FFFFh | 098000h to 09FFFFh |
| SA25 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000h to 12FFFFh | 090000h to 097FFFh |
| SA24 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000h to 11FFFFh | 088000h to 08FFFFh |
| SA23 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000h to 10FFFFh | 080000h to 087FFFh |
| SA22 | 0 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000h to 0FFFFFh | 078000h to 07FFFFh |
| SA21 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| SA20 | 0 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| SA19 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| SA18 | 0 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| SA17 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| SA16 | 0 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000h to 09FFFFh | 048000h to 04FFFFh |
| SA15 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000h to 08FFFFh | 040000h to 047FFFh |
| SA14 | 0 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000h to 07FFFFh | 038000h to 03FFFFh |
| SA13 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000h to 06FFFFh | 030000h to 037FFFh |
| SA12 | 0 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000h to 05FFFFh | 028000h to 02FFFFh |
| SA11 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000h to 04FFFFh | 020000h to 027FFFh |
| SA10 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000h to 03FFFFh | 018000h to 01FFFFh |
| SA9 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000h to 02FFFFh | 010000h to 017FFFh |
| SA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 010000h to 01FFFFh | 008000h to 00FFFFh |
| SA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 8/4 | 00E000h to 00FFFFh | 007000h to 007FFFh |
| SA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 8/4 | 00C000h to 00DFFFh | 006000h to 006FFFh |
| SA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 8/4 | 00A000h to 00BFFFh | 005000h to 005FFFh |

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| Sector | Sector Address | | | | | | | | | Sector Size (Kbytes/ Kwords) | (×8) Address Range | (×16) Address Range |
|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------------------|-----------------------|------------------------|
| | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | | |
| SA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8/4 | 008000h to 009FFFh | 004000h to 004FFFh |
| SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 8/4 | 006000h to 007FFFh | 003000h to 003FFFh |
| SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 8/4 | 004000h to 005FFFh | 002000h to 002FFFh |
| SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 8/4 | 002000h to 003FFFh | 001000h to 001FFFh |
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8/4 | 000000h to 001FFFh | 000000h to 000FFFh |

Note : The address range is A₂₀ : A₋₁ if in Byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$) .
 The address range is A₂₀ : A₀ if in Word mode ($\overline{\text{BYTE}} = V_{\text{IH}}$) .

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Sector Group Address Table (MBM29PL32TM)

| Sector Group | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Sectors |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| SGA0 | 0 | 0 | 0 | 0 | X | X | X | X | X | SA0 to SA3 |
| SGA1 | 0 | 0 | 0 | 1 | X | X | X | X | X | SA4 to SA7 |
| SGA2 | 0 | 0 | 1 | 0 | X | X | X | X | X | SA8 to SA11 |
| SGA3 | 0 | 0 | 1 | 1 | X | X | X | X | X | SA12 to SA15 |
| SGA4 | 0 | 1 | 0 | 0 | X | X | X | X | X | SA16 to SA19 |
| SGA5 | 0 | 1 | 0 | 1 | X | X | X | X | X | SA20 to SA23 |
| SGA6 | 0 | 1 | 1 | 0 | X | X | X | X | X | SA24 to SA27 |
| SGA7 | 0 | 1 | 1 | 1 | X | X | X | X | X | SA28 to SA31 |
| SGA8 | 1 | 0 | 0 | 0 | X | X | X | X | X | SA32 to SA35 |
| SGA9 | 1 | 0 | 0 | 1 | X | X | X | X | X | SA36 to SA39 |
| SGA10 | 1 | 0 | 1 | 0 | X | X | X | X | X | SA40 to SA43 |
| SGA11 | 1 | 0 | 1 | 1 | X | X | X | X | X | SA44 to SA47 |
| SGA12 | 1 | 1 | 0 | 0 | X | X | X | X | X | SA48 to SA51 |
| SGA13 | 1 | 1 | 0 | 1 | X | X | X | X | X | SA52 to SA55 |
| SGA14 | 1 | 1 | 1 | 0 | X | X | X | X | X | SA56 to SA59 |
| SGA15 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | SA60 to SA62 |
| | | | | | 0 | 1 | | | | |
| | | | | | 1 | 0 | | | | |
| SGA16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | SA63 |
| SGA17 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | SA64 |
| SGA18 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | SA65 |
| SGA19 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | SA66 |
| SGA20 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | SA67 |
| SGA21 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | SA68 |
| SGA22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | SA69 |
| SGA23 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SA70 |

Sector Group Address Table (MBM29PL32BM)

| Sector Group | A ₂₀ | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Sectors |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| SGA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SA0 |
| SGA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SA1 |
| SGA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SA2 |
| SGA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | SA3 |
| SGA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SA4 |
| SGA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SA5 |
| SGA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | SA6 |
| SGA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | SA7 |
| SGA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | SA8 to SA10 |
| | | | | | 1 | 0 | | | | |
| | | | | | 1 | 1 | | | | |
| SGA9 | 0 | 0 | 0 | 1 | X | X | X | X | X | SA11 to SA14 |
| SGA10 | 0 | 0 | 1 | 0 | X | X | X | X | X | SA15 to SA18 |
| SGA11 | 0 | 0 | 1 | 1 | X | X | X | X | X | SA19 to SA22 |
| SGA12 | 0 | 1 | 0 | 0 | X | X | X | X | X | SA23 to SA26 |
| SGA13 | 0 | 1 | 0 | 1 | X | X | X | X | X | SA27 to SA30 |
| SGA14 | 0 | 1 | 1 | 0 | X | X | X | X | X | SA31 to SA34 |
| SGA15 | 0 | 1 | 1 | 1 | X | X | X | X | X | SA35 to SA38 |
| SGA16 | 1 | 0 | 0 | 0 | X | X | X | X | X | SA39 to SA42 |
| SGA17 | 1 | 0 | 0 | 1 | X | X | X | X | X | SA43 to SA46 |
| SGA18 | 1 | 0 | 1 | 0 | X | X | X | X | X | SA47 to SA50 |
| SGA19 | 1 | 0 | 1 | 1 | X | X | X | X | X | SA51 to SA54 |
| SGA20 | 1 | 1 | 0 | 0 | X | X | X | X | X | SA55 to SA58 |
| SGA21 | 1 | 1 | 0 | 1 | X | X | X | X | X | SA59 to SA62 |
| SGA22 | 1 | 1 | 1 | 0 | X | X | X | X | X | SA63 to SA66 |
| SGA23 | 1 | 1 | 1 | 1 | X | X | X | X | X | SA67 to SA70 |

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Common Flash Memory Interface Code

| A ₀ to A ₆ | DQ ₀ to DQ ₁₅ | Description |
|----------------------------------|-------------------------------------|--|
| 10h 11h 12h | 0051h 0052h 0059h | Query-unique ASCII string "QRY" |
| 13h 14h | 0002h 0000h | Primary OEM Command Set (02h = Fujitsu standard) |
| 15h 16h | 0040h 0000h | Address for Primary Extended Table |
| 17h 18h | 0000h 0000h | Alternate OEM Command Set (00h = not applicable) |
| 19h 1Ah | 0000h 0000h | Address for Alternate OEM Extended Table (00h = not applicable) |
| 1Bh | 0027h | V _{CC} Min (write/erase) DQ ₇ -DQ ₄ : 1V/bit, DQ ₃ -DQ ₀ : 100 mV/bit |
| 1Ch | 0036h | V _{CC} Max (write/erase) DQ ₇ -DQ ₄ : 1V/bit, DQ ₃ -DQ ₀ : 100 mV/bit |
| 1Dh | 0000h | V _{PP} Min voltage (00h = no V _{pp} pin) |
| 1Eh | 0000h | V _{PP} Max voltage (00h =no V _{pp} pin) |
| 1Fh | 0007h | Typical timeout per single write 2 ^N μs |
| 20h | 0007h | Typical timeout for Min size buffer write 2 ^N μs |
| 21h | 000Ah | Typical timeout per individual sector erase 2 ^N ms |
| 22h | 0000h | Typical timeout for full chip erase 2 ^N ms |
| 23h | 0001h | Max timeout for write 2 ^N times typical |
| 24h | 0005h | Max timeout for buffer write 2 ^N times typical |
| 25h | 0004h | Max timeout per individual sector erase 2 ^N times typical |
| 26h | 0000h | Max timeout for full chip erase 2 ^N times typical |
| 27h | 0016h | Device Size = 2 ^N byte |
| 28h 29h | 0002h 0000h | Flash Device Interface description |
| 2Ah 2Bh | 0005h 0000h | Max number of byte in multi-byte write = 2 ^N |
| 2Ch | 0002h | Number of Erase Block Regions within device (01h = uniform) |
| 2Dh 2Eh 2Fh 30h | 0007h 0000h 0020h 0000h | Erase Block Region 1 Information |
| 31h 32h 33h 34h | 003Eh 0000h 0000h 0001h | Erase Block Region 2 Information |

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| A ₀ to A ₆ | DQ ₀ to DQ ₁₅ | Description |
|----------------------------------|-------------------------------------|--|
| 35h 36h 37h 38h | 0000h 0000h 0000h 0000h | Erase Block Region 3 Information |
| 39h 3Ah 3Bh 3Ch | 0000h 0000h 0000h 0000h | Erase Block Region 4 Information |
| 40h 41h 42h | 0050h 0052h 0049h | Query-unique ASCII string "PRI" |
| 43h | 0031h | Major version number, ASCII |
| 44h | 0033h | Minor version number, ASCII |
| 45h | 0008h | Address Sensitive Unlock Required |
| 46h | 0002h | Erase Suspend (02h = To Read & Write) |
| 47h | 0004h | Number of sectors in per group |
| 48h | 0001h | Sector Temporary Unprotection (01h = Supported) |
| 49h | 0004h | Sector Protection Algorithm |
| 4Ah | 0000h | Dual Operation (00h = Not Supported) |
| 4Bh | 0000h | Burst Mode Type (00h = Not Supported) |
| 4Ch | 0001h | Page Mode Type (01h = 4-Word Page Supported) |
| 4Dh | 00B5h | V _{ACC} (Acceleration) Supply Minimum DQ ₇ -DQ ₄ : 1V/bit, DQ ₃ -DQ ₀ : 100mV/bit |
| 4Eh | 00C5h | V _{ACC} (Acceleration) Supply Maximum DQ ₇ -DQ ₄ : 1V/bit, DQ ₃ -DQ ₀ : 100mV/bit |
| 4Fh | 00XXh | Write Protect (02h = MBM29PL32BM 03h = MBM29PL32TM 04h = Uniform sectors bottom Write Protect) |
| 50h | 01h | Program Suspend (01h = Supported) |

■ FUNCTIONAL DESCRIPTION

Standby Mode

There are two ways to implement the standby mode on the device, one using both the \overline{CE} and \overline{RESET} pins, and the other via the \overline{RESET} pin only.

When using both pins, CMOS standby mode is achieved with \overline{CE} and \overline{RESET} input held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μ A Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even when $\overline{CE} = "H"$. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the \overline{RESET} pin only, CMOS standby mode is achieved with \overline{RESET} input held at $V_{SS} \pm 0.3$ V ($\overline{CE} = "H"$ or $"L"$). Under this condition the current consumed is less than 5 μ A Max. Once the \overline{RESET} pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state, regardless of \overline{OE} input.

Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of device data. It can be useful in applications such as handy terminal, which requires low power consumption.

To activate this mode, the device automatically switch themselves to low power mode when the device addresses remain stable after 30 ns from data valid. It is not necessary to control \overline{CE} , \overline{WE} , and \overline{OE} in this mode. The current consumed is typically 1 μ A (CMOS Level).

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device read-out the data for changed addresses.

Autoselect

The Autoselect mode allows reading out of a binary code and identifies its manufacturer and type. It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 . Two identifier bytes may then be sequenced from the devices outputs by toggling A_0 . All addresses can be either High or Low except A_6 , A_3, A_2, A_1 and A_0 . See "MBM29PL32TM/BM User Bus Operations (Word Mode : BYTE = VIH)" and "MBM29PL32TM/BM User Bus Operations (Byte Mode : BYTE = VIL)" in ■DEVICE BUS OPERATION.

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29PL32TM/BM Standard Command Definitions" in ■DEVICE BUS OPERATION. Refer to Autoselect Command section.

In Word mode, a read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h). A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh and 0Fh. Notice that the above applies to Word mode. The addresses and codes differ from those of Byte mode. Refer to "Sector Group Protection Verify Autoselect Codes" in ■DEVICE BUS OPERATION.

Read Mode

The device has two control functions required to obtain data at the outputs. \overline{CE} is the power control and used for a device selection. \overline{OE} is the output control and used to gate data to the output pins.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable \overline{CE} to valid data at the output pins. The output enable access time is the delay from the falling edge of \overline{OE} to valid data at the output pins. (Assuming the addresses have been stable for at least $t_{ACC-tOE}$ time.) When reading out a data without changing addresses after power-up, input hardware reset or to change \overline{CE} pin from "H" or "L".

Page Mode Read

The device is capable of fast read access for random locations within limited address location called Page. The Page size of the device is 8 bytes / 4 words, within the appropriate Page being selected by the higher address bits A_{20} to A_2 and the address bits A_1 to A_0 in Word mode (A_1 to A_{-1} in Byte mode) determining the specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The initial page access is equal to the random access (t_{ACC}) and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to the page address access time(t_{PACC}). Here again, \overline{CE} selects the device and \overline{OE} is the output control and should be used to gate data to the output pins if the device is selected. Fast Page mode, accesses are obtained by keeping A_{20} to A_2 constant and changing A_1 and A_0 in Word mode (A_1 to A_{-1} in Byte mode) to select the specific word within that Page.

Output Disable

With the \overline{OE} input at logic high level (V_{IH}), output from the devices are disabled. This may cause the output pins to be in a high impedance state.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the device function.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing \overline{WE} to V_{IL} , while \overline{CE} is at V_{IL} and \overline{OE} is at V_{IH} . Addresses are latched on the falling edge of \overline{WE} or \overline{CE} , whichever starts later; while data is latched on the rising edge of \overline{WE} or \overline{CE} , whichever starts first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The device features hardware sector group protection. This feature will disable both program and erase operations in any combination of thirty two sector groups of memory. See "Sector Group Address Table (MBM29PL32TM)" and "Sector Group Address Table (MBM29PL32BM)" in ■DEVICE BUS OPERATION. The user's side can use the sector group protection using programming equipment. The device is shipped with all sector groups that are unprotected.

To activate it, the programming equipment must force V_{ID} on address pin A_9 and control pin \overline{OE} , $\overline{CE} = V_{IL}$ and $A_6 = A_3 = A_2 = A_0 = V_{IL}$, $A_1 = V_{IH}$. The sector group addresses (A_{20} , A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12}) should be set to the sector to be protected. "Sector Address Table (MBM29PL32TM)" and "Sector Address Table (MBM29PL32BM)" in ■DEVICE BUS OPERATION defines the sector address for each of the seventy-one (71) individual sectors, and "Sector Group Address Table (MBM29PL32TM)" and "Sector Group Address Table (MBM29PL32BM)" in ■DEVICE BUS OPERATION defines the sector group address for each of the twenty-four (24) individual group sectors. Programming of the protection circuitry begins on the falling edge of the \overline{WE} pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the \overline{WE} pulse. See "Sector Group Protection Timing Diagram" in ■SWITCHING WAVEFORMS and "Sector Group Protection Algorithm" in ■FLOW CHART for sector group protection timing diagram and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with \overline{CE} and \overline{OE} at V_{IL} and \overline{WE} at V_{IH} . Scanning the sector group addresses (A_{20} , A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12}) while (A_6 , A_3 , A_2 , A_1 , A_0) = (0, 0, 0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce "0" for unprotected sectors. In this mode, the lower order addresses, except for A_0 , A_1 , A_2 , A_3 , and A_6 can be either High or Low. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes. A_{-1} requires applying to V_{IL} on Byte mode.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location $XX02h$, where the higher order addresses (A_{20} , A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12}) are the desired sector group address will produce a logical "1" at DQ_0 for a protected sector group. See "Sector Group Protection Verify Autoselect Codes" in ■DEVICE BUS OPERATION for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the devices in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{\text{RESET}}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{\text{RESET}}$ pin, all the previously protected sector groups will be protected again. Refer to “Temporary Sector Group Unprotection Timing Diagram” in ■SWITCHING WAVEFORMS and “Temporary Sector Group Unprotection Algorithm” in ■FLOW CHART.

Hardware Reset

The devices may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL} from V_{IH} . The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least “ t_{RP} ” in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode “ t_{READY} ” after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the devices require an additional “ t_{RH} ” before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted.

Write Protect ($\overline{\text{WP}}$)

The Write Protection function provides a hardware method of protecting certain outermost 8K bytes / 4K words sectors without using V_{ID} . This function is one of two provided by the $\overline{\text{WP/ACC}}$ pin.

If the system asserts V_{IL} on the $\overline{\text{WP/ACC}}$ pin, the device disables program and erase functions in the outermost 8K bytes / 4K words sectors independently of whether this sector was protected or unprotected using the method described in “Sector Group Protection” above.

If the system asserts V_{IH} on the $\overline{\text{WP/ACC}}$ pin, the device reverts of whether the outermost 8K bytes / 4K words sectors were last set to be protected to the unprotected status. Sector protection or unprotection for this sector depends on whether this was last protected or unprotected using the method described in “Sector protection/unprotection”.

Accelerated Program Operation

The device offers accelerated program operation which enables programming in high speed. If the system asserts V_{ACC} to the $\overline{\text{WP/ACC}}$ pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 85%. This function is primarily intended to allow high speed programming, so caution is needed as the sector group becomes temporarily unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device is automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the $\overline{\text{WP/ACC}}$ pin returns the device to normal operation. Do not remove V_{ACC} from the $\overline{\text{WP/ACC}}$ pin while programming. See “Accelerated Program Timing Diagram” in ■SWITCHING WAVEFORM.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. “MBM29PL32TM/BM Standard Command Definitions” in ■DEVICE BUS OPERATION shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress. Moreover Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands must be asserted to DQ₇ to DQ₀ and DQ₁₅ to DQ₈ bits are ignored.

Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ₅ = 1) to Read mode, the Reset operation is initiated by writing the Reset command sequence into the command register. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically be in the reset state after power-up. In this case, a command sequence is not required in order to read data.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A₉ to a high voltage. However applying high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the address and the Autoselect command. Then the manufacture and device codes can be read from the address, and an actual data of memory cell can be read from the another address.

Following the command write, a read cycle from address 00h returns the manufactures’s code (Fujitsu = 04h). A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at address of 0Eh as well as at 0Fh. Notice that above applies to Word mode. The addresses and codes differ from those of Byte mode. Refer to “Sector Group Protection Verify Autoselect Codes” in ■DEVICE BUS OPERATION.

To terminate the operation, it is necessary to write the Reset command into the register. To execute the Autoselect command during the operation, Reset command must be written before the Autoselect command.

Programming

The devices are programmed on a word-by-word (or byte-by-byte) basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of \overline{CE} or \overline{WE} , whichever happens later and the data is latched on the rising edge of \overline{CE} or \overline{WE} , whichever happens first. The rising edge of \overline{CE} or \overline{WE} (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ₇ ($\overline{\text{Data Polling}}$), DQ₆ (Toggle Bit) or RY/BY. The $\overline{\text{Data Polling}}$ and Toggle Bit are automatically performed at the memory location being programmed.

The programming operation is completed when the data on DQ₇ is equivalent to data written to this bit at which the devices return to the read mode and program addresses are no longer latched. Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance. Hence $\overline{\text{Data Polling}}$ requires the same address which is being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any address sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may result in either failure condition or an apparent success according to the data polling algorithm. But a read from Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Note that attempting to program a “1” over a “0” will result in programming failure. This precaution is the same with Fujitsu standard NOR devices. “Embedded Program™ Algorithm” in ■FLOW CHART illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Program Suspend/Resume

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during Embedded Program operation immediately suspends the programming. The Program Suspend command can also be issued during a programming operation while an erase is suspended. Refer to "Erase Suspend/Resume" for the detail.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1us and updates the status bits. After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system also writes the Autoselect command sequence in the Program Suspend mode. The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Program Resume command to exit from the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

Write Buffer Programming Operations

Write Buffer Programming allows the system write to series of 16 words in one programming operation. This results in faster effective word programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle selecting the Sector Address in which programming will occur. In forth cycle contains both Sector Address and unique code for data bus width will be loaded into the page buffer at the Sector Address in which programming will occur.

The system then writes the starting address/data combination. This “starting address” must be the same Sector Address used in third and fourth cycles and its lower addresses of A₃ to A₀ should be 0h. All subsequent address must be incremented by 1. Addresses are latched on the falling edge of \overline{CE} or \overline{WE} , whichever happens later and the data is latched on the rising edge of \overline{CE} or \overline{WE} , whichever happens first. The rising edge of \overline{CE} or \overline{WE} (whichever happens first) starts programming. Upon executing the Write Buffer Programming Operations command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

DQ₇(\overline{Data} Polling), DQ₆(Toggle Bit), DQ₅(Exceeded Timing Limits), DQ₁(Write-to-Buffer Abort) should be monitored to determine the device status during Write Buffer Programming. In addition to these functions, it is also possible to indicate to the host system that Write Buffer Programming Operations are either in progress or have been completed by RY/BY. See “Hardware Sequence Flags”.

The \overline{Data} polling techniques described in “Data Polling Algorithm” in ■FLOW CHART should be used while monitoring the last address location loaded into the write buffer. In addition, it is not necessary to specify an address in Toggle Bit techniques described in “Toggle Bit Algorithm” in ■FLOW CHART. The automatic programming operation is completed when the data on DQ₇ is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (See "Hardware Sequence Flags").

The write-buffer programming operation can be suspended using the standard program suspend/resume commands.

Once the write buffer programming is set, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data combination will abort the Write Buffer Programming operation and the device will continue busy state.

The Write Buffer Programming Sequence can be ABORTED by doing the following :

- Different Sector Address is asserted.
- Write data other than the “Program Buffer to Flash” command after the specified number of “data load” cycles.

A “Write-to-Buffer-Abort Reset” command sequence must be written to the device to return to read mode. (See “MBM29PL32TM/BM Standard Command Definitions” in ■DEVICE BUS OPERATION for details on this command sequence.)

Chip Erase

Chip erase is a six bus cycle operation. It begins two “unlock” write cycles followed by writing the “set-up” command, and two “unlock” write cycles followed by the chip erase command which invokes the Embedded Erase algorithm.

The device does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm the devices automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the erase operation status by using DQ_7 ($\overline{\text{Data Polling}}$), DQ_6 ($\overline{\text{Toggle Bit I}}$) and DQ_2 ($\overline{\text{Toggle Bit II}}$) or RY/BY output signal. The chip erase begins on the rising edge of the last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first from last command sequence and completes when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read mode.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command.

Multiple sectors may be erased concurrently by writing the same six bus cycle operations. This sequence is followed by writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than Erase Time-out time(t_{row}). Otherwise that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can reoccur after the last Sector Erase command is written. A time-out of “ t_{row} ” from the rising edge of last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first, will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first occurs within the “ t_{row} ” time-out window the timer is reset (monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3 , Sector Erase Timer). Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete (refer to the Write Operation Status). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 70).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase using the Embedded Erase Algorithm. When erasing a sector, the remaining unselected sectors remain unaffected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data Polling}}$), DQ_6 ($\overline{\text{Toggle Bit}}$) or RY/BY.

The sector erase begins after the “ t_{row} ” time-out from the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever happens first for the last sector erase command pulse and completes when the data on DQ_7 is “1” (see Write Operation Status section), at which the devices return to the read mode. Data polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt Sector Erase operation and then perform read or programming to a sector not being erased. This command is applicable ONLY during the Sector Erase operation within the time-out period for sector erase. Writing the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the "Erase Resume" command (30h) resumes the erase operation.

When the "Erase Suspend" command is written during the Sector Erase operation, the device takes maximum of "t_{SPD}" to suspend the erase operation. When the devices enter the erase-suspended mode, the RY/ $\overline{\text{BY}}$ output pin will be at High-Z and the DQ₇ bit will be at logic "1" and DQ₆ will stop toggling. The user must use the address of the erasing sector for reading DQ₆ and DQ₇ to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation is suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase-suspended. Reading successively from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ₂ to toggle. See the section on DQ₂.

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, it is the same as programming in the regular Program mode, except that the data must be programmed to sectors that are not erase-suspended. Reading successively from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ₂ to toggle. The end of the erase-suspended Program operation is detected by the Data polling of $\overline{\text{DQ}}_7$ or by the Toggle Bit I of DQ₆, which is the same as the regular Program operation. Note that DQ₇ must be read from the Program address while DQ₆ can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Fast Mode Set/Reset

The device has Fast Mode function. It dispenses with the initial two unlock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming consists of two cycles instead of four bus cycles in standard program command. The read operation is also executed after exiting this mode. During the Fast mode, do not write any command other than the Fast program/Fast mode reset command. To exit from this mode, write Fast Mode Reset command into the command register. (Refer to the "Embedded Program™ Algorithm for Fast Mode" in ■FLOW CHART.) The V_{CC} active current is required even $\overline{\text{CE}} = V_{\text{IH}}$ during Fast Mode.

Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). See "Embedded Program™ Algorithm for Fast Mode" in ■FLOW CHART.

Extended Sector Group Protection

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables protection of the sector group by forcing V_{ID} on \overline{RESET} pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force V_{ID} and control timing for control pins. The only \overline{RESET} pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on \overline{RESET} pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then the sector group addresses pins ($A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}$ and A_{12}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set to the sector group to be protected (set V_{IL} for the other addresses pins is recommended), and write extended sector group protection command (60h). A sector group is typically protected in 250 μ s. To verify programming of the protection circuitry, the sector group addresses pins ($A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}$ and A_{12}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set and write a command (40h). Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", write the extended sector group protection command (60h) again. To terminate the operation, set \overline{RESET} pin to V_{IH} . (Refer to the "Extended Sector Group Protection Timing Diagram" in ■SWITCHING WAVEFORMS and "Extended Sector Group Protection Algorithm" in ■FLOW CHART.)

Query Command (CFI : Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is "0". Refer to the CFI code table. To terminate operation, it is necessary to write the Reset command sequence into the register. (See "Common Flash Memory Interface Code" in ■DEVICE BUS OPERATION.)

HiddenROM Mode

(1) HiddenROM Region

The HiddenROM (HiddenROM) feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the HiddenROM region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The HiddenROM region is 256 bytes / 128 words in length. After the system writes the HiddenROM Entry command sequence, it may read the HiddenROM region by using device addresses A_6 to A_0 (A_{20} to A_7 are all "0"). That is, the device sends only program command that would normally be sent to the address to the HiddenROM region. This mode of operation continues until the system issues the Exit HiddenROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the address.

If you request Fujitsu to program the ESN in the device, please contact a Fujitsu representative for more information.

(2) HiddenROM Entry Command

The device has a HiddenROM area with One Time Protect function. This area is to enter the security code and to enable the change of the code once set. Programming is allowed in this area until it is protected. However, once it gets protected, it is impossible to unprotect. Therefore, extreme caution is required.

The HiddenROM area is 256 bytes / 128 words. This area is in SA0. Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. It is called HiddenROM mode when the HiddenROM area appears.

Sectors other than the block area SA0 can be read during HiddenROM mode. Read/program of the HiddenROM area is possible during HiddenROM mode. Write the HiddenROM reset command sequence to exit the HiddenROM mode. Note that any other commands should not be issued than the HiddenROM program/protection/reset commands during the HiddenROM mode. When you issue the other commands including the suspend resume capability, send the HiddenROM reset command first to exit the HiddenROM mode and then issue each command.

(3) HiddenROM Program Command

To program the data to the HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the usual program command, except that it needs to write the command during HiddenROM mode. Therefore the detection of completion method is the same as in the past, using the DQ₇ data pooling, DQ₆ Toggle bit or RY/BY. You should pay attention to the address to be programmed. If an address not in the HiddenROM area is selected, the previous data will be deleted.

During the write into the HiddenROM region, the program suspend command issuance is prohibited.

(4) HiddenROM Protect Command

There are two methods to protect the HiddenROM area. One is to write the sector group protect setup command (60h), set the sector address in the HiddenROM area and $(A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0)$, and write the sector group protect command (60h) during the HiddenROM mode. The same command sequence may be used because it is the same as the extension sector group protect in the past, except that it is in the HiddenROM mode and does not apply high voltage to the RESET pin. Please refer to above mentioned "Extended Sector Group Protection" for details of sector group protect setting.

The other method is to apply high voltage (V_{ID}) to A_9 and OE, set the sector address in the HiddenROM area and $(A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0)$, and apply the write pulse during the HiddenROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A_9 , specify $(A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0)$ and the sector address in the HiddenROM area, and read. When "1" appears on DQ₀, the protect setting is completed. "0" will appear on DQ₀ if it is not protected. Apply write pulse again. The same command sequence could be used for the above method because other than the HiddenROM mode, it is the same as the sector group protect previously mentioned.

Take note that other sector groups will be affected if an address other than those for the HiddenROM area is selected for the sector group address, so please be careful. Pay close attention that once it is protected, protection CANNOT BE CANCELLED.

Write Operation Status

Detailed in “Hardware Sequence Flags” are all the status flags which can determine the status of the device for current mode operation. During sector erase, the part provides the status flags automatically to the I/O ports. The information on DQ₂ is address sensitive. If an address from an erasing sector is consecutively read, then the DQ₂ bit will toggle. However DQ₂ will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing.

Once erase suspend is entered address sensitivity still applies. If the address of a non-erasing sector (one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (one unavailable for read) is applied, the device will output its status bits.

Hardware Sequence Flags

| Status | | DQ ₇ | DQ ₆ | DQ ₅ | DQ ₃ | DQ ₂ | DQ ₁ ^{*3} | |
|--|----------------------------|---|-------------------|-----------------|-----------------|----------------------|-------------------------------|------|
| In Progress | Embedded Program Algorithm | \overline{DQ}_7 | Toggle | 0 | 0 | 1 | 0 | |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle ^{*1} | N/A | |
| | Program Suspend Mode | Program-Suspend-Read (Program Suspended Sector) | Data | Data | Data | Data | Data | Data |
| | | Program-Suspend-Read (Non-Program Suspended Sector) | Data | Data | Data | Data | Data | Data |
| | Erase Suspend Mode | Erase-Suspend-Read (Erase Suspended Sector) | 1 | 1 | 0 | 0 | Toggle ^{*1} | N/A |
| | | Erase-Suspend-Read (Non-Erase Suspended Sector) | Data | Data | Data | Data | Data | Data |
| Erase-Suspend-Program (Non-Erase Suspended Sector) | | \overline{DQ}_7 | Toggle | 0 | 0 | 1 ^{*2} | N/A | |
| Exceeded Time Limits | Embedded Program Algorithm | \overline{DQ}_7 | Toggle | 1 | 0 | 1 | N/A | |
| | Embedded Erase Algorithm | 0 | Toggle | 1 | 1 | N/A | N/A | |
| | Erase Suspend Mode | Erase-Suspend-Program (Non-Erase Suspended Sector) | \overline{DQ}_7 | Toggle | 1 | 0 | N/A | N/A |
| Write to Buffer ^{*4} | BUSY State | \overline{DQ}_7 | Toggle | 0 | N/A | N/A | 0 | |
| | Exceeded Timing Limits | \overline{DQ}_7 | Toggle | 1 | N/A | N/A | 0 | |
| | ABORT State | N/A | Toggle | 0 | N/A | N/A | 1 | |

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ₂ to toggle.

*2 : Reading from non-erase suspend sector address will indicate logic “1” at the DQ₂ bit.

*3 : DQ₁ indicates the Write-to-Buffer ABORT status during Write-Buffer-Programming operations.

*4 : The \overline{Data} Polling algorithm detailed in “ \overline{Data} Polling Algorithm” in ■FLOW CHART should be used for Write-Buffer-Programming operations. Note that \overline{DQ}_7 during Write-Buffer-Programming indicates the data-bar for DQ₇ data for the LAST LOADED WRITE-BUFFER ADDRESS location.

DQ₇

$\overline{\text{Data}}$ Polling

The devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read devices will produce reverse data last written to DQ₇. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ₇. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ₇ output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a “1” at the DQ₇ output. The flowchart for $\overline{\text{Data}}$ Polling (DQ₇) is shown in “ $\overline{\text{Data}}$ Polling Algorithm” in ■FLOW CHART.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise, the status may become invalid.

If a program address falls within a protected sector, Data polling on DQ₇ is active for approximately 1 μs , then the device returns to read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ₇ is active for approximately 100 μs , then the device returns to read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ₇) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ₇ at one instant of time, and then that byte's valid data the next. Depending on when the system samples the DQ₇ output, it may read the status or valid data. Even if the device completes the Embedded Algorithm operation and DQ₇ has a valid data, the data outputs on DQ₆ to DQ₀ may still be invalid. The valid data on DQ₇ to DQ₀ will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspendmode or sector erase time-out.

See “ $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram” in ■SWITCHING WAVEFORM for the $\overline{\text{Data}}$ Polling timing specifications and diagram.

DQ₆

Toggle Bit I

The device also feature the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling) data from the devices will result in DQ₆ toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ₆ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programm operation, if the sector being written to is protected, the Toggle bit will toggle for about 1 μs and then stop toggling with the data unchanged. In erase, the device will erase all the selected sectors except for the protected ones. If all selected sectors are protected, the chip will toggle the Toggle bit for about 100 μs and then drop back into read mode, having data kept remained.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ₆ to toggle. See “Toggle Bit I Timing Diagram during Embedded Algorithm Operations” in ■SWITCHING WAVEFORM for the Toggle Bit I timing specifications and diagram.

DQ₅

Exceeded Timing Limits

DQ₅ will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ₅ will produce a “1”. This is a failure condition indicating that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in “MBM29PL32TM/BM User Bus Operations (Word Mode : BYTE = VIH)” and “MBM29PL32TM/BM User Bus Operations (Byte Mode : BYTE = VIL)” in ■DEVICE BUS OPERATION.

The DQ₅ failure condition may also appear if a user tries to program a non blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ₇ bit and DQ₆ never stop toggling. Once the device has exceeded timing limits, the DQ₅ bit will indicate a “1”. Note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with command sequence.

DQ₃

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ₃ will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates a valid erase command has been written, DQ₃ may be used to determine whether the sector erase timer window is still open. If DQ₃ is “1” the internally controlled erase cycle has begun. If DQ₃ is “0”, the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ₃ prior to and following each subsequent Sector Erase command. If DQ₃ were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags”.

DQ₂

Toggle Bit II

This Toggle bit II, along with DQ₆, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ₂ to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ₂ to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic “1” at the DQ₂ bit.

DQ₆ is different from DQ₂ in that DQ₆ toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ₇, is summarized as follows:

For example, DQ₂ and DQ₆ can be used together to determine if the erase-suspend-read mode is in progress. (DQ₂ toggles while DQ₆ does not.) See also “Hardware Sequence Flags” and “DQ₂ vs. DQ₆” in ■SWITCHING WAVEFORM.

Furthermore, DQ₂ can also be used to determine which sector is being erased. At the erase mode, DQ₂ toggles if this bit is read from an erasing sector.

Reading Toggle Bits DQ₆/ DQ₂

Whenever the system initially begins reading Toggle bit status, it must read DQ₇ to DQ₀ at least twice in a row to determine whether a Toggle bit is toggling. Typically a system would note and store the value of the Toggle bit after the first read. After the second read, the system would compare the new value of the Toggle bit with the first. If the Toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ₇ to DQ₀ on the following read cycle.

However, if, after the initial two read cycles, the system determines that the Toggle bit is still toggling, the system also should note whether the value of DQ₅ is high (see the section on DQ₅) . If it is, the system should then determine again whether the Toggle bit is toggling, since the Toggle bit may have stopped toggling just as DQ₅ went high. If the Toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the Toggle bit is toggling and DQ₅ has not gone high. The system may continue to monitor the Toggle bit and DQ₅ through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to "Toggle Bit Algorithm" in ■FLOW CHART.)

Toggle Bit Status

| Mode | DQ ₇ | DQ ₆ | DQ ₂ |
|--|-------------------|-----------------|-----------------|
| Program | \overline{DQ}_7 | Toggle | 1 |
| Erase | 0 | Toggle | Toggle *1 |
| Erase-Suspend-Read (Erase-Suspended Sector) | 1 | 1 | Toggle *1 |
| Erase-Suspend-Program | \overline{DQ}_7 | Toggle | 1 *2 |

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ₂ to toggle.

*2 : Reading from the non-erase suspend sector address will indicate logic "1" at the DQ₂ bit.

DQ₁

Write-to-Buffer Abort

DQ₁ indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ₁ produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See "Write Buffer Programming Operations" section for more details.

RY/ \overline{BY}

Ready/Busy

The device provides a RY/ \overline{BY} open-drain output pin to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. If the device is placed in an Erase Suspend mode, the RY/ \overline{BY} output will be high, by means of connecting with a pull-up resistor to V_{cc}.

During programming, the RY/ \overline{BY} pin is driven low after the rising edge of the fourth \overline{WE} pulse. During an erase operation, the RY/ \overline{BY} pin is driven low after the rising edge of the sixth \overline{WE} pulse. The RY/ \overline{BY} pin will indicate a busy condition during the \overline{RESET} pulse. See "RY/ \overline{BY} Timing Diagram during Program/Erase Operation Timing Diagram" and "RESET Timing Diagram (During Embedded Algorithms)" in ■SWITCHING WAVEFORM for a detailed timing diagram. The RY/ \overline{BY} pin is pulled high in standby mode.

Since this is an open-drain output, RY/ \overline{BY} pins can be tied together in parallel with a pull-up resistor to V_{cc}.

Word/Byte Configuration

$\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the device. When this pin is driven high, the device operates in the word (16-bit) mode. Data is read and programmed at DQ₁₅ to DQ₀. When this pin is driven low, the device operates in byte (8-bit) mode. In this mode, DQ₁₅/A₋₁ pin becomes the lowest address bit, and DQ₁₄ to DQ₈ bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ₇ to DQ₀ and DQ₁₅ to DQ₈ bits are ignored.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically reset the internal state machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

(1) Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} . If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO} . It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} .

If Embedded Erase Algorithm is interrupted, the intervened erasing sector(s) is(are) not valid.

(2) Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

(3) Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{WE}} = V_{IH}$. To initiate a write, $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

(4) Power-up Write Inhibit

Power-up of the devices with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to read mode on power-up.

(5) Sector Protection

Device user is able to protect each sector group individually to store and protect data. Protection circuit voids both write and erase commands that are addressed to protected sectors.

Any commands to write or erase addressed to protected sector are ignored .

■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|--|------------------------------------|--------|----------------------|------|
| | | Min | Max | |
| Storage Temperature | T _{stg} | -55 | +125 | °C |
| Ambient Temperature with Power Applied | T _A | -20 | +85 | °C |
| Voltage with Respect to Ground All Pins Except A ₉ , $\overline{\text{OE}}$, and $\overline{\text{RESET}}$ *1,*2 | V _{IN} , V _{OUT} | -0.5 | V _{CC} +0.5 | V |
| Power Supply Voltage *1 | V _{CC} | -0.5 | +4.0 | V |
| A ₉ , $\overline{\text{OE}}$, and $\overline{\text{RESET}}$ *1,*3 | V _{IN} | -0.5 | +12.5 | V |
| $\overline{\text{WP/ACC}}$ *1,*3 | V _{ACC} | -0.5 | +12.5 | V |

*1 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -0.2 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns

*3 : Minimum DC input voltage is -0.5V. During voltage transitions, these pins may undershoot V_{SS} to -0.2 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-V_{CC}) dose not exceed to +9.0 V. Maximum DC input voltage is +12.5 V which may overshoot to +14.0 V for periods of up to 20 ns .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES*1

| Parameter | | Symbol | Value | | Unit |
|-----------------------------------|----|-----------------|-------|------|------|
| | | | Min | Max | |
| Ambient Temperature | 90 | T _A | -20 | +70 | °C |
| | 10 | | -20 | +85 | |
| V _{CC} Supply Voltage *2 | | V _{CC} | +3.0 | +3.6 | V |

*1 : Operating ranges define those limits between which the functionality of the device is guaranteed.

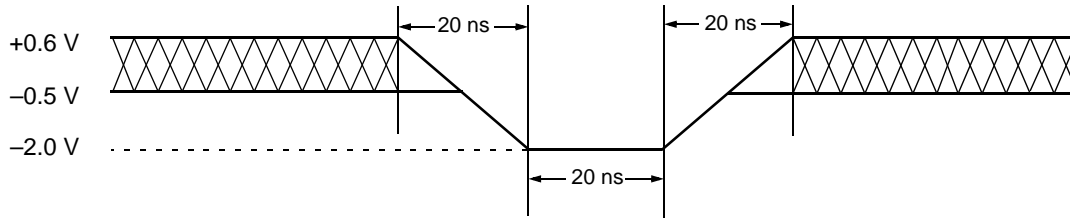
*2 : Voltage is defined on the basis of V_{SS} = GND = 0V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

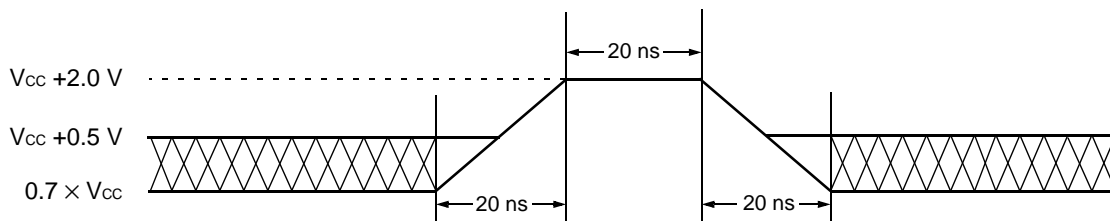
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

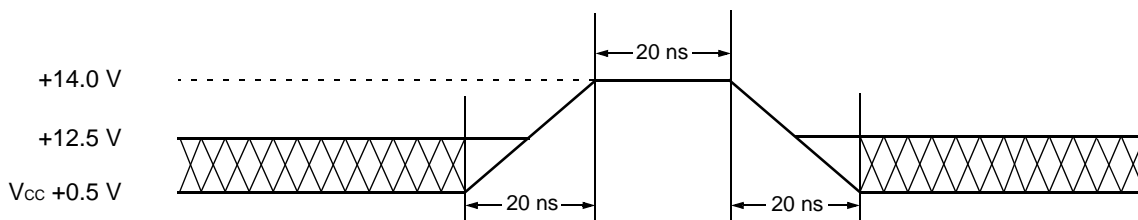
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note: This waveform is applied for A_9 , \overline{OE} , \overline{RESET} , and Acc .

Maximum Overshoot Waveform 2

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

| Parameter | Symbol | Conditions | Value | | | Unit | |
|--|------------------|--|--------------------------------|------|-----------------------|------|----|
| | | | Min | Typ | Max | | |
| Input Leakage Current | I _{LI} | V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC} Max | — | — | — | μA | |
| | | — | — | — | | | |
| Output Leakage Current | I _{LO} | V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC} Max | -2.0 | — | +2.0 | μA | |
| A ₉ , $\overline{\text{OE}}$, $\overline{\text{RESET}}$ Inputs Leakage Current | I _{LIT} | V _{CC} = V _{CC} Max, A ₉ , $\overline{\text{OE}}$, $\overline{\text{RESET}}$ = 12.5 V | — | — | 35 | μA | |
| V _{CC} Active Current (Read) *1,*2 | I _{CC1} | $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , f = 5 MHz | Word | — | 18 | 20 | mA |
| | | — | Byte | — | 16 | 20 | |
| | | $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , f = 10 MHz | Word | — | 35 | 50 | |
| | | — | Byte | — | 35 | 50 | |
| V _{CC} Active Current (Intra-Page Read) *2 | I _{CC2} | $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , t _{PRC} = 25ns, 4-Word | — | 10 | 20 | mA | |
| V _{CC} Active Current (Program / Erase) *2,*3 | I _{CC3} | $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} | — | 50 | 60 | mA | |
| V _{CC} Standby Current *2 | I _{CC4} | $\overline{\text{CE}}$ = V _{CC} ± 0.3 V, $\overline{\text{RESET}}$ = V _{CC} ± 0.3 V, $\overline{\text{OE}}$ = V _{IH} , $\overline{\text{WP/ACC}}$ = V _{CC} ± 0.3 V | — | 1 | 5 | μA | |
| V _{CC} Reset Current *2 | I _{CC5} | $\overline{\text{RESET}}$ = V _{CC} ± 0.3 V, $\overline{\text{WP/ACC}}$ = V _{CC} ± 0.3 V | — | 1 | 5 | μA | |
| V _{CC} Automatic Sleep Current *4 | I _{CC6} | $\overline{\text{CE}}$ = V _{SS} ± 0.3 V, $\overline{\text{RESET}}$ = V _{CC} ± 0.3 V, V _{IN} = V _{CC} ± 0.3V or V _{SS} ± 0.3V, $\overline{\text{WP/ACC}}$ = V _{CC} ± 0.3 V | — | 1 | 5 | μA | |
| V _{CC} Active Current (Erase-Suspend-Program) *2 | I _{CC7} | $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} | — | 50 | 60 | mA | |
| ACC Accelerated Program Current | I _{ACC} | $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , V _{CC} = V _{CC} Max, $\overline{\text{WP/ACC}}$ = V _{ACC} Max | $\overline{\text{WP/ACC}}$ pin | — | — | 20 | mA |
| | | — | V _{CC} Pin | — | — | 60 | |
| Input Low Level | V _{IL} | — | -0.5 | — | 0.6 | V | |
| Input High Level | V _{IH} | — | 0.7×V _{CC} | — | V _{CC} + 0.3 | V | |
| Voltage for $\overline{\text{WP/ACC}}$ Sector Protection/Unprotection and Program Acceleration | V _{ACC} | V _{CC} = 3.0 V to 3.6 V | 11.5 | 12.0 | 12.5 | V | |
| Voltage for Autoselect, and Temporary Sector Unprotected | V _{ID} | V _{CC} = 3.0 V to 3.6 V | 11.5 | 12.0 | 12.5 | V | |
| Output Low Voltage Level | V _{OL} | I _{OL} = 4.0 mA, V _{CC} = V _{CC} Min | — | — | 0.45 | V | |
| Output High Voltage Level | V _{OH} | I _{OH} = -2.0 mA, V _{CC} = V _{CC} Min | 0.85×V _{CC} | — | — | V | |
| Low V _{CC} Lock-Out Voltage | V _{LKO} | — | 2.3 | — | 2.5 | V | |

- *1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
- *2 : Maximum I_{CC} values are tested with $V_{CC} = V_{CC\ Max}$
- *3 : I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.
- *4 : Automatic sleep mode enables the low power mode when address remain stable for $t_{ACC} + 30\ ns$.

2. AC Characteristics

• Read Only Operations Characteristics

| Parameter | Symbols | | Condition | Value* | | | | Unit |
|--|-------------------------|--------------------|--|--------|-----|-----|-----|------|
| | JEDEC | Standard | | 90 | | 10 | | |
| | | | | Min | Max | Min | Max | |
| Read Cycle Time | t _{AVAV} | t _{RC} | — | 90 | — | 100 | — | ns |
| Address to Output Delay | t _{AVQV} | t _{ACC} | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$ | — | 90 | — | 100 | ns |
| Chip Enable to Output Delay | t _{ELQV} | t _{CE} | $\overline{OE} = V_{IL}$ | — | 90 | — | 100 | ns |
| Page Read Cycle Time | — | t _{PRC} | — | 25 | — | 30 | — | ns |
| Page Address to Output Delay | — | t _{PACC} | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$ | — | 25 | — | 30 | ns |
| Output Enable to Output Delay | t _{GLQV} | t _{OE} | — | — | 25 | — | 30 | ns |
| Chip Enable to Output High-Z | t _{EHQZ} | t _{DF} | — | — | 25 | — | 30 | ns |
| Output Enable Hold Time | Read | t _{OEH} | — | 0 | — | 0 | — | ns |
| | Toggle and Data Polling | | — | 10 | — | 10 | — | ns |
| Output Enable to Output High-Z | t _{GHQZ} | t _{DF} | — | — | 25 | — | 30 | ns |
| Output Hold Time From Addresses, \overline{CE} or \overline{OE} , Whichever Occurs First | t _{AXQX} | t _{OH} | — | 0 | — | 0 | — | ns |
| \overline{RESET} Pin Low to Read Mode | — | t _{READY} | — | — | 20 | — | 20 | μs |

* : Test Conditions :

Output Load : 1 TTL gate and 30 pF

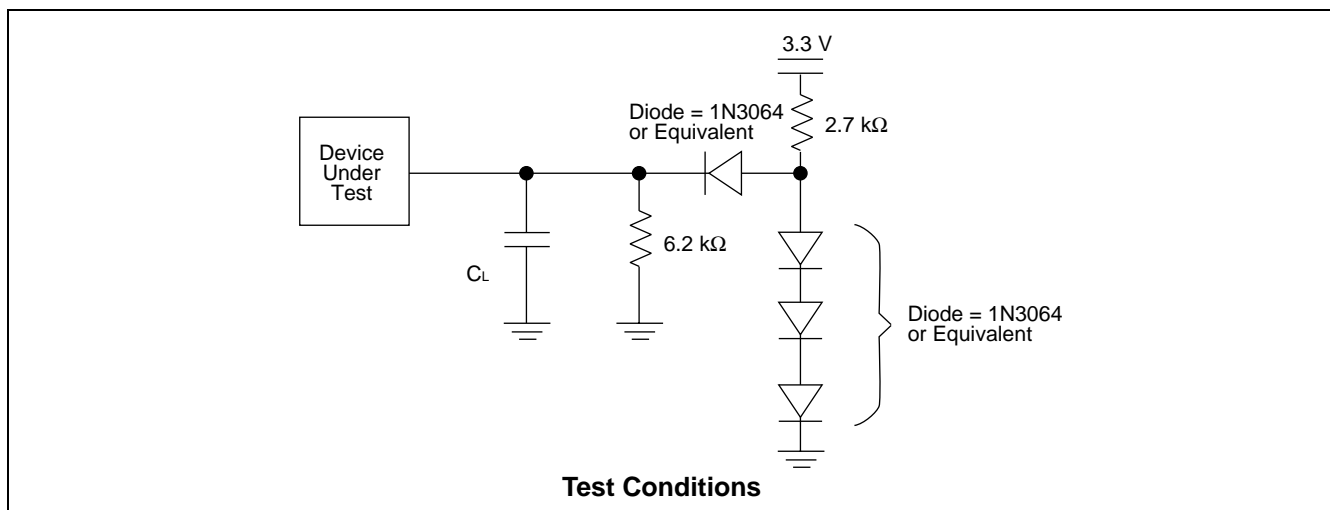
Input rise and fall times : 5 ns

Input pulse levels : 0.0 V or V_{CC}

Timing measurement reference level

Input : V_{CC} / 2

Output : V_{CC} / 2



• Write (Erase/Program) Operations

| Parameter | Symbol | | Value | | | | | | Unit |
|--|--------------------|--------------------|-------|------|-----|-----|------|-----|------|
| | | | 90 | | | 10 | | | |
| | JEDEC | Standard | Min | Typ | Max | Min | Typ | Max | |
| Write Cycle Time | t _{AVAV} | t _{WC} | 90 | — | — | 100 | — | — | ns |
| Address Setup Time | t _{AVWL} | t _{AS} | 0 | — | — | 0 | — | — | ns |
| Address Setup Time to \overline{OE} Low During Toggle Bit Polling | — | t _{ASO} | 15 | — | — | 15 | — | — | ns |
| Address Hold Time | t _{WLAX} | t _{AH} | 45 | — | — | 45 | — | — | ns |
| Address Hold Time from \overline{CE} or \overline{OE} High During Toggle Bit Polling | — | t _{AHT} | 0 | — | — | 0 | — | — | ns |
| Data Setup Time | t _{DVWH} | t _{DS} | 35 | — | — | 35 | — | — | ns |
| Data Hold Time | t _{WHDX} | t _{DH} | 0 | — | — | 0 | — | — | ns |
| Output Enable Setup Time | — | t _{OES} | 0 | — | — | 0 | — | — | ns |
| \overline{CE} High During Toggle Bit Polling | — | t _{CEPH} | 20 | — | — | 20 | — | — | ns |
| \overline{OE} High During Toggle Bit Polling | — | t _{OEPH} | 20 | — | — | 20 | — | — | ns |
| Read Recover Time Before Write (\overline{OE} High to \overline{WE} Low) | t _{GHWL} | t _{GHWL} | 0 | — | — | 0 | — | — | ns |
| Read Recover Time Before Write (\overline{OE} High to \overline{CE} Low) | t _{GHEL} | t _{GHEL} | 0 | — | — | 0 | — | — | ns |
| \overline{CE} Setup Time | t _{ELWL} | t _{CS} | 0 | — | — | 0 | — | — | ns |
| \overline{WE} Setup Time | t _{WLLEL} | t _{WS} | 0 | — | — | 0 | — | — | ns |
| \overline{CE} Hold Time | t _{WHEH} | t _{CH} | 0 | — | — | 0 | — | — | ns |
| \overline{WE} Hold Time | t _{EHWH} | t _{WH} | 0 | — | — | 0 | — | — | ns |
| \overline{CE} Pulse Width | t _{ELEH} | t _{CP} | 35 | — | — | 35 | — | — | ns |
| Write Pulse Width | t _{WLWH} | t _{WP} | 35 | — | — | 35 | — | — | ns |
| \overline{CE} Pulse Width High | t _{EHEL} | t _{CPH} | 25 | — | — | 25 | — | — | ns |
| Write Pulse Width High | t _{WHWL} | t _{WPH} | 30 | — | — | 30 | — | — | ns |
| Effective Page Programming Time (Write Buffer Programming) | Per Word | t _{WHWH1} | — | 23.5 | — | — | 23.5 | — | μs |
| Programming Time | | | | Word | — | 100 | — | — | 100 |
| Sector Erase Operation *1 | t _{WHWH2} | t _{WHWH2} | — | 1.0 | — | — | 1.0 | — | s |
| V _{CC} Setup Time | — | t _{VCS} | 50 | — | — | 50 | — | — | μs |
| Recovery Time From RY/ \overline{BY} | — | t _{PB} | 0 | — | — | 0 | — | — | ns |
| Erase/Program Valid to RY/ \overline{BY} Delay | — | t _{BUSY} | — | — | 90 | — | — | 90 | ns |
| Rise Time to V _{ID} *2 | — | t _{VIDR} | 500 | — | — | 500 | — | — | ns |
| Rise Time to V _{ACC} *3 | — | t _{VACCR} | 500 | — | — | 500 | — | — | ns |
| Voltage Transition Time *2 | — | t _{VLHT} | 4 | — | — | 4 | — | — | μs |

(Continued)

MBM29PL32TM/BM_{90/10}

(Continued)

| Parameter | Symbol | | Value | | | | | | Unit |
|---|--------|-------------------|-------|-----|-----|-----|-----|-----|------|
| | | | 90 | | | 10 | | | |
| | JEDEC | Standard | Min | Typ | Max | Min | Typ | Max | |
| Write Pulse Width *2 | — | t _{WPP} | 100 | — | — | 100 | — | — | μs |
| \overline{OE} Setup Time to \overline{WE} Active *2 | — | t _{OESP} | 4 | — | — | 4 | — | — | μs |
| \overline{CE} Setup Time to \overline{WE} Active *2 | — | t _{CSP} | 4 | — | — | 4 | — | — | μs |
| \overline{RESET} Pulse Width | — | t _{RP} | 500 | — | — | 500 | — | — | ns |
| \overline{RESET} High Time Before Read | — | t _{RH} | 100 | — | — | 100 | — | — | ns |
| Delay Time from Embedded Output Enable | — | t _{EOE} | — | — | 90 | — | — | 100 | ns |
| Erase Time-out Time | — | t _{TOW} | 50 | — | — | 50 | — | — | μs |
| Erase Suspend Transition Time | — | t _{SPD} | — | — | 20 | — | — | 20 | μs |

*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Group Protection operation.

*3 : This timing is for Accelerated Program operation.

■ ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Unit | Remarks |
|--|---------|------|------|-------|--|
| | Min | Typ | Max | | |
| Sector Erase Time | — | 1 | 15 | s | Excludes programming time prior to erasure |
| Programming Time | — | 100 | 3000 | μs | Excludes system-level overhead |
| Effective Page Programming Time (Write Buffer Programming) | — | 23.5 | — | μs | |
| Chip Programming Time | — | — | 300 | s | |
| Absolute Maximum Programming Time (16 words) | — | — | 6 | ms | Non programming within the same page |
| Erase/Program Cycle | 100,000 | — | — | cycle | — |

■ TSOP (1) PIN CAPACITANCE

| Parameter | Symbol | Test Setup | Value | | Unit |
|---|------------------|----------------------|-------|-----|------|
| | | | Typ | Max | |
| Input Capacitance | C _{IN} | V _{IN} = 0 | 8 | 10 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} = 0 | 8.5 | 12 | pF |
| Control Pin Capacitance | C _{IN2} | V _{IN} = 0 | 8 | 10 | pF |
| Reset pin and \overline{WP}/ACC Pin Capacitance | C _{IN3} | V _{IN} = 0 | 20 | 25 | pF |

Notes : • Test conditions T_A = +25°C, f = 1.0 MHz
 • DQ₁₅/A-1 pin capacitance is stipulated by output capacitance.

■ FBGA PIN CAPACITANCE

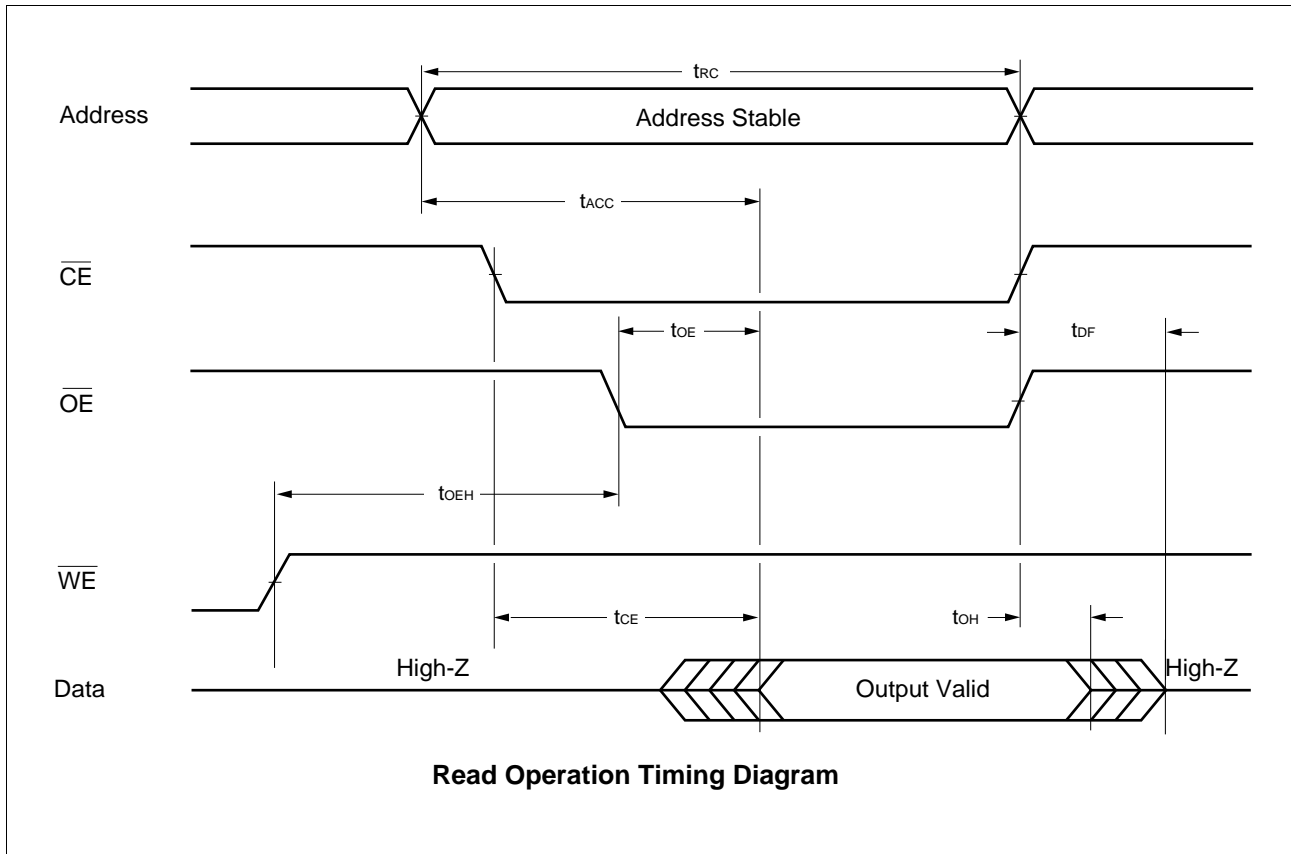
| Parameter | Symbol | Test Setup | Value | | Unit |
|-------------------------------------|------------------|----------------------|-------|-----|------|
| | | | Typ | Max | |
| Input Capacitance | C _{IN} | V _{IN} = 0 | TBD | TBD | pF |
| Output Capacitance | C _{OUT} | V _{OUT} = 0 | TBD | TBD | pF |
| Control Pin Capacitance | C _{IN2} | V _{IN} = 0 | TBD | TBD | pF |
| \overline{WP}/ACC Pin Capacitance | C _{IN3} | V _{IN} = 0 | TBD | TBD | pF |

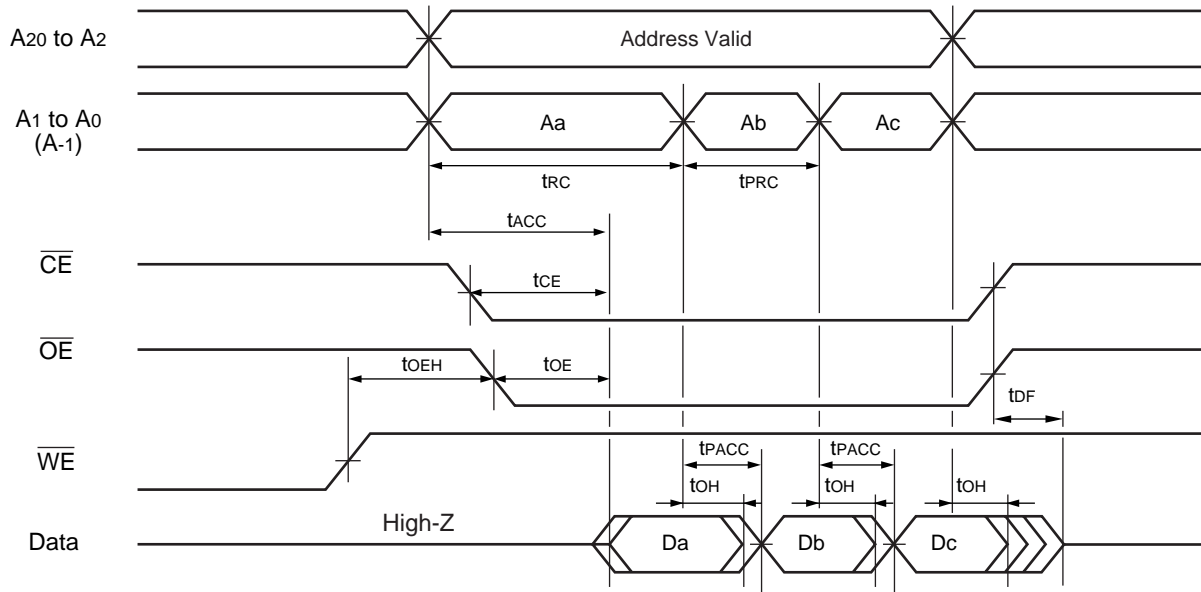
Notes : • Test conditions T_A = +25°C, f = 1.0 MHz
 • DQ₁₅/A-1 pin capacitance is stipulated by output capacitance.

SWITCHING WAVEFORMS

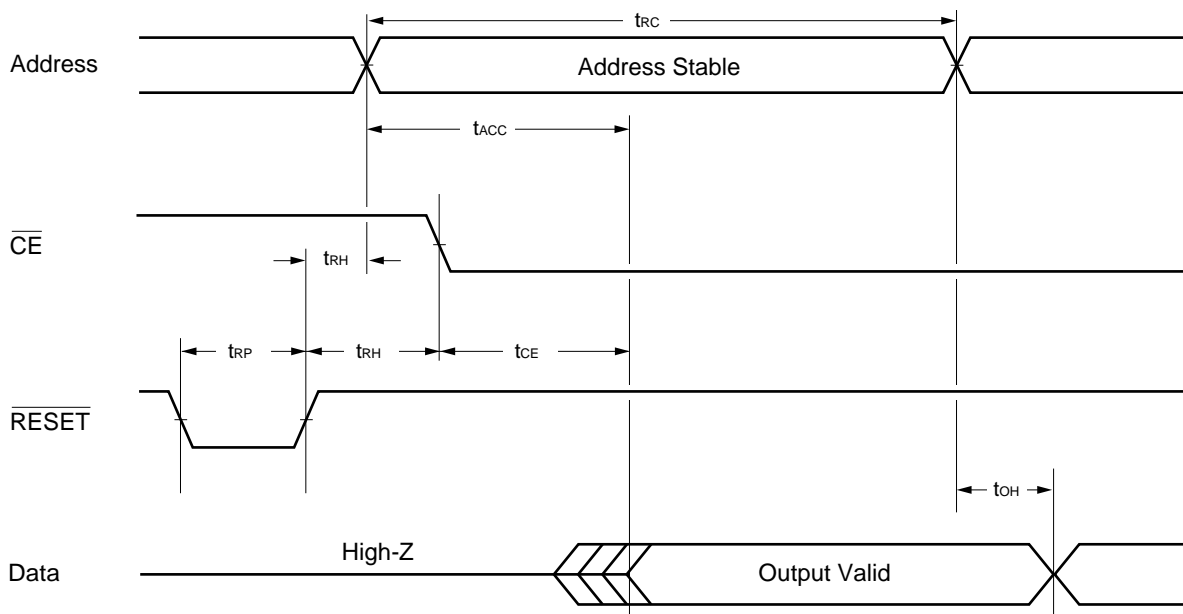
Key to Switching Waveforms

| WAVEFORM | INPUTS | OUTPUTS |
|----------|---------------------------------|---|
| | Must Be Steady | Will Be Steady |
| | May Change from H to L | Will Be Changing from H to L |
| | May Change from L to H | Will Be Changing from L to H |
| | "H" or "L" Any Change Permitted | Changing State Unknown |
| | Does Not Apply | Center Line is High-Impedance "Off" State |

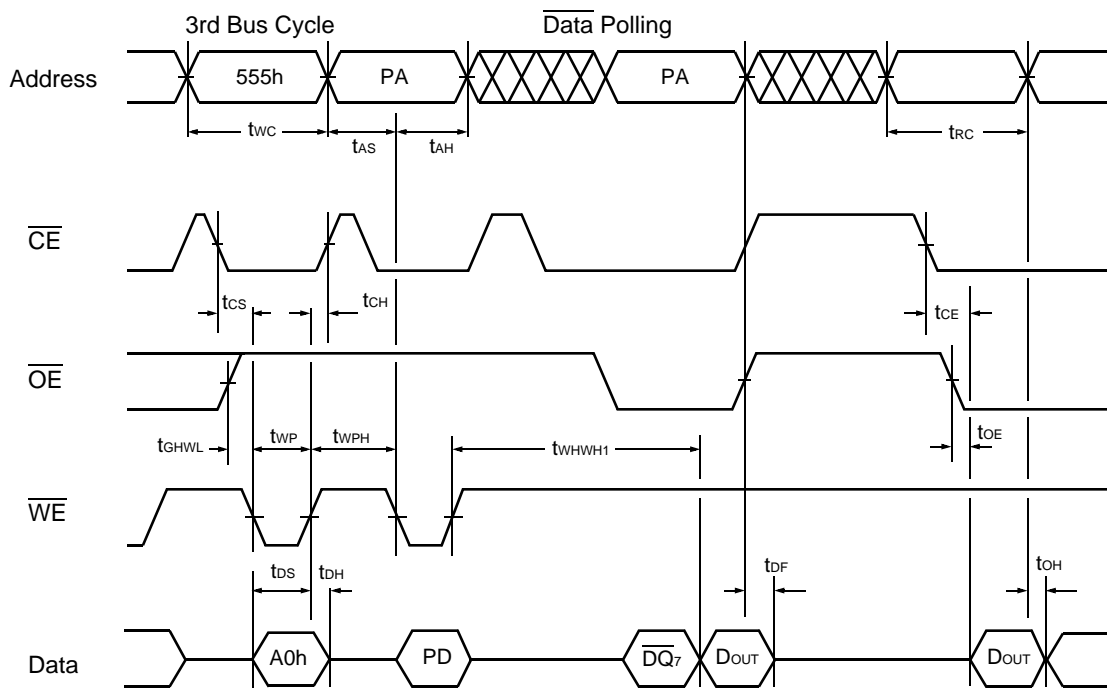




Page Read Operation Timing Diagram

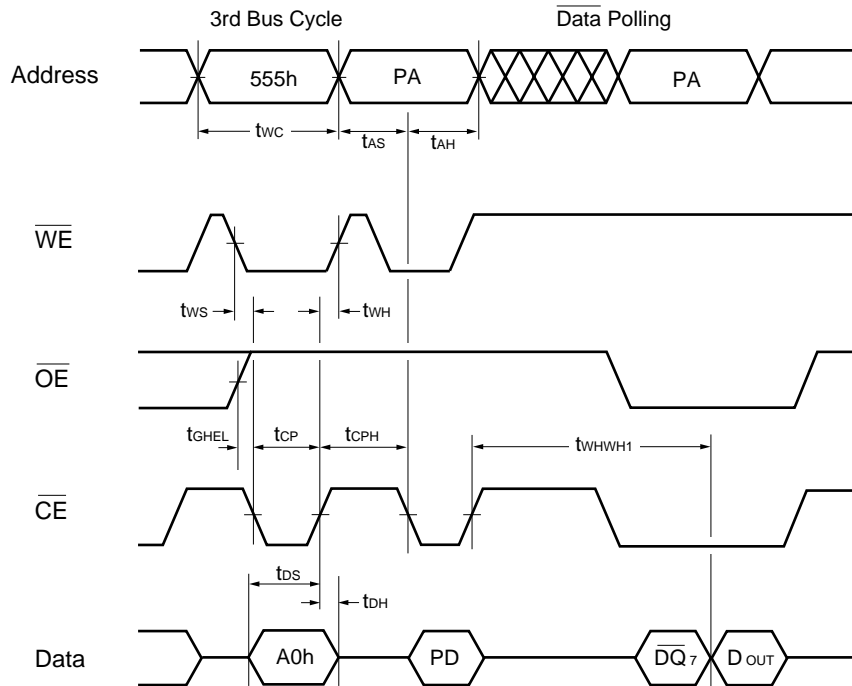


Hardware Reset/Read Operation Timing Diagram



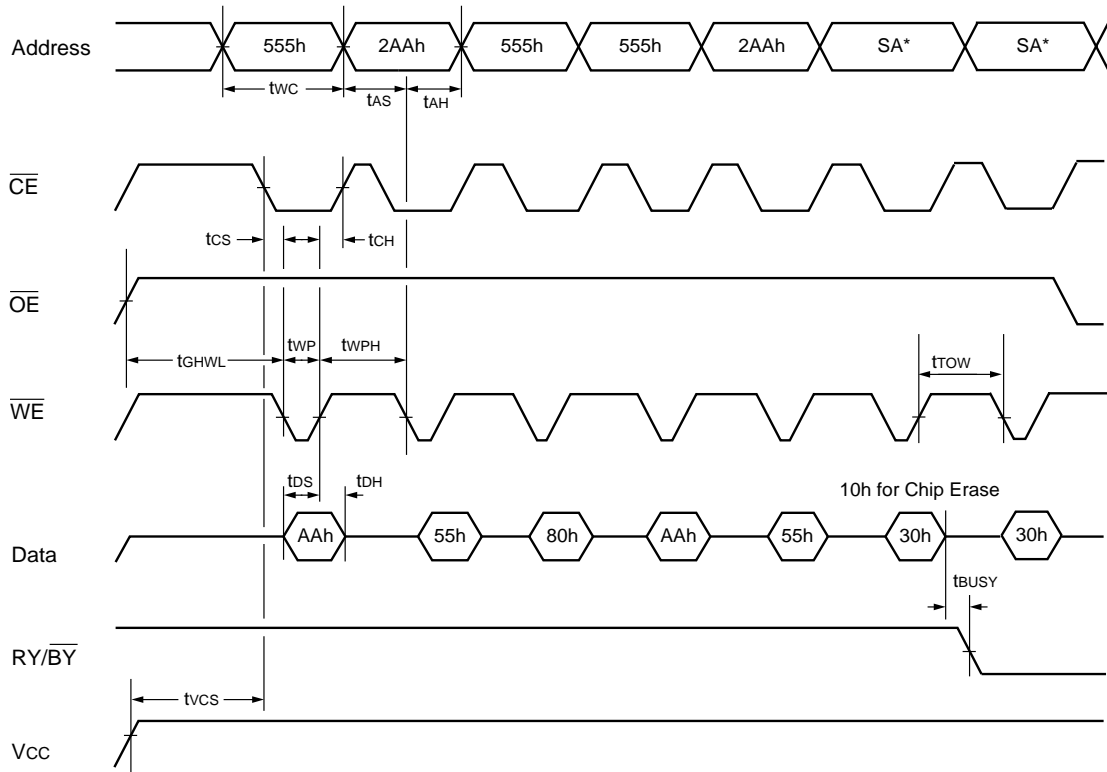
- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at word address.
 - \overline{DQ}_7 is the output of the complement of the data written to the device.
 - D_{OUT} is the output of the data written to the device.
 - Figure indicates the last two bus cycles out of four bus cycle sequence.

Alternate \overline{WE} Controlled Program Operation Timing Diagram



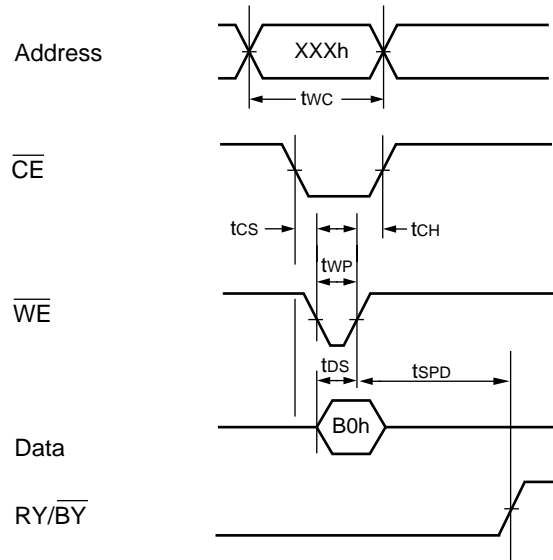
- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at word address.
 - \overline{DQ}_7 is the output of the complement of the data written to the device.
 - D_{OUT} is the output of the data written to the device.
 - Figure indicates the last two bus cycles out of four bus cycle sequence.

Alternate \overline{CE} Controlled Program Operation Timing Diagram

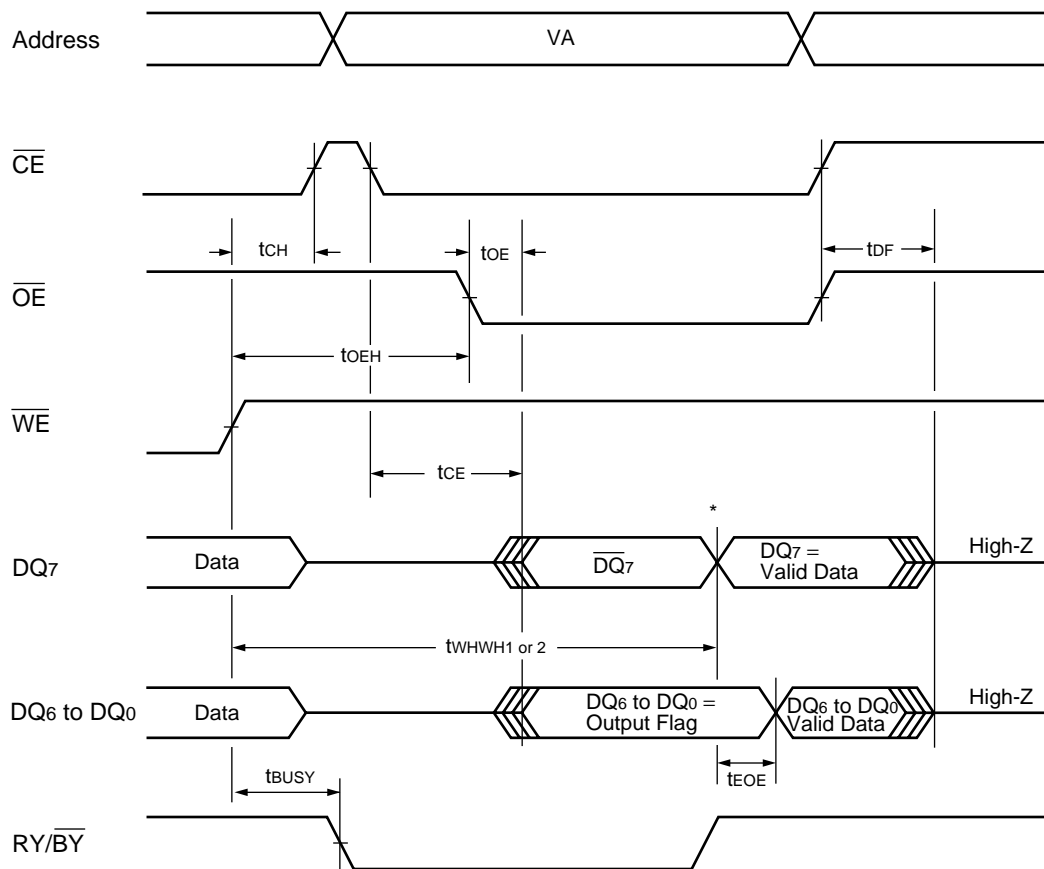


* : SA is the sector address for Sector Erase. Address = 555h (Word), AAh (Byte) for Chip Erase.

Chip/Sector Erase Operation Timing Diagram

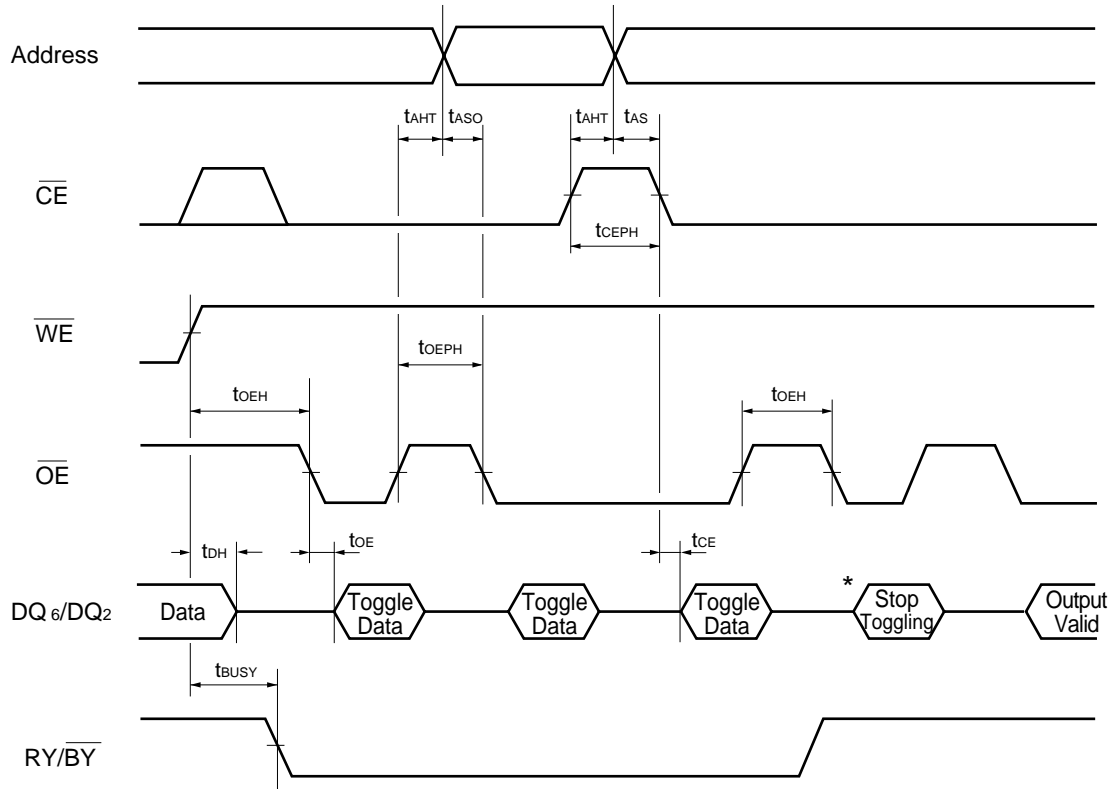


Erase Suspend Operation Timing Diagram



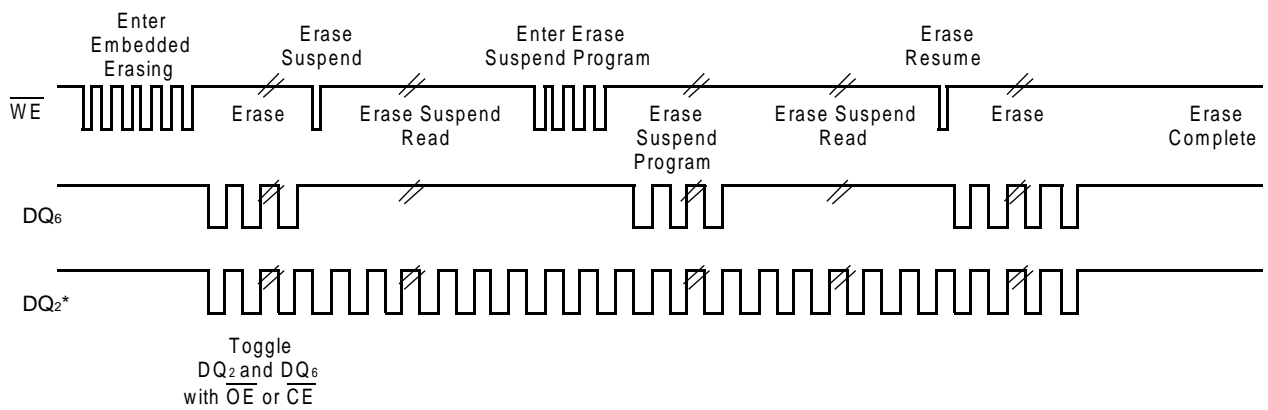
* : DQ₇ = Valid Data (The device has completed the Embedded operation.)

\overline{Data} Polling during Embedded Algorithm Operation Timing Diagram



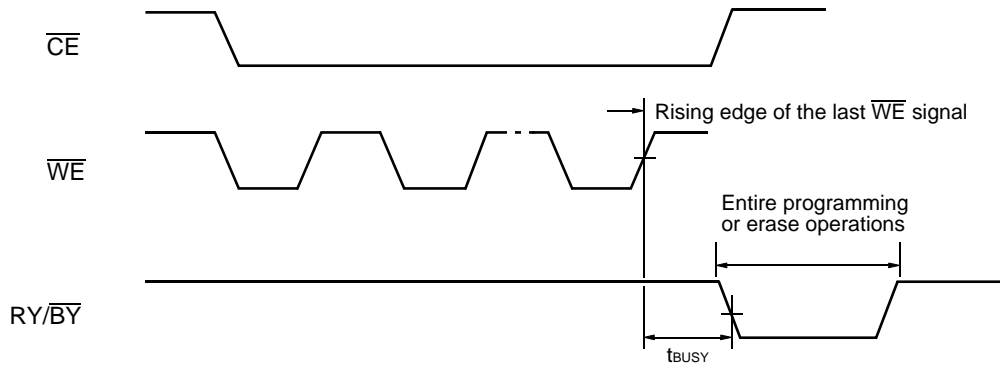
* : DQ_6 stops toggling (The device has completed the Embedded operation).

Toggle Bit I Timing Diagram during Embedded Algorithm Operations

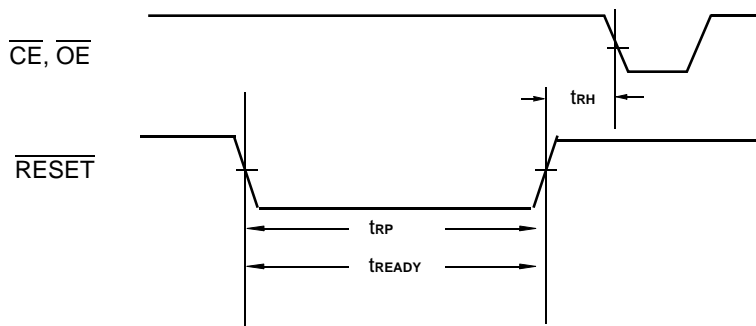


* : DQ_2 is read from the erase-suspended sector.

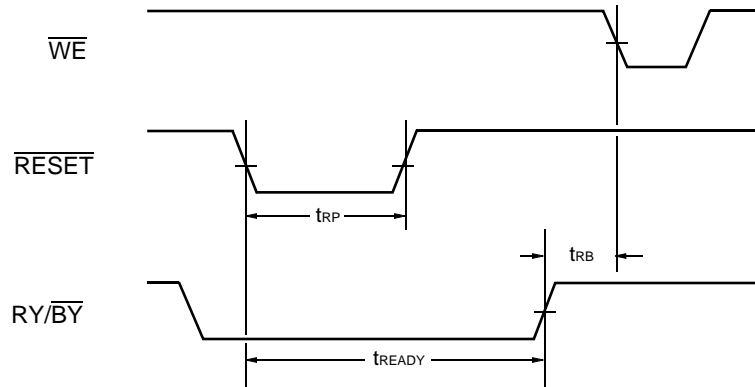
DQ_2 vs. DQ_6



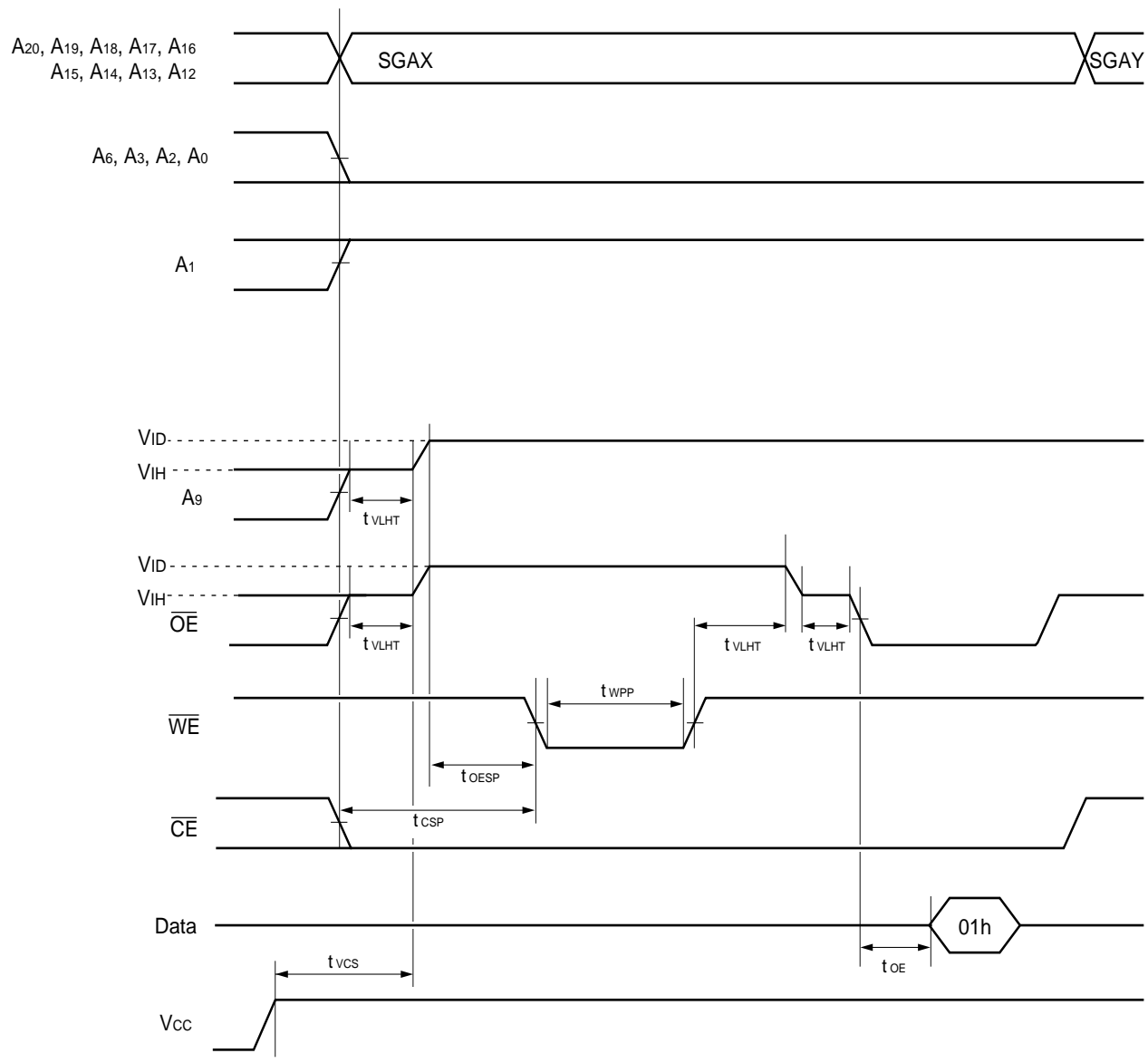
RY/\overline{BY} Timing Diagram during Program/Erase Operation Timing Diagram



\overline{RESET} Timing Diagram (Not during Embedded Algorithms)

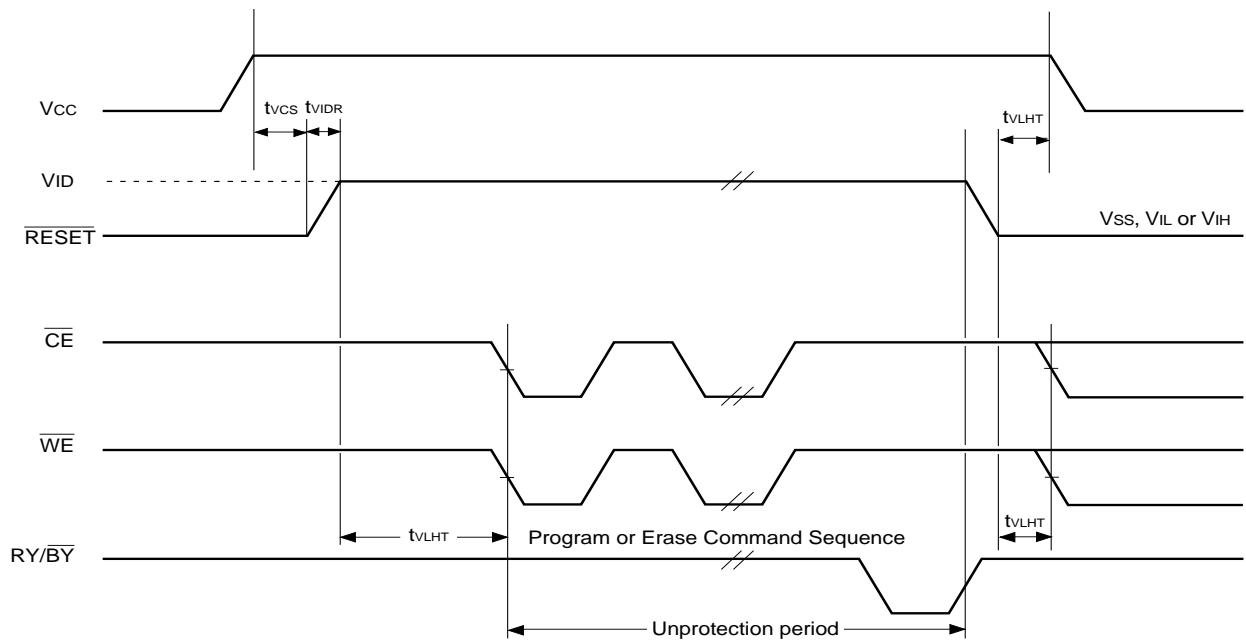


\overline{RESET} Timing Diagram (During Embedded Algorithms)

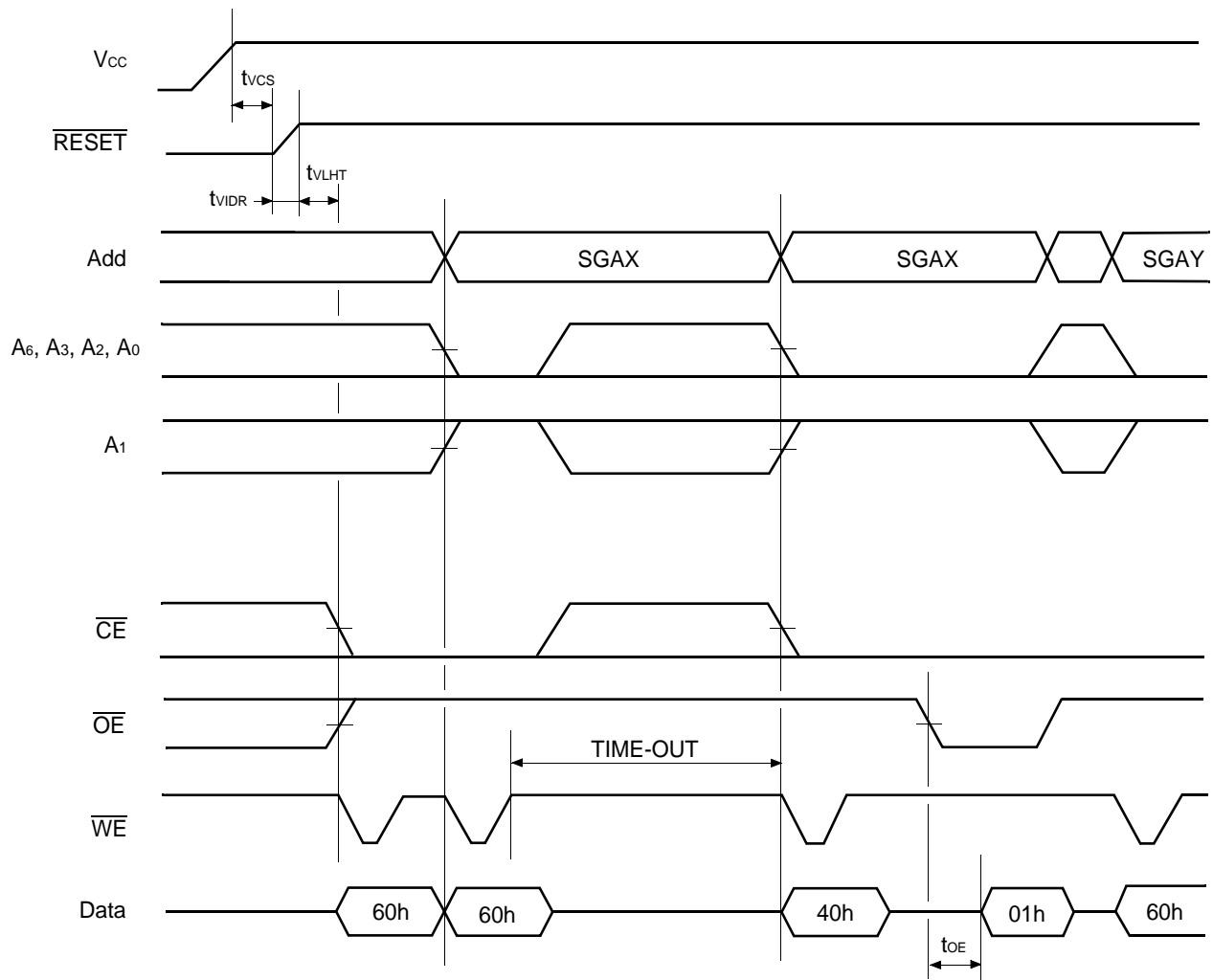


SGAX : Sector Group Address to be protected
 SGAY : Next Sector Group Address to be protected

Sector Group Protection Timing Diagram

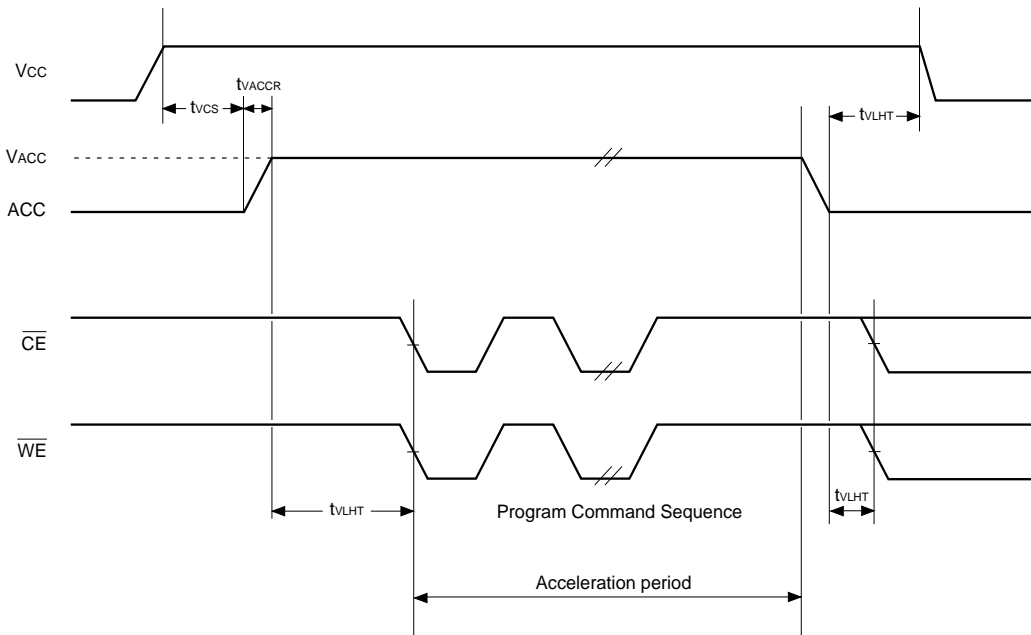


Temporary Sector Group Unprotection Timing Diagram



SGAX: Sector Group Address to be protected
 SGAY : Next Sector Group Address to be protected
 TIME-OUT : Time-Out window = 250 μs (Min)

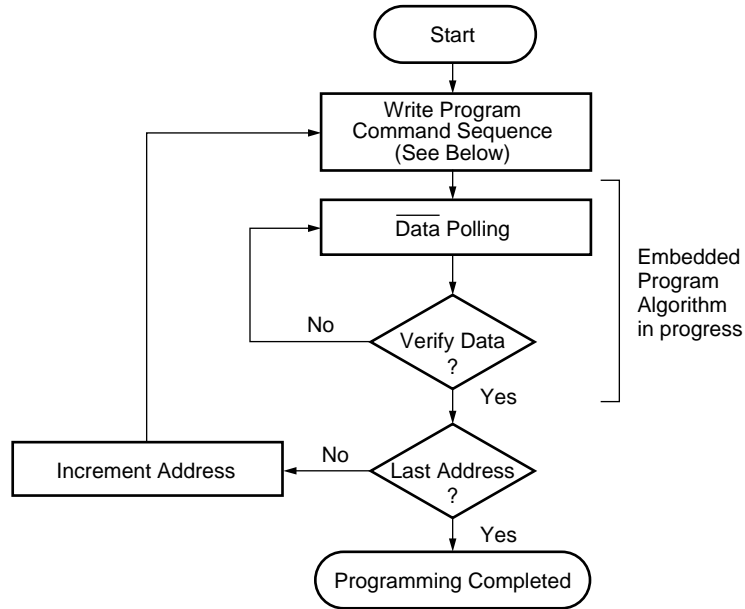
Extended Sector Group Protection Timing Diagram



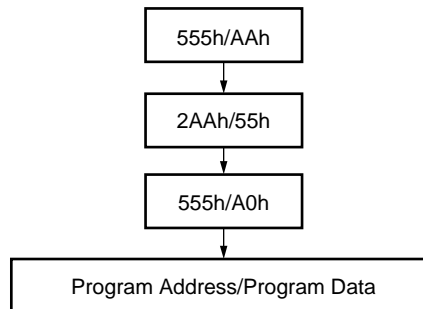
Accelerated Program Timing Diagram

■ FLOW CHART

EMBEDDED ALGORITHMS



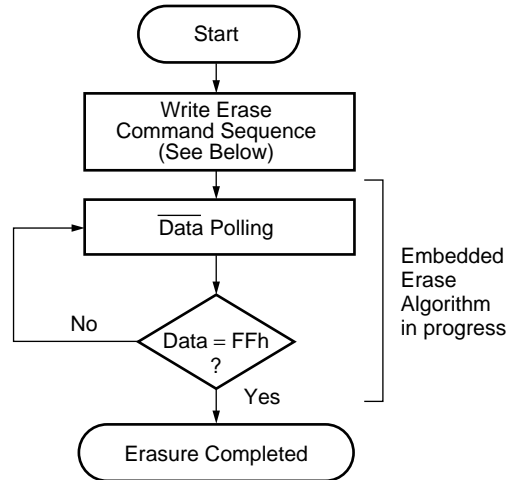
Program Command Sequence (Address/Command):



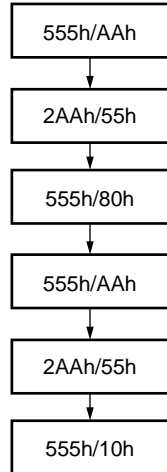
Note : The sequence is applied for Word (×16) mode.
The addresses differ from Byte (×8) mode.

Embedded Program™ Algorithm

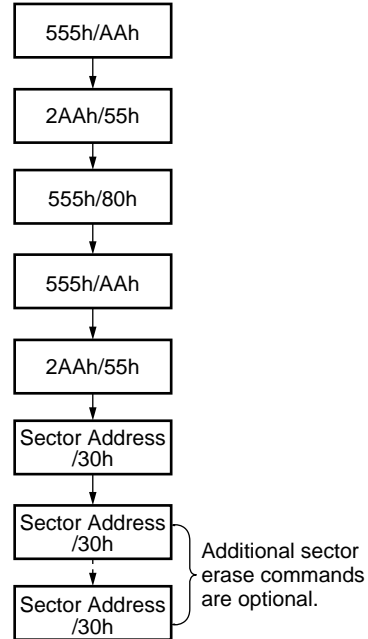
EMBEDDED ALGORITHMS



Chip Erase Command Sequence
(Address/Command):

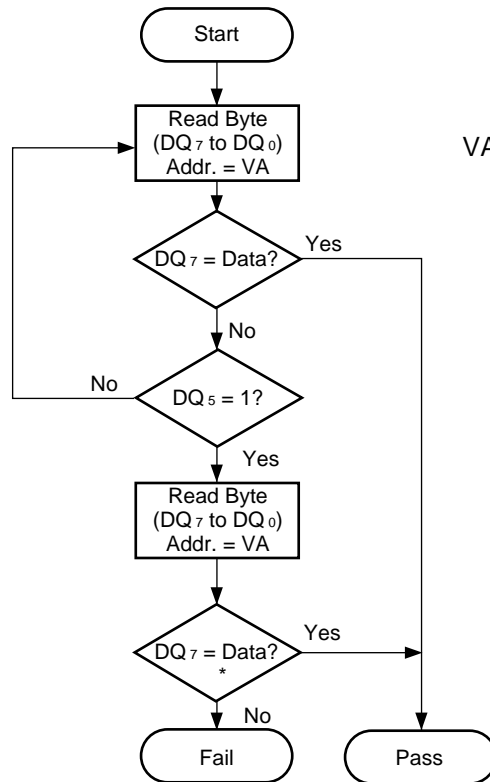


Individual Sector/Multiple Sector
Erase Command Sequence
(Address/Command):



Note : The sequence is applied for Word (×16) mode.
The addresses differ from Byte (× 8) mode.

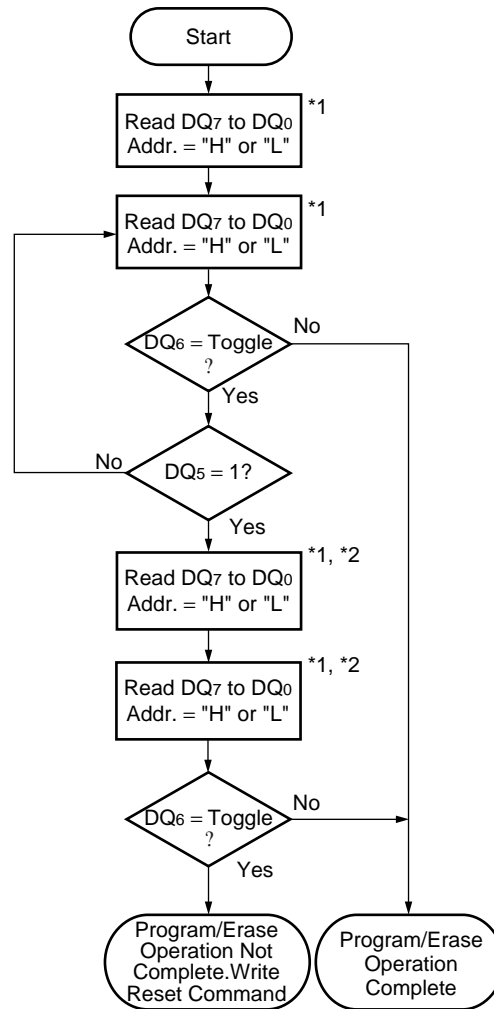
Embedded Erase™ Algorithm



VA = Valid address for programming
 = Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation
 = Any of the sector addresses within the sector not being protected during chip erase operation

* : DQ₇ is rechecked even if DQ₅ = "1" because DQ₇ may change simultaneously with DQ₅.

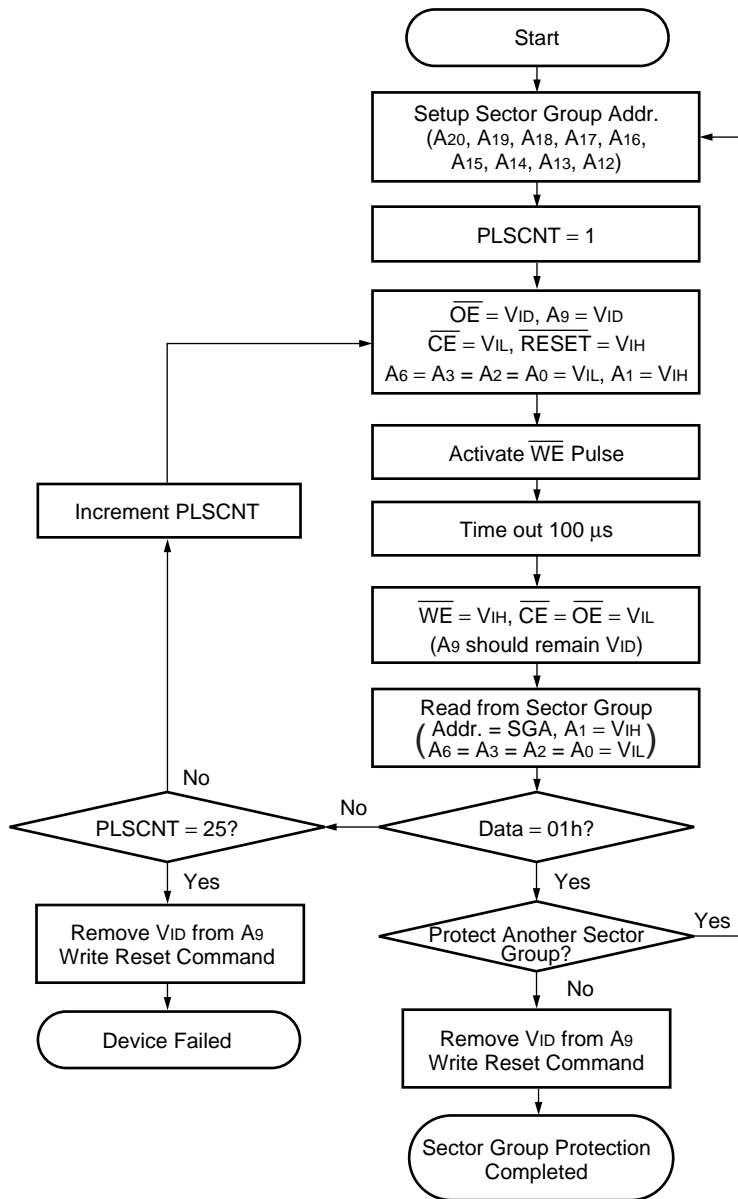
Data Polling Algorithm



*1 : Read Toggle bit twice to determine whether it is toggling.

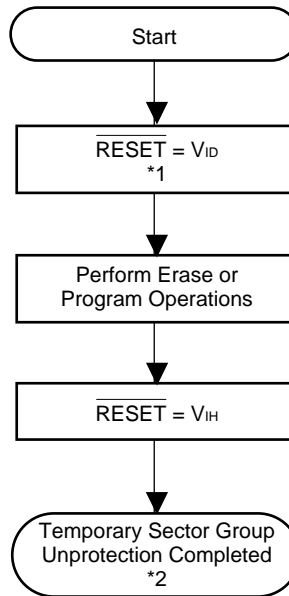
*2 : Recheck Toggle bit because it may stop toggling as DQ₅ changes to "1".

Toggle Bit Algorithm



* : A-1 is V_{IL} in Byte (× 8) mode.

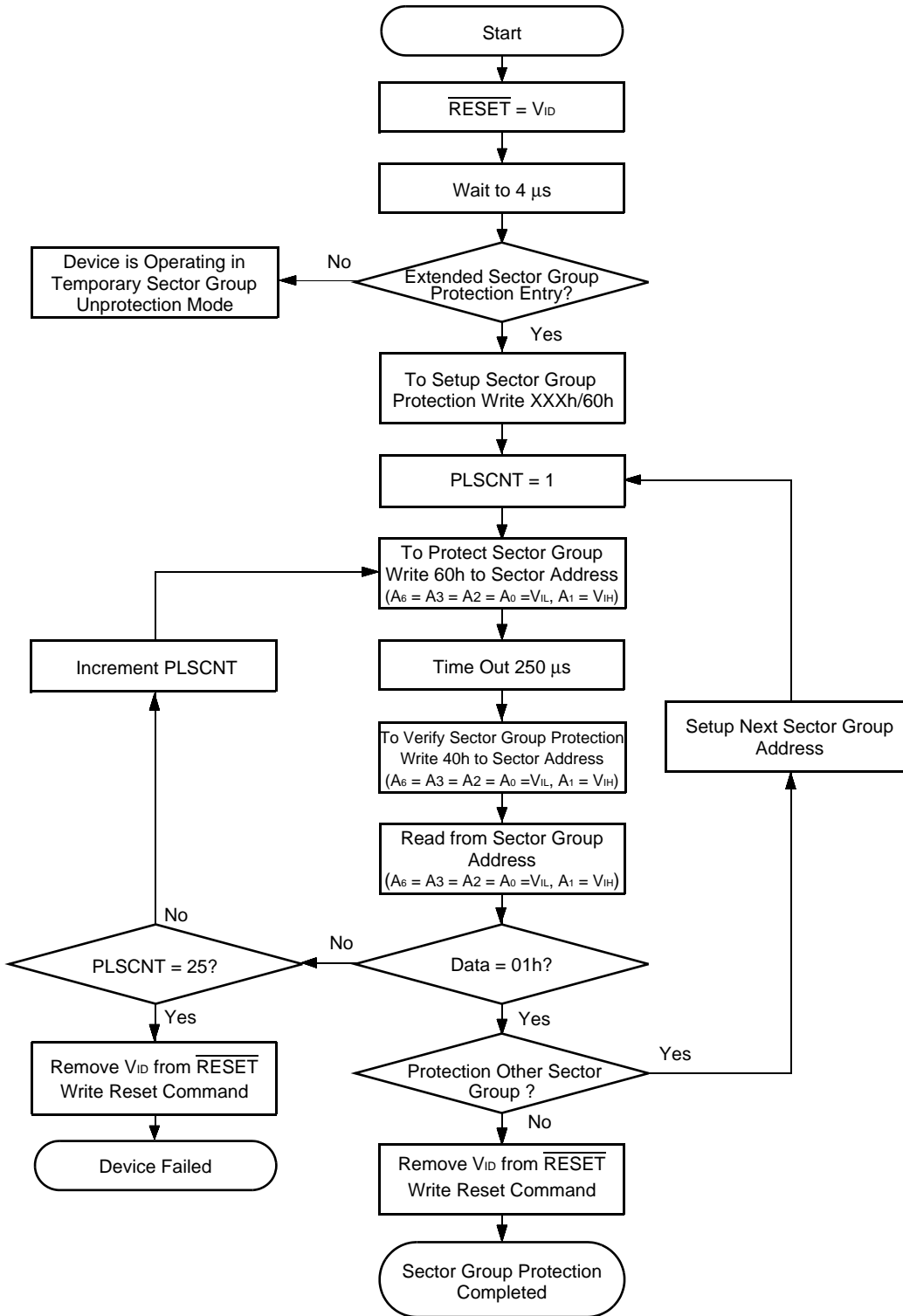
Sector Group Protection Algorithm



*1 : All protected sector groups are unprotected.

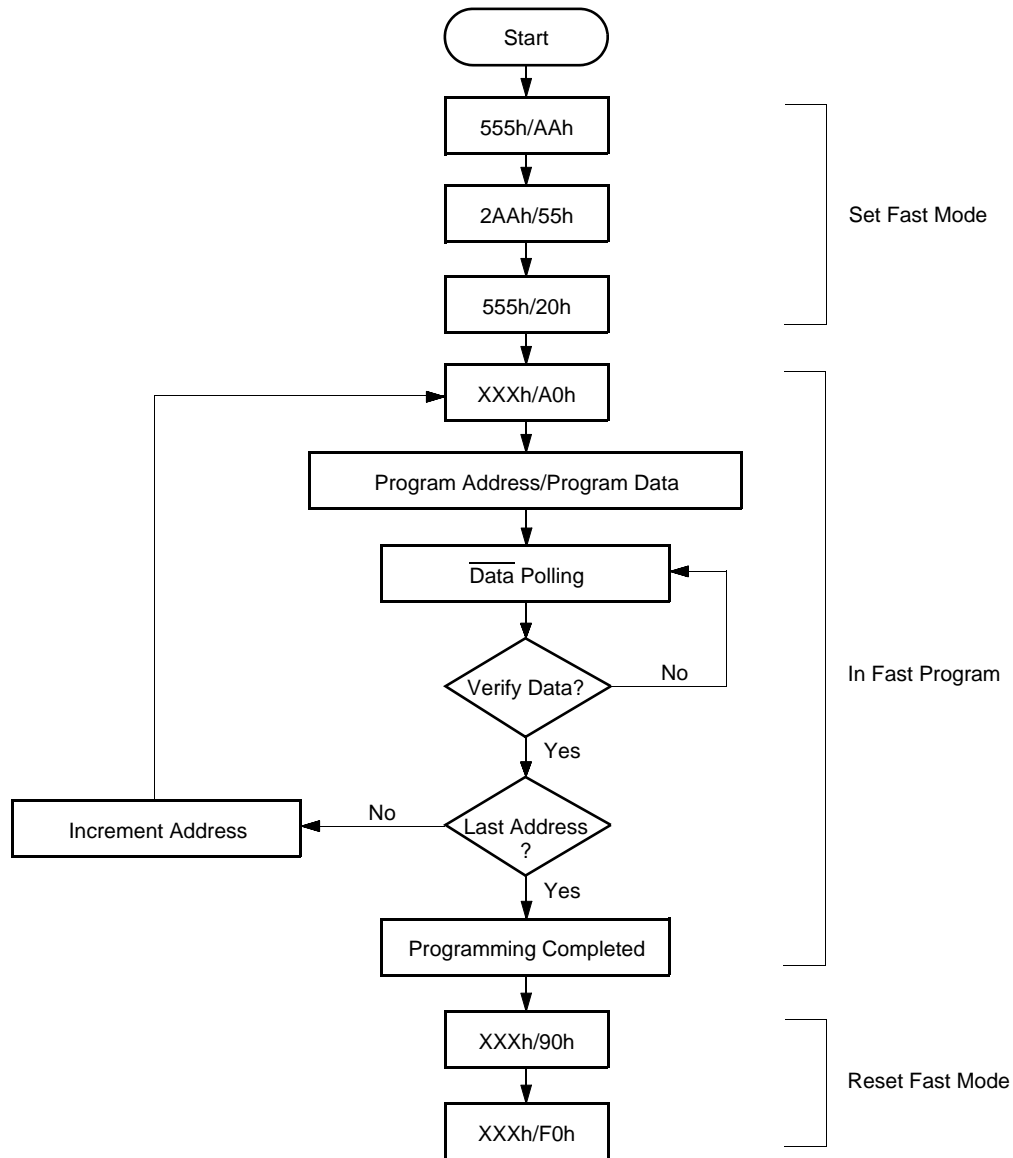
*2 : All previously protected sector groups are protected.

Temporary Sector Group Unprotection Algorithm



Extended Sector Group Protection Algorithm

FAST MODE ALGORITHM



- Notes :
- The sequence is applied for Word (× 16) mode.
 - The addresses differ from Byte (× 8) mode.

Embedded Program™ Algorithm for Fast Mode

MBM29PL32TM/BM_{90/10}

■ ORDERING INFORMATION

| Part No. | Package | Access Time (ns) | Remarks |
|------------------|--|------------------|---------------|
| MBM29PL32TM90TN | 48-pin, plastic TSOP (1) (FPT-48P-M19) (Normal Bend) | 90 ns | Top Sector |
| MBM29PL32TM10TN | | 100 ns | |
| MBM29PL32TM90PBT | 48-ball, plastic FBGA (BGA-48P-M20) | 90 ns | |
| MBM29PL32TM10PBT | | 100 ns | |
| MBM29PL32BM90TN | 48-pin, plastic TSOP (1) (FPT-48P-M19) (Normal Bend) | 90 ns | Bottom Sector |
| MBM29PL32BM10TN | | 100 ns | |
| MBM29PL32BM90PBT | 48-ball, plastic FBGA (BGA-48P-M20) | 90 ns | |
| MBM29PL32BM10PBT | | 100 ns | |

MBM29PL32TM/BM

90

TN

PACKAGE TYPE

TN = 48-Pin Thin Small Outline Package
(TSOP(1)) Standard Pinout

PBT = 48-Ball Fine pitch Ball Grid Array
Package (FBGA)

SPEED OPTION

90 = 90ns access time

10 = 100ns access time

DEVICE NUMBER/DESCRIPTION

32 Mega-bit (4M × 8/2M × 16) MirrorFlash with Page Mode,
Boot Sector

3.0 V-only Read, Program, and Erase

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(1)
(FPT-48P-M19)

Note 1) * : Values do not include resin protrusion.

Resin protrusion and gate protrusion are +0.15(.006)Max(each side).

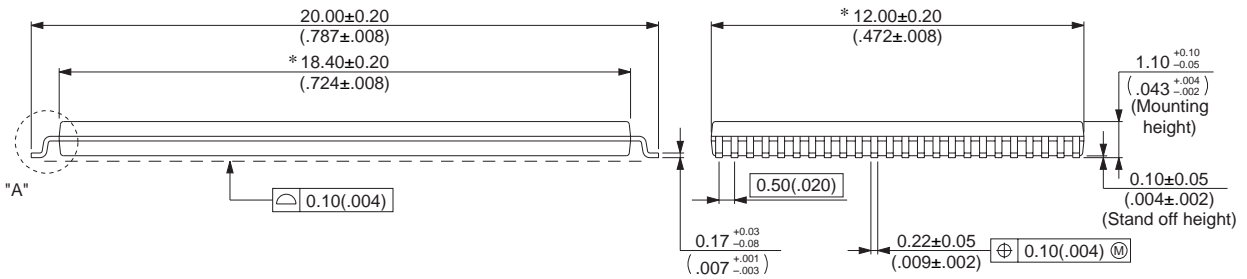
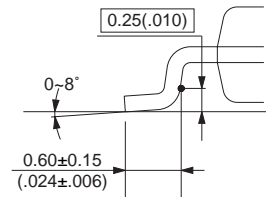
Note 2) Pins width and pins thickness include plating thickness.

Note 3) Pins width do not include tie bar cutting remainder.

LEAD No.



Details of "A" part



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Dimensions in mm (inches)

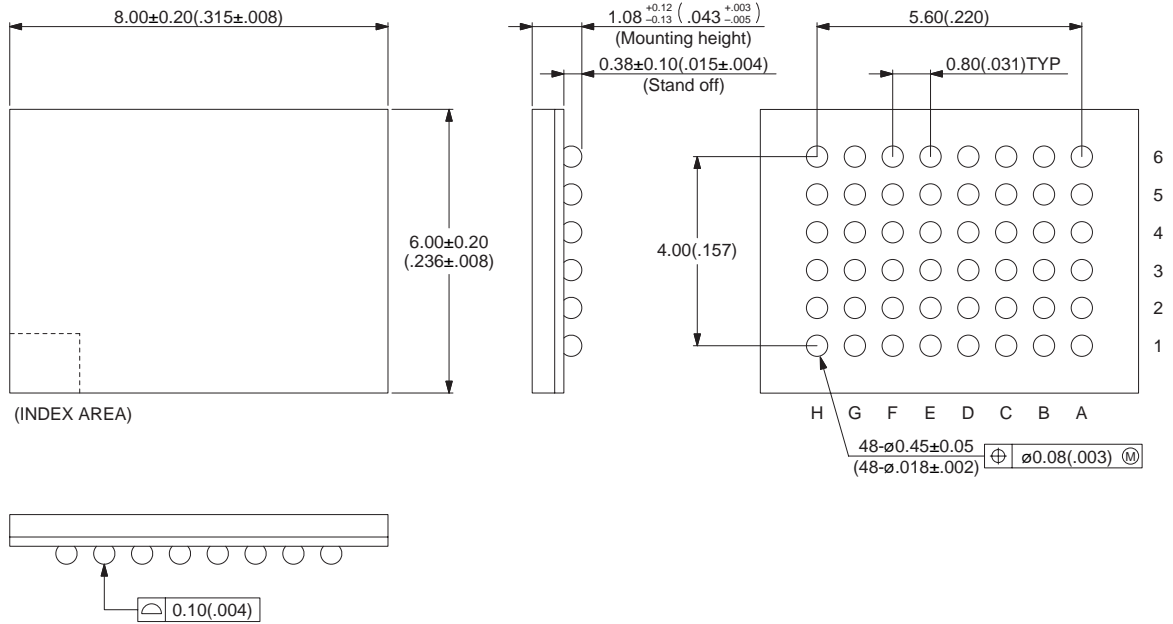
Note : The values in parentheses are reference values.

(Continued)

MBM29PL32TM/BM_{90/10}

(Continued)

48-ball plastic FBGA
(BGA-48P-M20)



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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